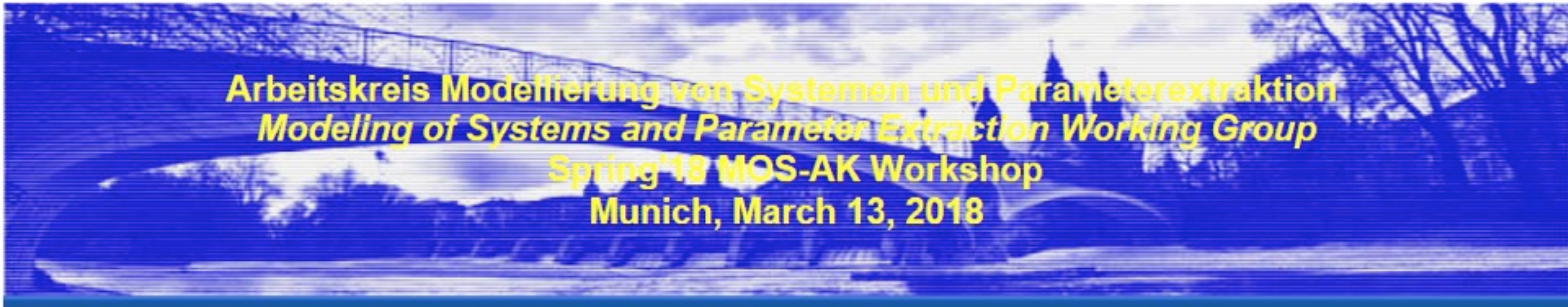


Virtual prototyping for power diode and IGBT development

Maria Cotorogea
Peter Türkes
Andreas Groove

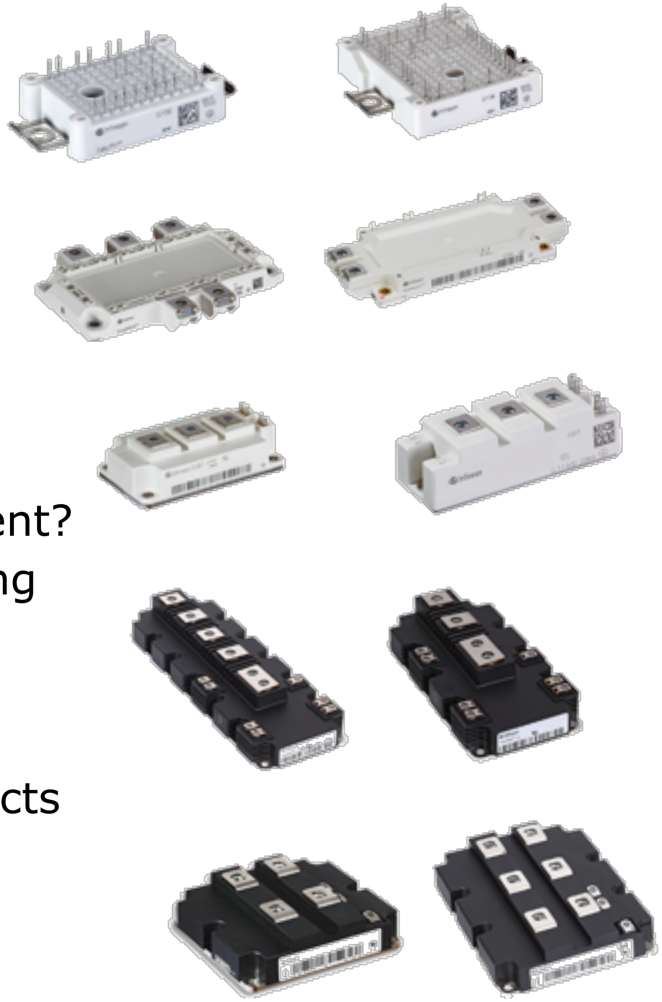
MOS-AK Worshop
Munich, March 13, 2018

Outline

Outline

Introduction

- IGBTs and power diodes are bipolar devices
- Losses are dominated by stored charges
- **Development target:** higher power density
  higher switching frequencies
- **IGBT-modules:**
  - Chip development
  - Package development
- Virtual Prototyping Group in Munich
- Why virtual prototyping in IGBT-module development?
  - Reduce development costs and time by reducing learning cycles
- **Target:** accurately predict switching behavior
- **Strategy:** rollout on technology and package projects
- **Model requirements:**
  - physics based models for IGBTs and diodes
  - knowledge of parasitic elements and couplings
  - fast model implementation and simulation



Introduction

Not in focus

- Device triggered oscillation mechanisms
- Failure mechanisms
- Device reliability

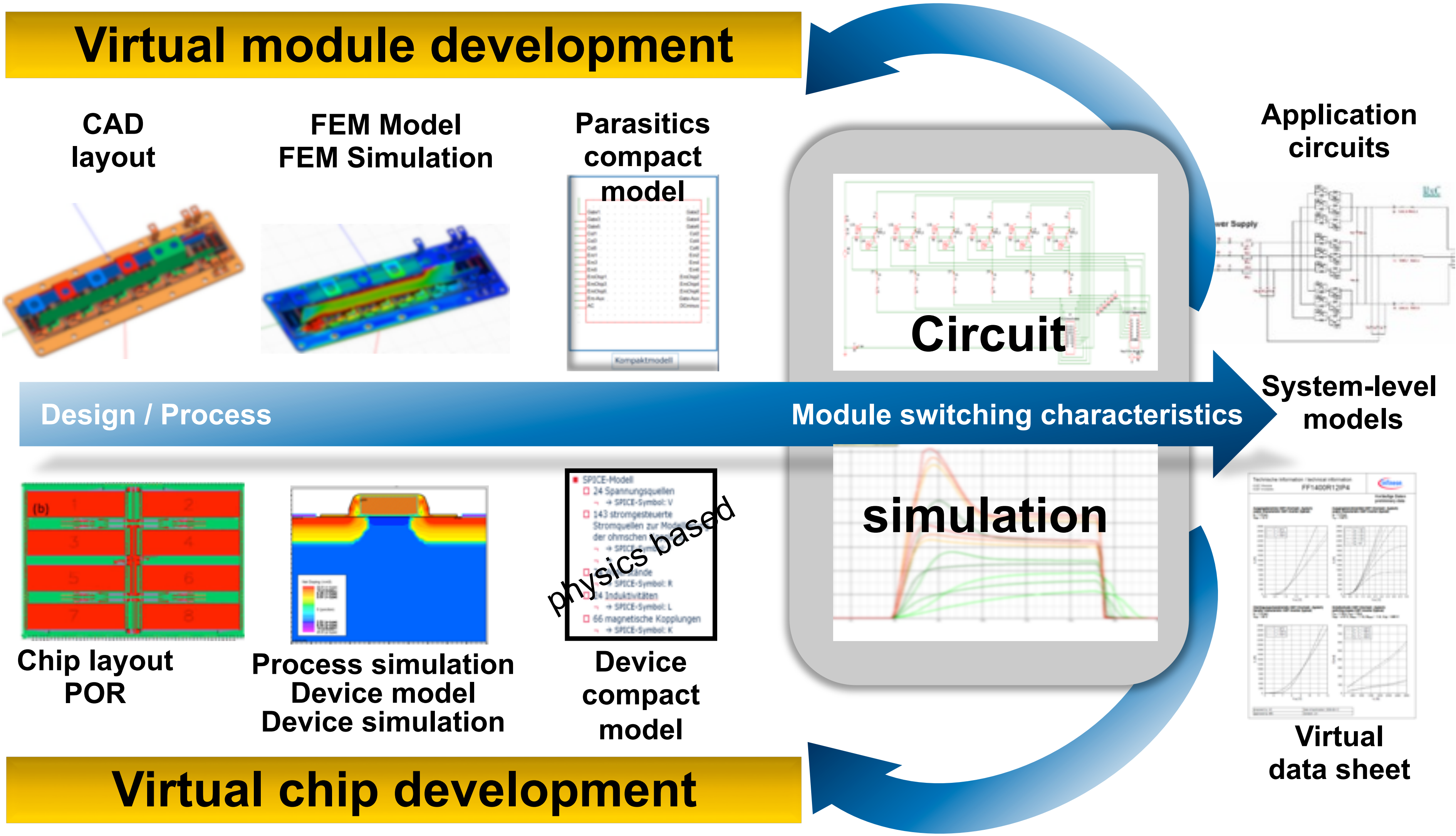
Outcome of VP activities

- Provide interfaces between different simulation levels (device simulation → circuit simulation → system simulation)
- Evaluate and enhance today's modeling precision of compact models to describe switching behavior of bipolar devices within SOA
- Consider electrical parasitics due to package design
- Assess current distribution in modules with several devices in parallel
- Investigate effect of manufacturing process tolerances in FE and BE
- Consider thermal couplings in modules and propose an electro-thermal co-simulation as full circuit-simulation approach

Outline

1. Introduction
2. Virtual Prototyping Approach
3. Compact modelling of power devices
4. Assessment of Model Precision
5. Electro-thermal co-simulation in SPICE
6. Summary and Outlook

Virtual Prototyping Approach
Virtual chip-module development flow



Virtual Prototyping Approach

General Concept behind the Idea

Switching behavior

- switching conditions
- power circuit & driver
- power devices & packages

} *inherent electrical & thermal couplings*

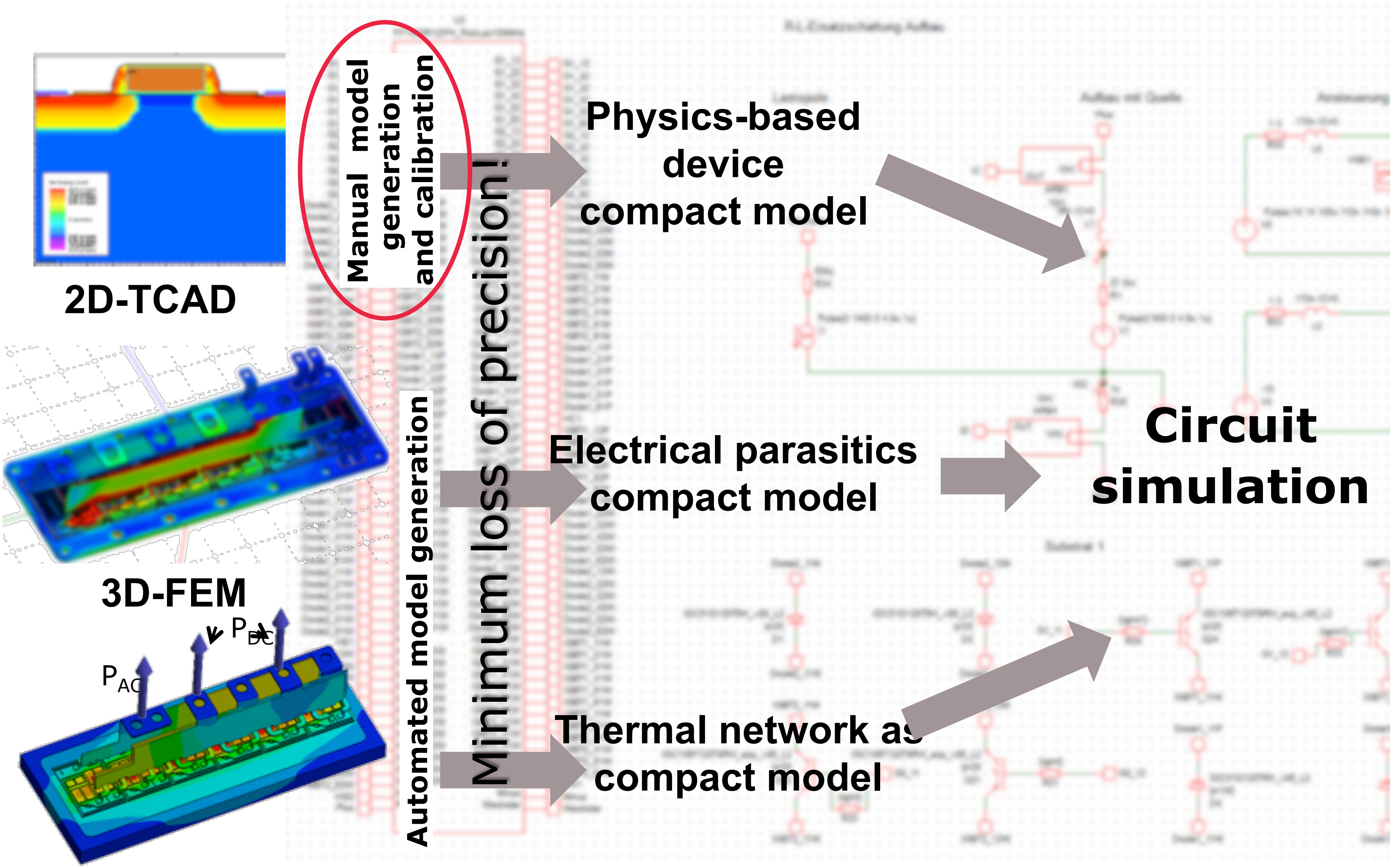
Conside-rations

- short time scale: high du/dt & di/dt
- large time scale: self-heating

Simulation needs

- appropriate electro-thermal models for IGBTs and diodes
- electrical and thermal parasitics models
- modeling techniques accounting for 2D or 3D geometrical design
- tools capable of facilitating a rapid iterative virtual design process

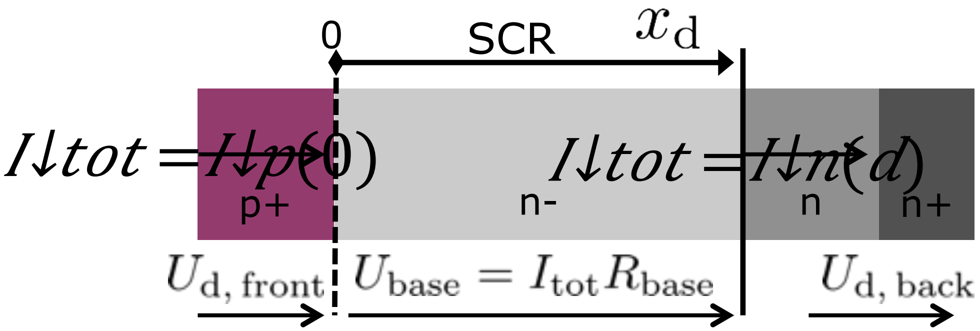
Virtual Prototyping Approach



Outline

Compact modelling of power devices

Description of charge dynamics in the drift region



Example: p-i-n diode

Determined by implicit equation, derived from Poisson-Equation

Approximation as a pure 1D problem!

Charge dynamics in the base is described by the ambipolar diffusion equation (ADE):

$$\frac{\partial p}{\partial t} = -\frac{p}{\tau} + D_a \frac{\partial^2 p}{\partial x^2}$$

$$\text{with } n \approx p \rightarrow R_{Base},\ Q_{base}$$

We need four boundary conditions

- Solution Methods for the local charge distribution:
  - Fourier Transformation
  - **Kraus-Approximation using hyperbolic Functions**
  - Finite Element Method (FEM)
  - **Finite Difference Method (FDM)**

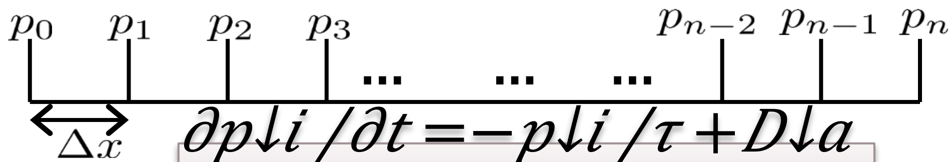
Disadvantages of FDM over Kraus-Ansatz

- FDM has more unknowns and thus equations
- The SPICE code is significantly more complex!
- Convergence: Choose the correct boundary conditions

Compact modelling of power devices

Description of charge dynamics in the drift region

- Discretize base into equidistant points where the carrier concentration is calculated



$$\frac{\partial p_i}{\partial t} = -\frac{p_i}{\tau} + D_a \frac{p_{i-1} - 2p_i + p_{i+1}}{\Delta x^2}$$

Each point one equation

- Time integration → directly calculated during transient analysis in SPICE
- Local integration for $Q_{base}(t)$ and $R_{base}(t)$ → discrete sums with SPICE subcircuit

Numerical Stable Boundary Conditions (BC)

- **Note:** Moving SCR boundary, thus Δx is changing with time
- High Injection at both junctions (anode & cathode):

$$p_0 = n_i \exp\left(\frac{2U_{d,front}}{V_T}\right) \qquad p_n \approx n_n = n_i \exp\left(\frac{2U_{d,back}}{V_T}\right)$$

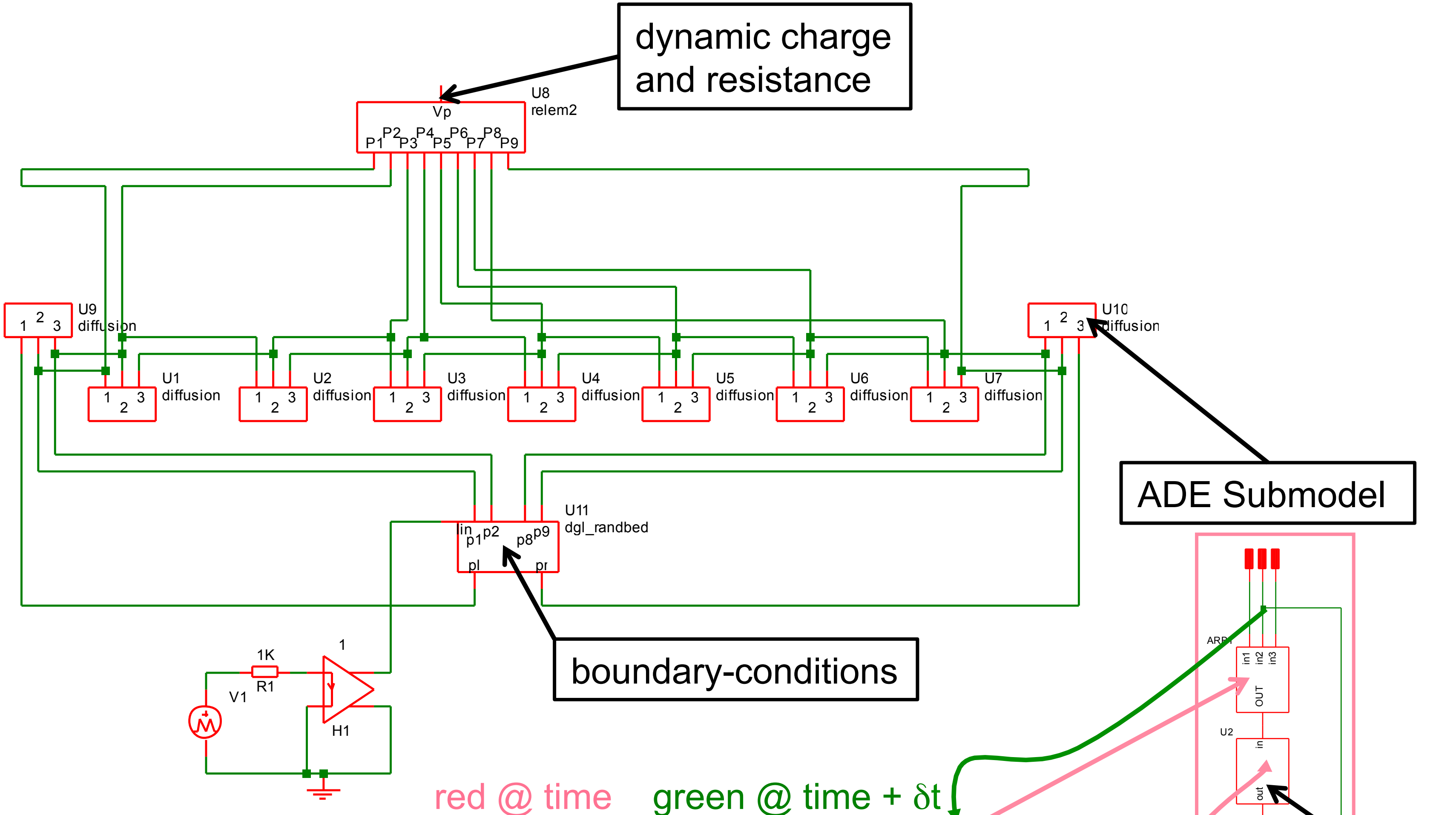
- First 4 and last 4 points are used in Lagrange polynomials for local gradients at both junctions (anode & cathode):

$$\frac{\partial p_0}{\partial x} = \frac{1}{6\Delta x}\left(-11p_0 + 18p_1 - 9p_2 + 2p_3\right) = -\frac{\mu_n}{\mu_n + \mu_p}\frac{1}{q \cdot A \cdot D} I_{tot}$$

$$\frac{\partial p_n}{\partial x} = \frac{1}{6\Delta x}\left(-2p_{n-3} + 9p_{n-2} - 18p_{n-1} + 11p_n\right) = \frac{\mu_p}{\mu_n + \mu_p}\frac{1}{q \cdot A \cdot D} I_{tot}$$

Compact modelling of power devices

Implementation of charge dynamics model in SPICE

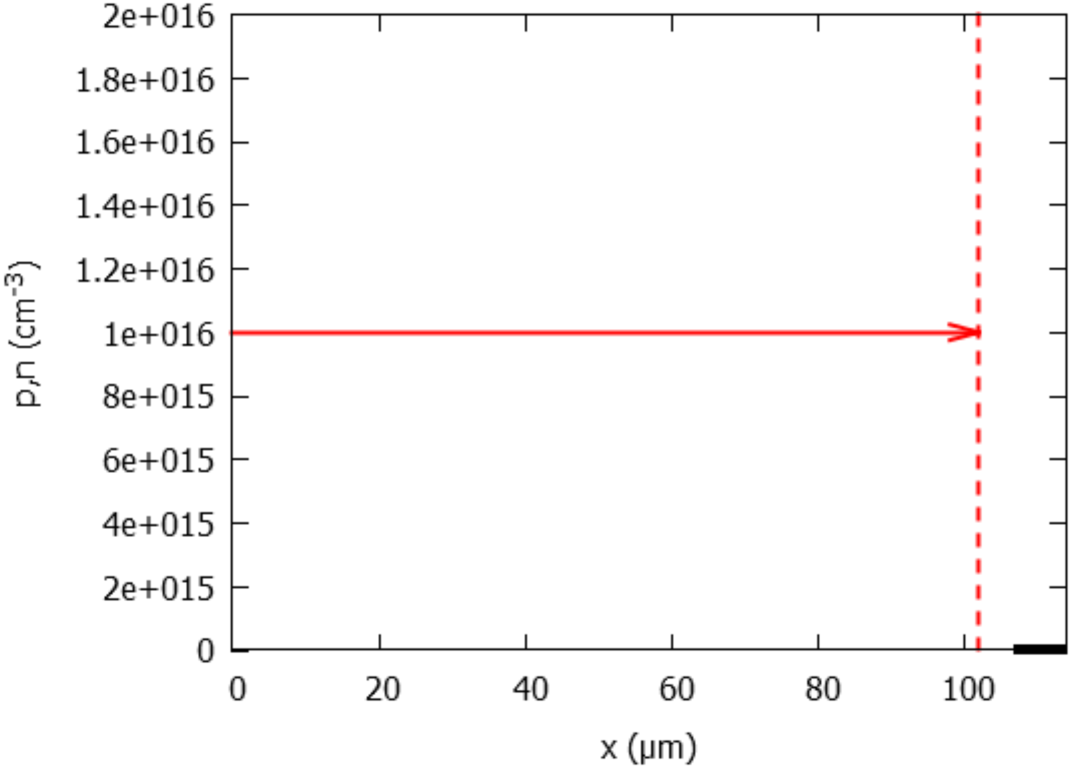


$$\frac{dp_i}{dt} = \frac{D\cdot\tau\cdot(p_{i-1}+p_{i+1}) - p_i\cdot(2\cdot D\cdot\tau+\delta x^2)}{\tau\cdot\delta x^2}$$

Compact modelling of power devices

Implementation of charge dynamics model in SPICE

For 20 discretization points

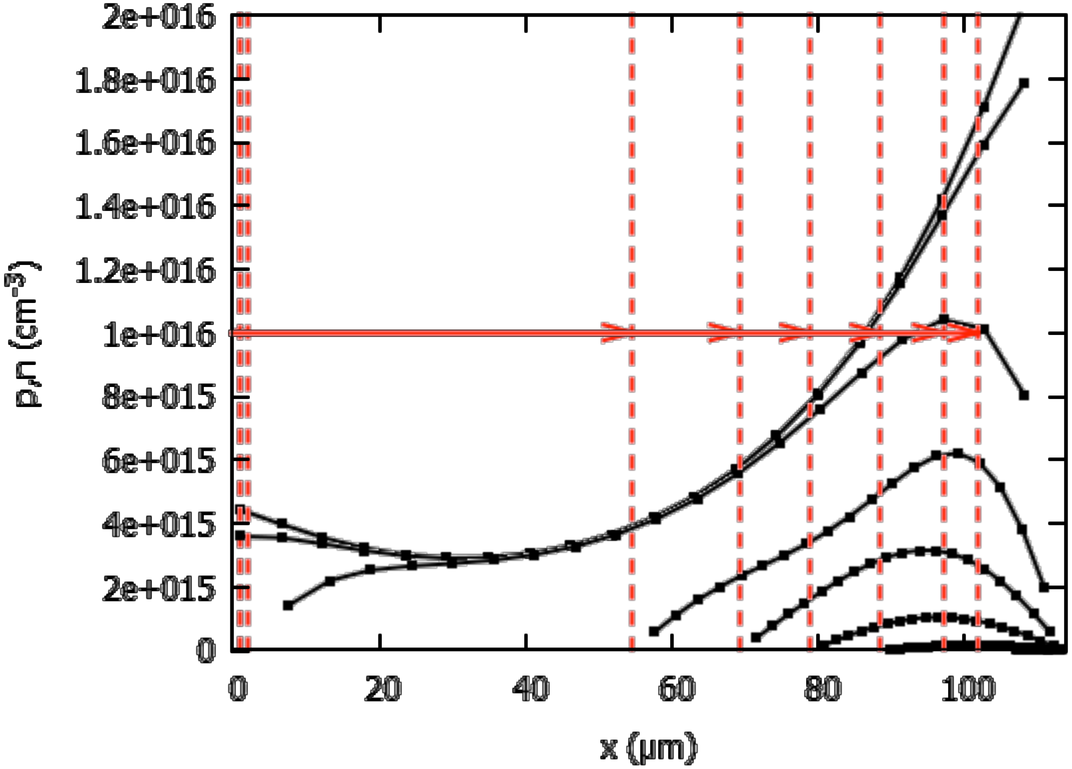


Plasma concentration in a diode during turn-off

Unique feature of a SIMetrix model

Compact modelling of power devices
Implementation of charge dynamics model in SPICE

For 20 discretization points



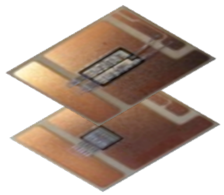
Plasma concentration in a diode during turn-off

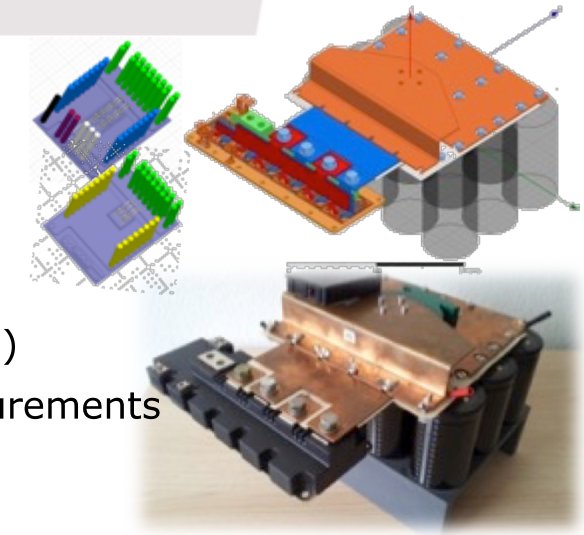
Unique feature of a SIMetrix model

Outline

Assessment of modelling precision
Work flow

› Calibration

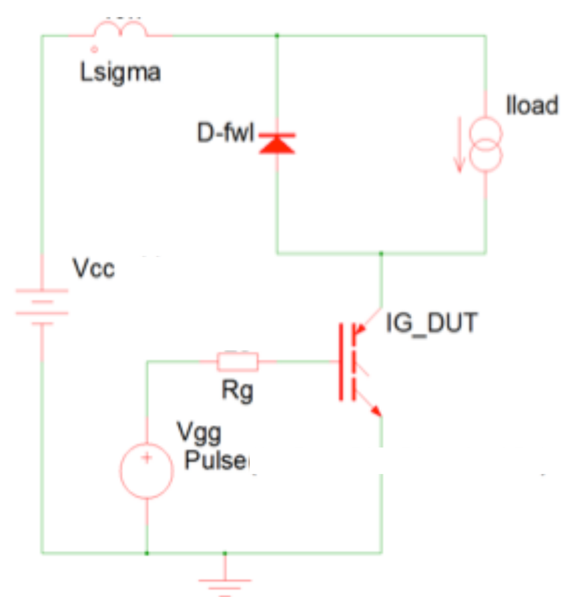




- TCAD and compact chip models are calibrated on measurements of single chips mounted on DCBs
- Parasitics are extracted for the module and the test setup directly from the CAD layout (no C, R @ DC and L @ 100MHz)
- Parasitics of the driver are fitted from characterization measurements

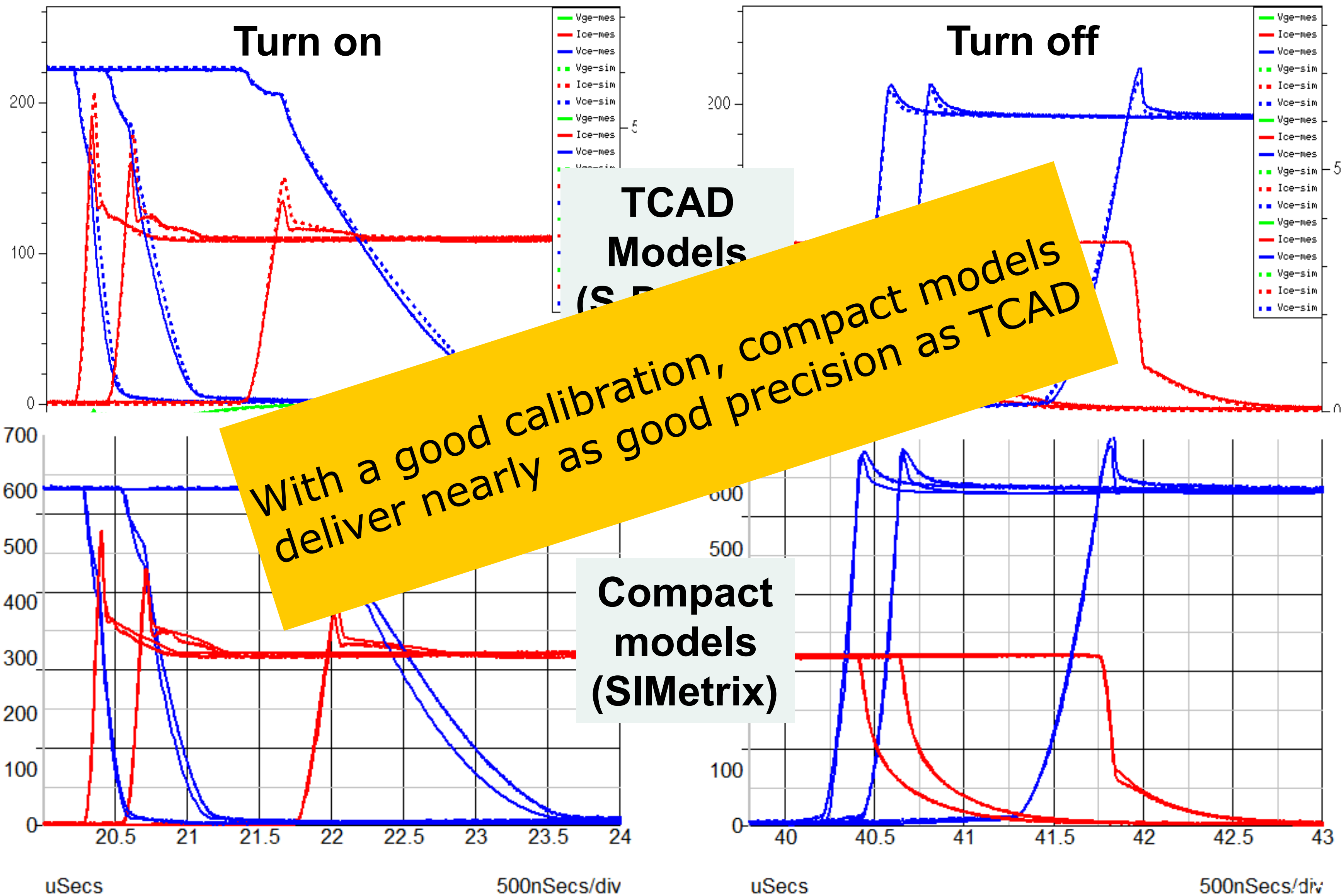
› Precision assessment

- DoE for dynamic characterization in test circuit varying R_g, V_{CC}, I_{Load}, T_j and L_σ
- Measurements and simulations for at least 24 switching conditions
- Mounting as single-chip and in module package
- Evaluation of IGBT turn on and off + diode reverse recovery
- For each switching conditions extraction of up to 68 switching parameters from simulated and measured curves
- Qualitative assessment: overlay of simulated and measured switching transients for different switching conditions
- Quantitative assessment: simulation error (deviation) of extracted parameters for single-chip and module mounting



Assessment of modelling precision

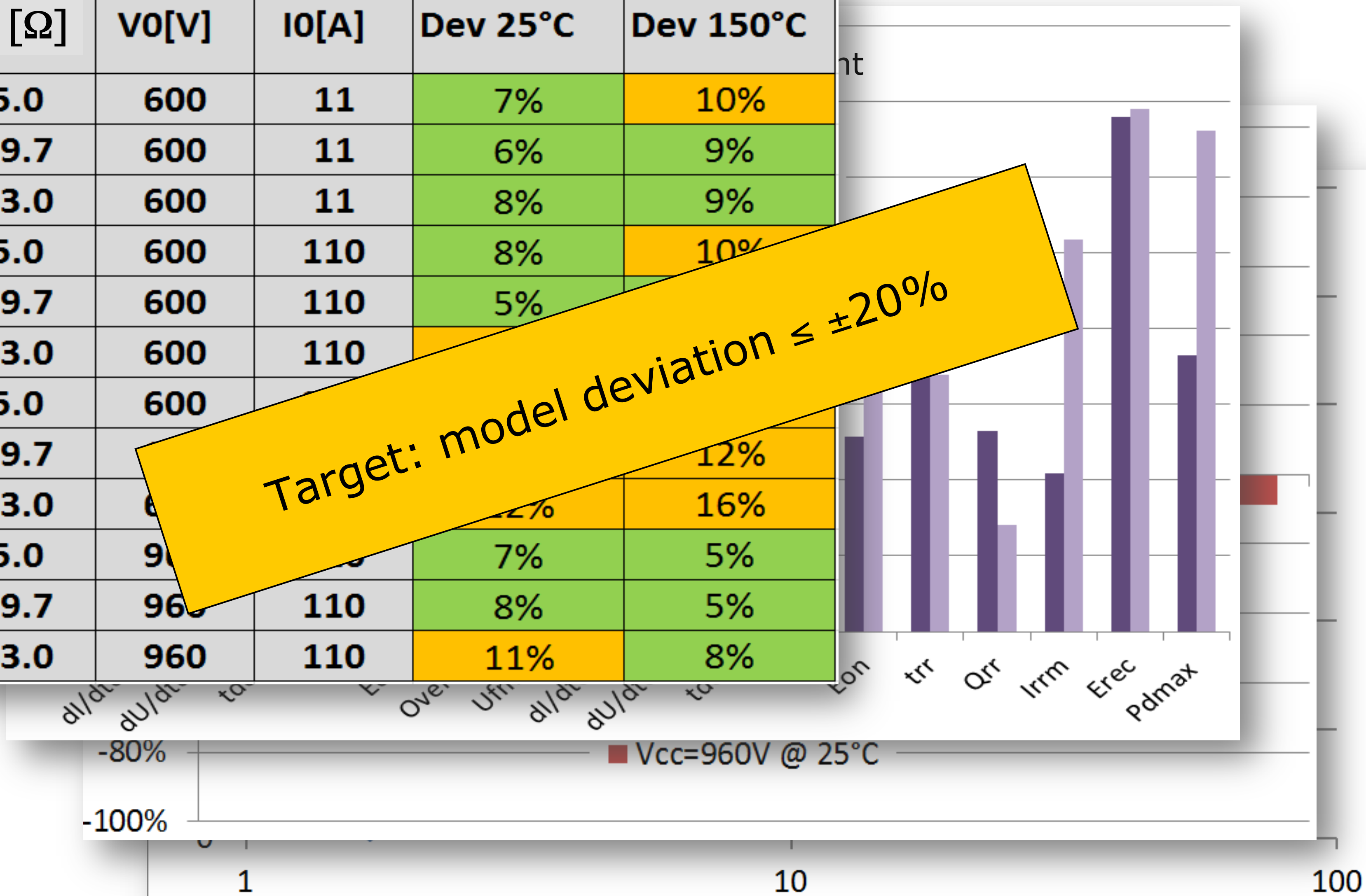
Switching curves (best-can-do calibration)



Assessment of modelling precision
Extracted dynamic parameters

Rg [Ω]	V0[V]	I0[A]	Dev 25°C	Dev 150°C
5.0	600	11	7%	10%
19.7	600	11	6%	9%
83.0	600	11	8%	9%
5.0	600	110	8%	10%
19.7	600	110	5%	[illegible]
83.0	600	110	[illegible]	[illegible]
5.0	600	[illegible]	[illegible]	[illegible]
19.7	[illegible]	[illegible]	[illegible]	12%
83.0	[illegible]	[illegible]	12%	16%
5.0	[illegible]	[illegible]	7%	5%
19.7	960	110	8%	5%
83.0	960	110	11%	8%

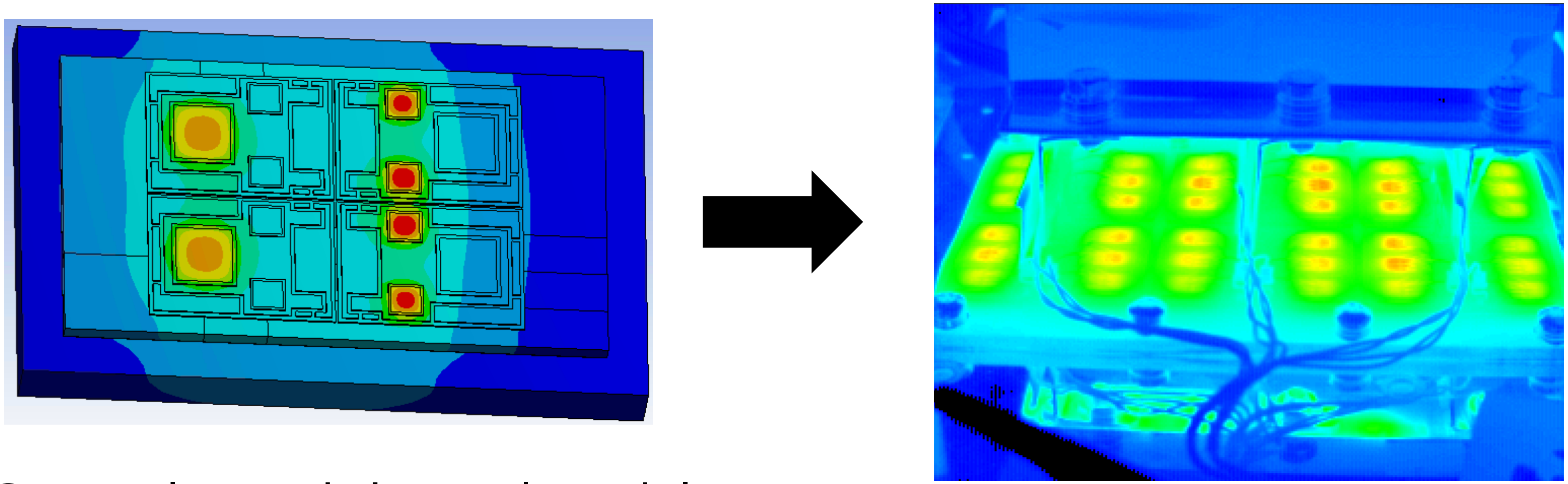
Target: model deviation ≤ ±20%



Outline

Electro-thermal co-simulation in SPICE

Motivation

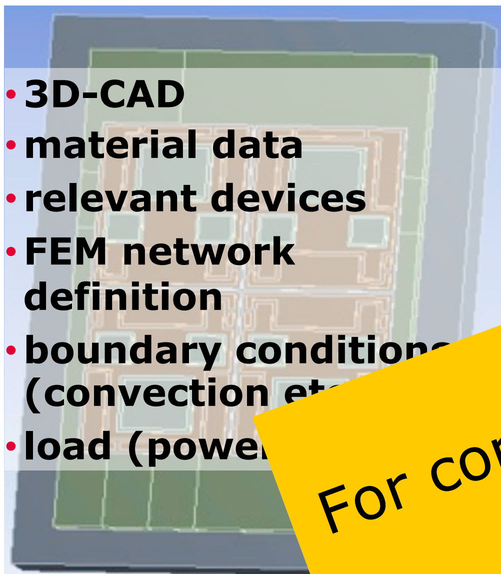


- Currently used thermal models:
  - Foster model (partial-fraction network, data sheet parameters)
  - Cauer model (continued-fraction network, physically correct)
  - Matlab model (direct combination of step responses from FEM analysis with power signal via convolution integral)
- Serious draw back: amount of RC elements when considering thermal couplings in complex modules
- Good to have:
  - thermal model that can be directly integrated in circuit simulation
  - Coupling with electrical model that considers loss distribution

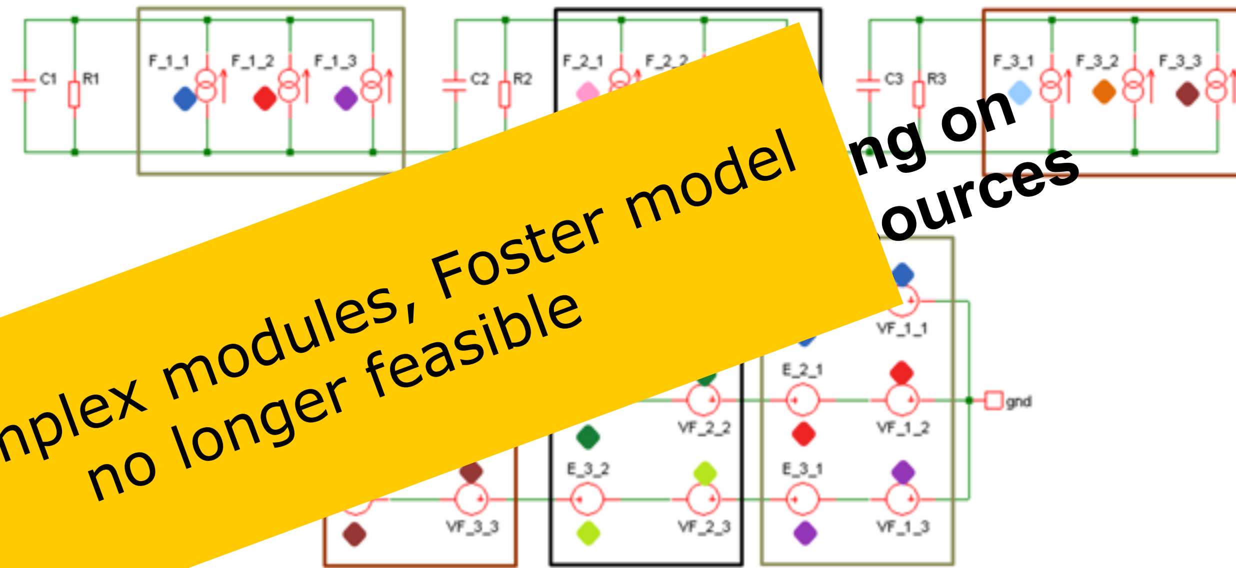
Electro-thermal co-simulation in SPICE

Thermal model generation with MOR tool for ANSYS

› Generates reduced thermal model without calculation of a temperature field.
  - MOR = **M**odel **O**rder **R**eduction (procedure)
  - ROM = **R**educed **O**rder **M**odel (result)



- **3D-CAD**
- **material data**
- **relevant devices**
- **FEM network definition**
- **boundary condition (convection et**
- **load (powe**



ng on
ources

For complex modules, Foster model no longer feasible

62mm m

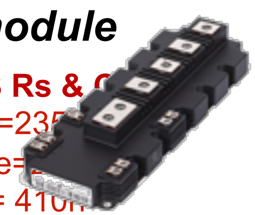
Foster model with 624 Rs & C
Fitting time=15
Working time=2
Total time = 29.2h

ROM for 180 dimensions with 6840 elements:
Working time=2.0h
Total time = 2.1h

Examples

PrimePack™3 module

Foster model with 9408 Rs & C
Fitting time=235
Working time=
Total time = 410h

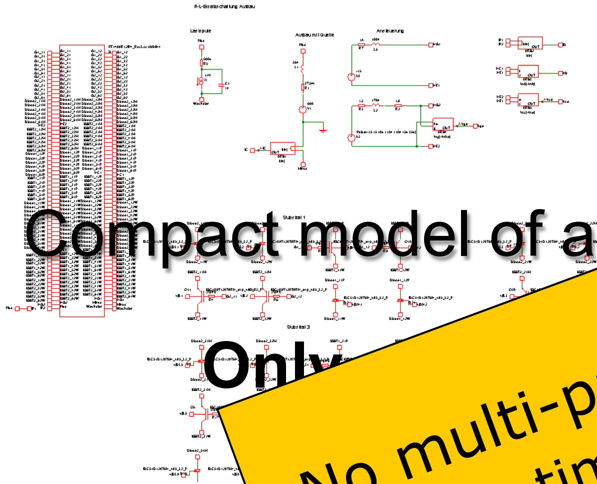


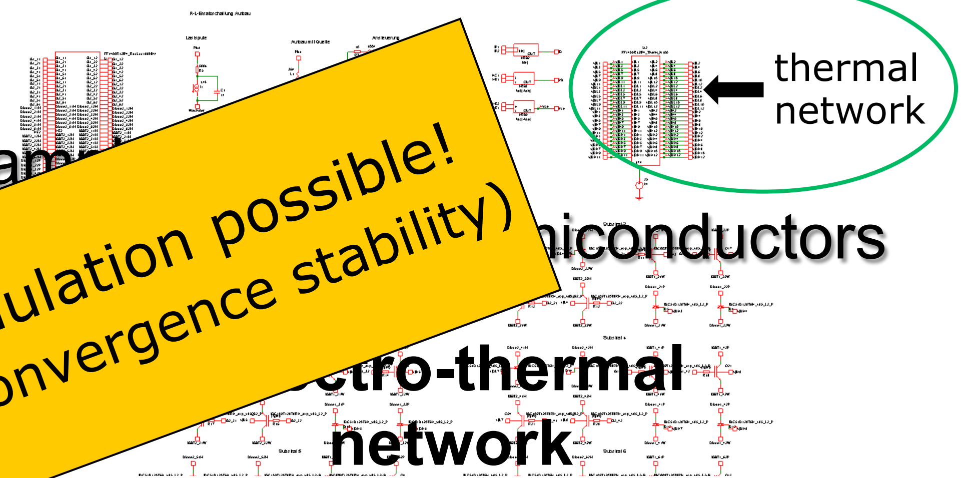
ROM for 1000 dimensions with 146k elements:
Working time=3h
Total time = 12h

Electro-thermal co-simulation in SPICE

Electro-thermal simulations with ROM for PP3

- Electro-thermal model in SIMetrix results from merging the thermal ROM and the electrical compact model of the PP3
(semiconductor models were modified for power calculation and thermal handling)





Exam

Compact model of a Pri miconductors

Only ctro-thermal network

No multi-pulse simulation possible!
(analysis time and convergence stability)

Transient powe the module
at t rature

Output
Transient temperature and power loss distribution in the module until thermal steady state reached

Transient multi-pulse simulation

Period: 35µs
Convergence fail after 48 pulses!
Estimated analysis time for 10ms: 37.8h
Estimated analysis time for 100s: 43y!

Period: 35µs
Convergence fail after 11 pulses!
Estimated analysis time for 10ms: 140.3h
Estimated analysis time for 100s: 160y

Electro-thermal co-simulation in SPICE
Approach

- Transient multi-pulse electro-thermal simulation: not viable because of analysis time and convergence stability
- Next approach: perform separated, but coupled iterative simulations with pure electrical and pure thermal model

  - simulate stationary temperature and power loss distribution in the module at thermal steady state in a DC/DC converter
  - simulate transient temperature and power loss distribution in the module during thermal ramp up with sinusoidal current load *(emulates inverter operation)*

Electro-thermal co-simulation in SPICE
Approach

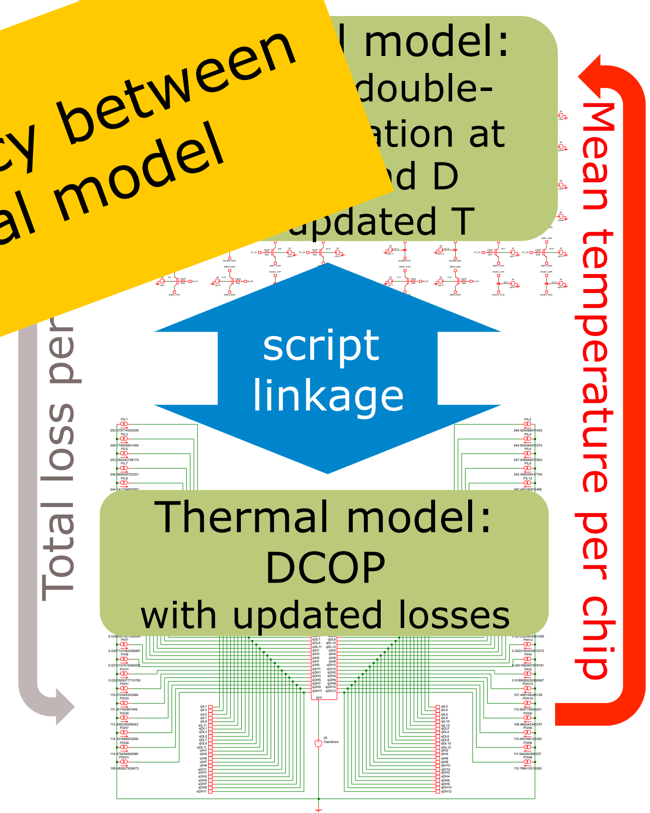
› Transient multi-pulse electro-thermal simulation: not viable because of analysis time and convergence stability

› Next approach: perform separated, but coupled iterative simulations with pure electrical and pure thermal model

- simulate stationary temperature an[d] loss distribution in the modul[e] steady state in a DC/D[C]

- simulate tran[…] power loss distributi[…] during thermal ramp […] sinusoidal current load *(emulates [in]verter operation)*

Iterations until consistency between electrical and thermal model

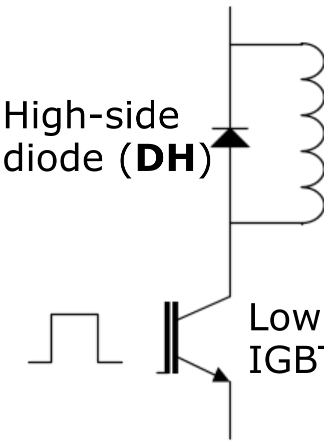


Electro-thermal co-simulation in SPICE
Example: PrimePack^{TM}3

Stationary pseudo electro-thermal simulation

- Circuit: buck converter, low-side IGBT is switched
- Design: converter layout calculation for T_{jmax}=150°C
- $T_{initial}$ = 25°C
- Convergence criterion < 0.05°C
- 10 iteration needed
- Total analysis time: 3.3h

Input Voltage	600	V
Blocking Voltage	1200	V
Output Voltage	300	V
Duty Cycle	0.54	
Switching Frequency	1500	Hz
Output Current	1240	A



- **Result:** mean temperature of each chip in good agreement with full FEM simulation

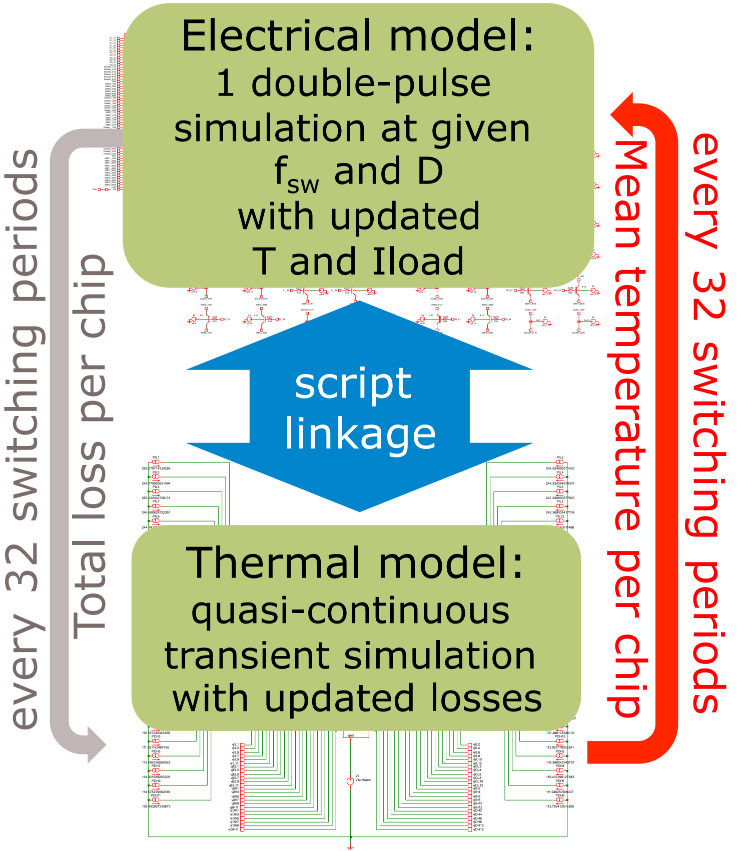
Electro-thermal co-simulation in SPICE
Approach

› Transient multi-pulse electro-thermal simulation: not viable because of analysis time and convergence stability

› Next approach: perform separated, but coupled iterative simulations with pure electrical and pure thermal model

- simulate stationary temperature and power loss distribution in the module at thermal steady state in a DC/DC converter

- simulate transient temperature and power loss distribution in the module during thermal ramp up with sinusoidal current load *(emulates inverter operation)*

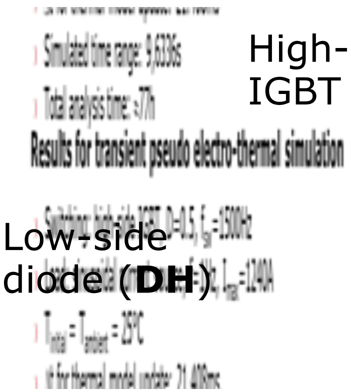


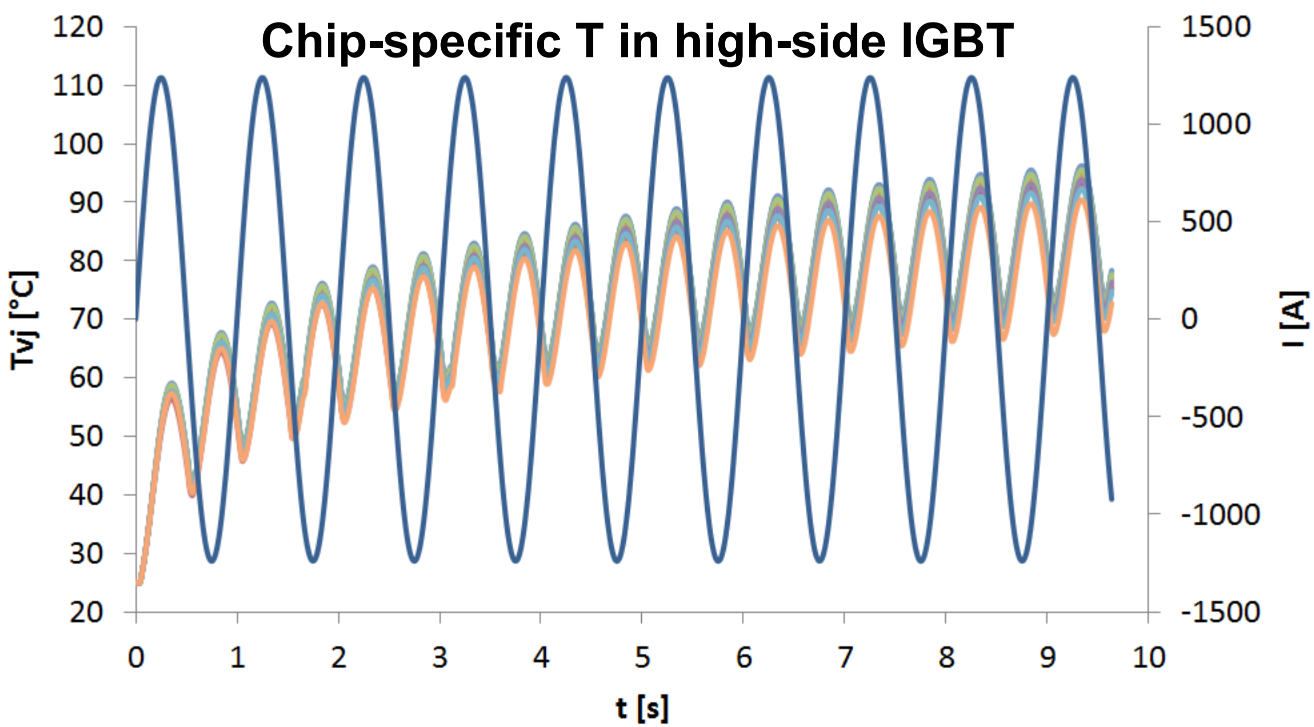
Electro-thermal co-simulation in SPICE

Example: PrimePack™3

Results for transient pseudo electro-thermal simulation

- Switching: high-side IGBT, D=0.5, f_{sw}=1500Hz
- Load: sinusoidal current source, f=1Hz, I_{max}=1240A
- $T_{initial}$ = $T_{ambient}$ = 25°C
- Δt for thermal model update: 21.408ms
- Simulated time range: 9,6336s
- Total analysis time: ? 77h





Outline

1 Introduction

2 Virtual Prototyping Approach

3 Compact modelling for power devices

4 Assessment of Model Precision

5 Electro-thermal co-simulation in SPICE

6 Summary and Outlook

Summary

- Virtual prototyping flow for device and package development
- Detailed evaluation of simulation precision
- Current distribution in modules for design optimization
- Investigation of impact of main FE and BE tolerances
- Simulation-based system-level models for thermal converter design
- Enhanced IGBT and diode compact models
- Electro-thermal co-simulation at circuit level

Outlook

Compact chip models:
Equivalent circuits → Verilog-A

Extraction of compact chip models from TCAD flow

Automated generation of compact chip models

Vision

Establish MOR technique to predict temp. distribution

Establish automated calibration routine

Extend VP to discrete IGBTs in evaluation boards

THANK YOU FOR YOUR ATTENTION

Part of your life. Part of tomorrow.