Device aging simulations enabling circuit optimizations

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8.11.2017 – MOS AK 13.3.2018
Aging – Critical Stress Conditions?
Funded by: BMBF and European Union Catrene Program 01/2015-12/2017

Motivation:
- Electronic systems in cars planes require high reliability
- New reliability aware design approaches and solutions are needed
- Resist targets: New approaches for resilient integrated systems

Resilience:
- The ability of a system or component to resist a certain load change by adapting its initial stable configuration to the new situation
RESIST Project Partners
Agenda

1. Worst Case Aging Models
2. Variability
3. BTI Recovery
4. Circuit Simulations
5. Outlook and Cooperation
Electrical stress generates charged traps

\[ V_T = 0.49 \text{ V} \quad T_{age} = 0 \text{ a} \]

\[ V_T = 0.65 \text{ V} \quad T_{age} = 1 \text{ a} \]

\[ V_T = 0.55 \text{ V} \quad T_{age} = 2 \text{ a} \]

A. Asenov et. al., *Simulation of Intrinsic Parameter Fluctuations in Decananometer and Nanometer-Scale MOSFETs*, IEEE Transactions on Electron Devices 50(9), 2003
NMOS Hot Carrier Injection (HCI) Effect

- $E_{max}$ at drain corner causes hot carrier generation
- Hot carriers cause $I_{sub}$, $I_{gate}$ and oxide damages

Degradation $f(T,V_{DS},V_{gs})$
- Parametric shift
  - Increase of $V_{th}$
  - Decrease of $g_m$
  - Increase of $I_{off}$
  - Decrease of $I_{dsat}$

Impact Ionization

Oxide Damage

$S$ $G$ $D$

P-well

$\text{n}^+$ $\text{n}^+$ $\text{n}^+$ $\text{P}$-$\text{well}$
Negative Bias Temperature Instability (NBTI) Effect
- Hydrogen-silicon bond (Si-H) is broken
- Hydrogen is trapped into the oxide $\rightarrow$ interface trap

Positive Bias Temperature Instability (PBTI) Effect

Degradation $f(T,V_{GS})$
Recovers

Parametric shift
- Increase of $V_{th}$
- Decrease of $g_m$
- Increase of $I_{off}$
- Decrease of $I_{dsat}$
Worst-Case Aging Models – Main Features 1

**BTI - Basic Set of Generic Equations for \( \Delta V_{th} \) and \( \Delta I/I_o \) Contributions**

\[
(BTI) \quad < L(V_{gs}) \cdot C \cdot e^{\left\{ \frac{B_V}{\pm |V_{gs}|} + \frac{-E_a}{(k_B \cdot T_{op})} + \frac{B_L}{L_{des}} \right\}} > t \cdot (t_{op})^n
\]

**HCI - Basic Set of Generic Equations for \( \Delta V_{th} \) and \( \Delta I/I_o \) Contributions**

\[
(HCI) \quad < L(V_{gs}, V_{ds}) \cdot C \cdot e^{\left\{ \frac{B_V}{\pm |V_{ds}|} + \frac{-E_a}{(k_B \cdot T_{op})} + \frac{B_L}{L_{des}} \right\}} \cdot A(|V_{gs}|) > t \cdot (t_{op})^n
\]

- \( \pm \) depends on device type: + for nmos, - for pmos
- \( V_{gs} \) and \( V_{ds} \) are time dependent transistor terminal voltages
- Boltzmann term \( \exp\left\{ \frac{-E_a}{(k_B \cdot T_{op})} \right\} \) for temperature dependency
- \( (t_{op})^n \) describes extrapolation to final long-term aging time, typically \( t_{op} = 10y \)
- \(<...>_t \) is the weighted summation over simulated stress time
- \( L(\ldots) \) are limiting functions required for numerical reasons
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Distribution of the threshold voltage after BTI

Distribution of $V_{th}$ after NBTI stress
$\rightarrow$ convolution of:
- Distribution of the virgin devices
- Distribution of the NBTI degradation

Impact of BTI Variability


Standard deviation $s$ of $V_{th,lin}$ of the transistors with different areas (nm$^2$) before and after stress

Pelgrom plot of the standard deviations $s$ of the stress induced $V_{th,lin}$ and $V_{th,sat}$ shift. Like the $s$ of zero hour parameters also the $s$ of the $V_{th}$ shift is proportional to $\sim 1/\sqrt{w \times l}$. 

Pelgrom-Plot

NBTI: $V_{GS} = -2.0V$; $T=125^\circ C$; 14h
Distributions of the threshold voltage after recovery up to 43 weeks at T=125°C. Both the $V_{th}$ values and the variability recover in direction of the virgin values (rightmost curve).

Present status of circuit aging simulations

Neglection of BTI induced variability due to:
- 0h variability dominates variability
- BTI induced variability recovers together with the BTI degradation
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Can we just neglect Recovery of BTI?

'S-Curve': BTI degradation as a function of the duty-cycle of a rectangular signal (f=100 kHz) applied to the gate for 10ks.

Neglecting recovery is more than 2 times over-estimating the degradation after BTI for a duty cycle of 50%
Integrating Recovery into Circuit Simulations

Why it is so complicated to consider BTI recovery for circuit simulations?

- Recovery depends on the full device history
  - real-time simulations necessary
  - No simple extrapolation possible
- Physical models: Charging/discharging of every single trap
  - Very time-consuming, huge calculation effort
- Simplifications: E.g. Fraunhofer Gesellschaft approach
  - But: Still time-consuming and high measurement effort
- New approach developed: Publication will follow soon
Physics-based Compact Modeling of NBTI for Analog and Digital Circuit Design


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Fig. 4: MSM experiments with analog stress patterns. Left: During the MSM stress phase we periodically apply one of the four stress patterns: digital AC, sine, sawtooth, inverse sawtooth (a to d). The stress voltage oscillates between the values $V_i \leq -V_{p,s}(t) \leq V_h$. Right (three plots): The MSM setup uses a sequence of four stress intervals of duration $10^{-2}$ s, $10^{-1}$ s, $10^1$ s and $10^2$ s (bottom-up in the plots) and traces the respective recovery curves. We compare experimental data (symbols) to TCAD results (thick dashes) and to compact model results (solid line). Due to numerical complexity, TCAD data so far is only available for the two smaller stress times. The difference between TCAD and compact model results is often hardly noticeable. Most importantly, the theoretical predictions and experimental measurements are in good agreement. The consistency of experimental and compact model data at large stress times validates the compact model’s extrapolation method to large stress times also from a practical point of view. The present setup applies a stress frequency of 2kHz, a temperature of 125°C and stress voltages between $V_i = 0.5V$ and $V_h = 2.8V$.

Fig. 5: Threshold voltage shift during analog stress. We compare TCAD (dashed line) to compact model (solid line) results on $\Delta V_{th}(t)$ during the first five periods of the stress phase. For all four stress patterns, both models are in excellent agreement. The simulations use a stress frequency of 500Hz, a temperature of 125°C and voltage values $V_i = 0.5V$ and $V_h = 2.8V$. 

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2018-03-13 restricted
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Device Aging Simulation – Design Flow

Device Aging Simulation – Design Flow Building Blocks

Multi-step Spice simulation sequence

1. Fresh Simulation
2. Stress Simulation
3. Aged Simulation
deploying

- A Spice simulation engine
- Add-on worst-case aging models
- assertions for stress integration
- alter concept for instance specific
- Avenue/ADE-XL test sequence as flow control engines
Worst-Case/Realistic Stress Conditions

Main Impact Factors
• Aging Model Dependencies (VDS, VGS, Temperature)
• Analog Circuit Modes (Circuit Duty Cycles, Sleep Modes, Start-up Phase)

Temperature Implications
• local temperature increase
• mixed temperature stress profiles
• worst-case temperature condition for single device dependent on aging effect (BTI, HCI) and device type, but circuit contains always a mixture

Stress Scenario Discussion
• worst-case vs. realistic stress pattern
• suppression of start-up simulation phases
• handling of complex multi-circuit mode stress pattern
For the NOR ringo, HCS should play a less dominant role, than for the IV due to the exponential drain voltage dependence.
Results: Inverter Ringo, T=175°C, Vdd=2.4V

Frequency recorded during stress

Vstress=2.4V
T=175°C

Sim: HCS+BTI without recovery
Sim: HCS+BTI with recovery
Sim: BTI with recovery
Measurement data (10 chips)

HCS and BTI contribute both approx. equally.
Outlook & cooperation

› Efficient usable worst case models were developed

› Variability is currently neglected (0h hour variability has been shown to be bigger than aging-induced variability)

› Recovery is no longer neglected – Publication will follow soon

› Relevant circuit examples (Ring- and Relaxation-Oscillators) are further studied
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