



Extraction of a Scalable Electrical Model for a HV (600/800 V) MOS Transistor

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- **Introduction**
- **HV MOS Transistor description**
- **Model extraction strategy description**
- **Results**
- **Conclusions**

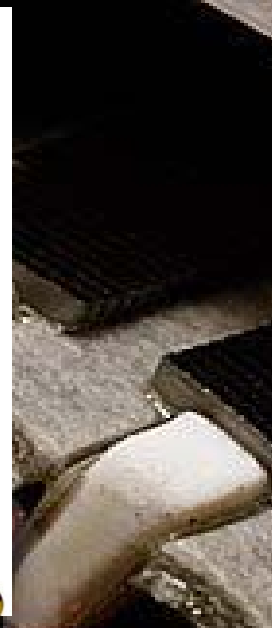
- **Introduction**

- ┌ HV MOS Transistor description
- ┌ Model extraction strategy description
- ┌ Results
- ┌ Conclusions

- 600V/800V MOS are commonly present in several applications of our daily life:
 - Low consumption bulbs
 - Devices connected to the power line which use:
 - Switching regulators
 - DC/DC converters
 - Motor drivers
 - Automotive
 - Etc...



Electric Motors & Motor Drivers



Automotive Applications



- **Car electromechanical systems**

- Fuel pump
- Water pump
- Air conditioning
- Windows



- **Engine of Electric Car**

- European Funded Project E³CAR

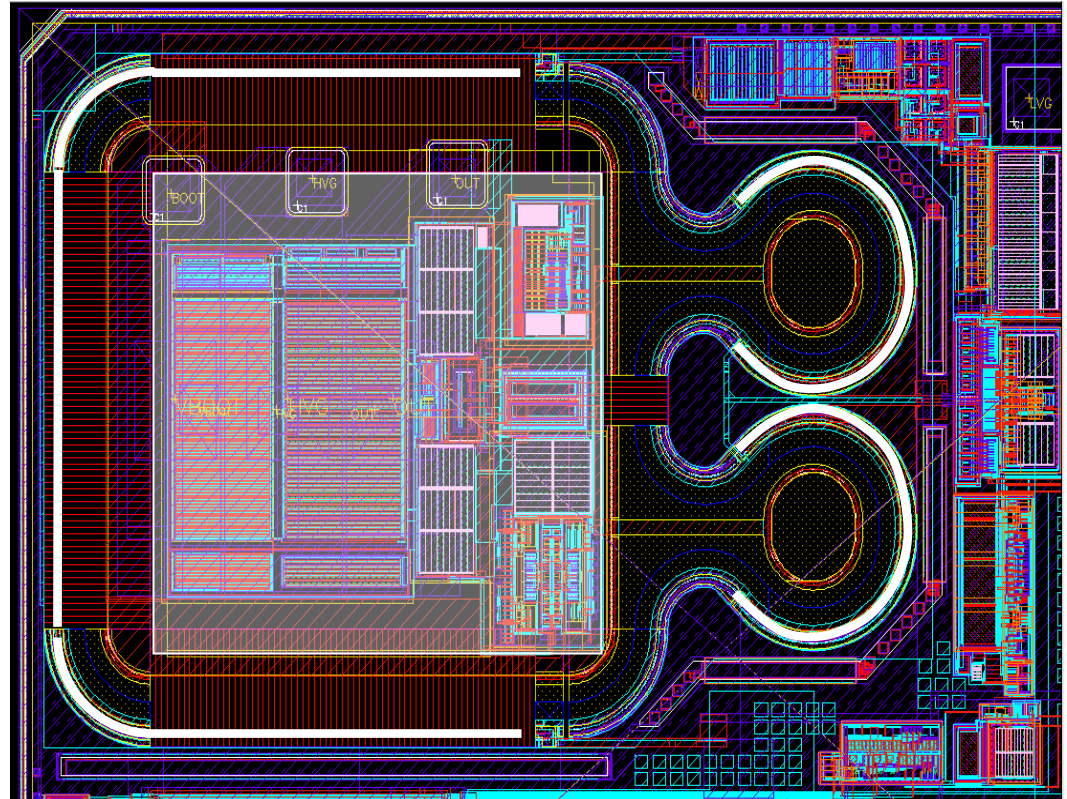


- ┆ Introduction
- **HV MOS Transistor description**
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- ┆ Results
- ┆ Conclusions

■ Level Shifter

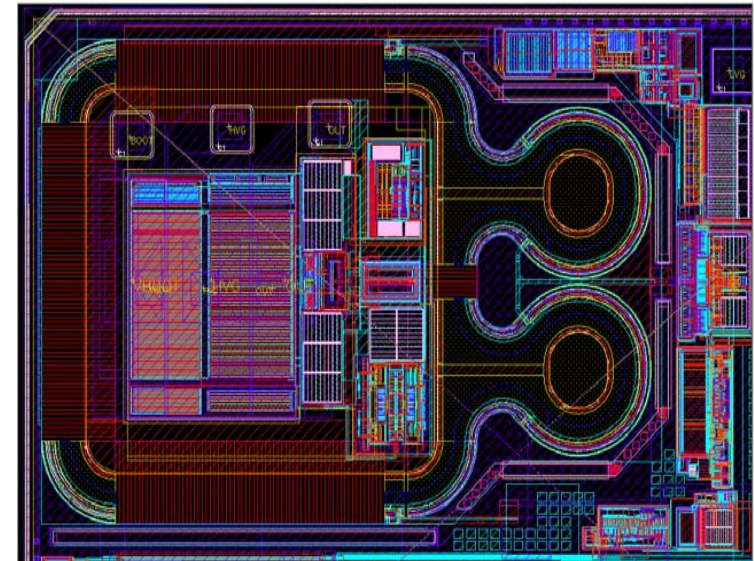
(*Mickey Mouse*):

- *Ears* are dedicated MOS used to bring in/out electrical signals
 - Its perimeter is also an active device
 - Isolated pocket which can contain low/medium voltage devices
-
- Realized in a $0.35\mu\text{m}$ smart power technology, BCD6SOFFLINE, able to integrate 3.3V/5V CMOS, BJTs, passives with MV MOS and 600/800 V MOS.



Model Purpose

- Since the perimeter transistor of the floating pocket is used to separate high voltage world from low voltage one, its shape is not defined *a priori*, but it is built up to contain low voltage devices

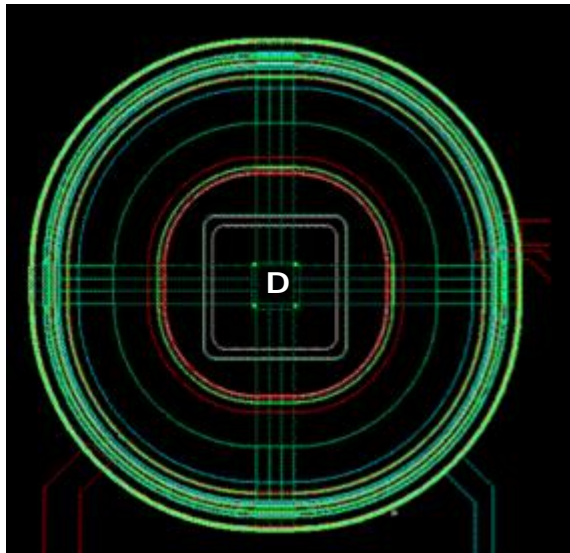


■ GOAL:

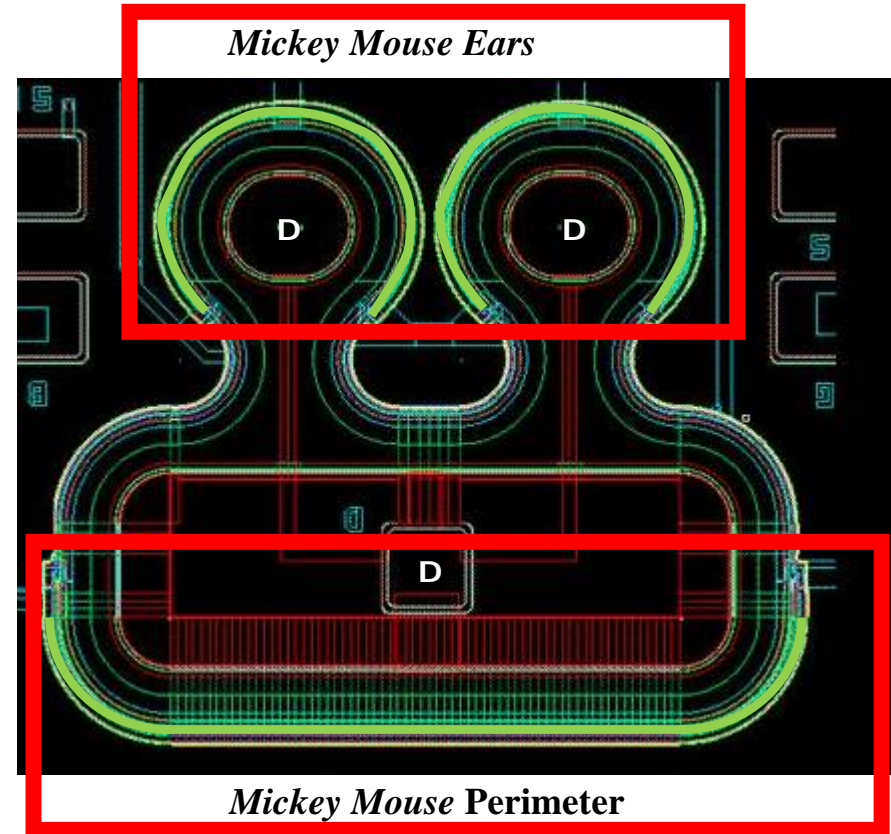
- Extraction of fully scalable models, able to take into account:

- Linear width
 - Number of curves
 - Number of *Ears*
- } To describe perimeter devices behavior
 → To describe the *Ear* electrical behavior

Available Devices for Model Extraction



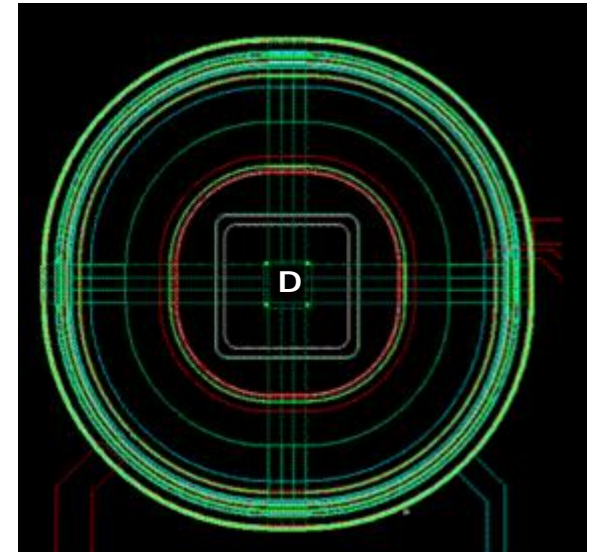
Round MOS



Step 1. Round MOS Modeling:

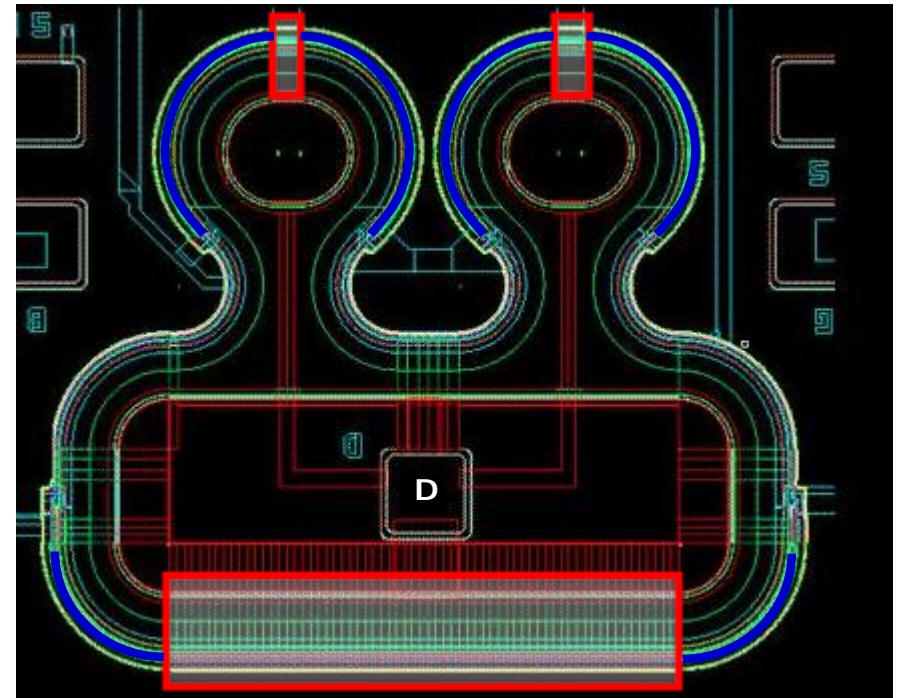
- $W \approx 1.5\text{mm}$

- Extraction of Round MOS model:
 - Intrinsic MOS, Rdrift, parasitic elements
- Extracted parameters have been adopted as initial values for subsequent models



Step 2. Doubling intrinsic MOS

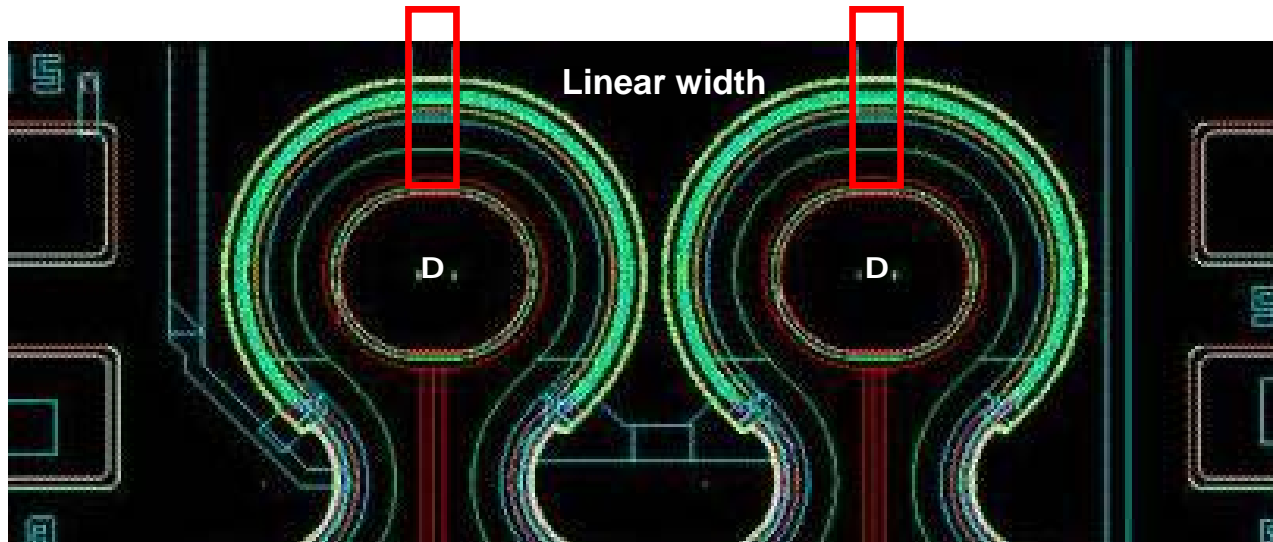
- Insertion of 2 MOS into the model card:
 1. To describe straight transistors
Parameter is linear width
 2. To describe curved MOS
Parameter is number of curves
(a curve has a fixed curvilinear width)



Linear width

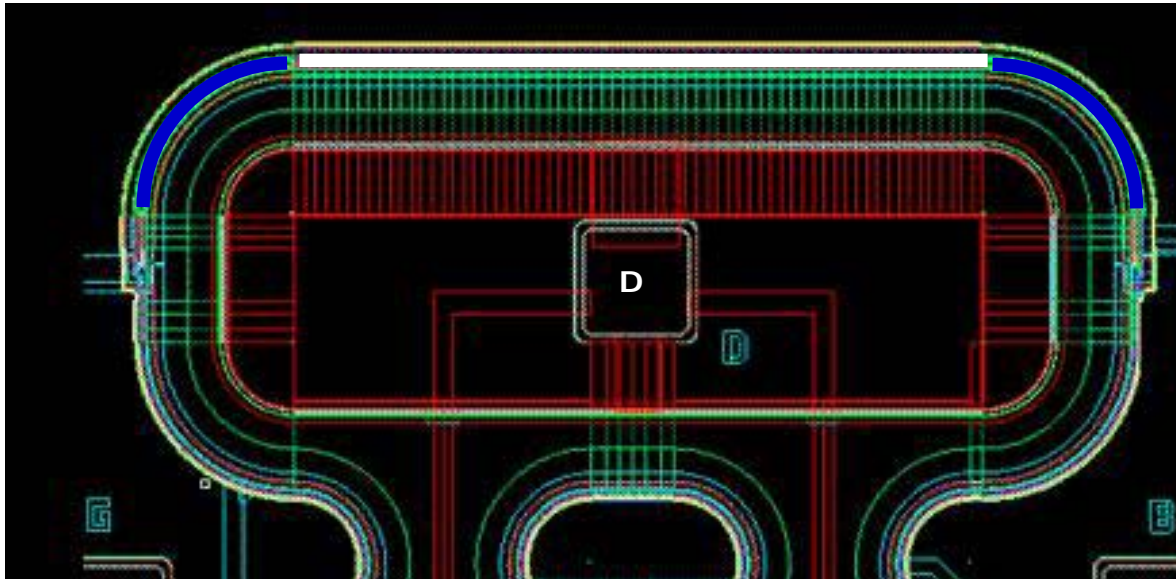
Curvilinear width

Step 3. *Ears* Modeling



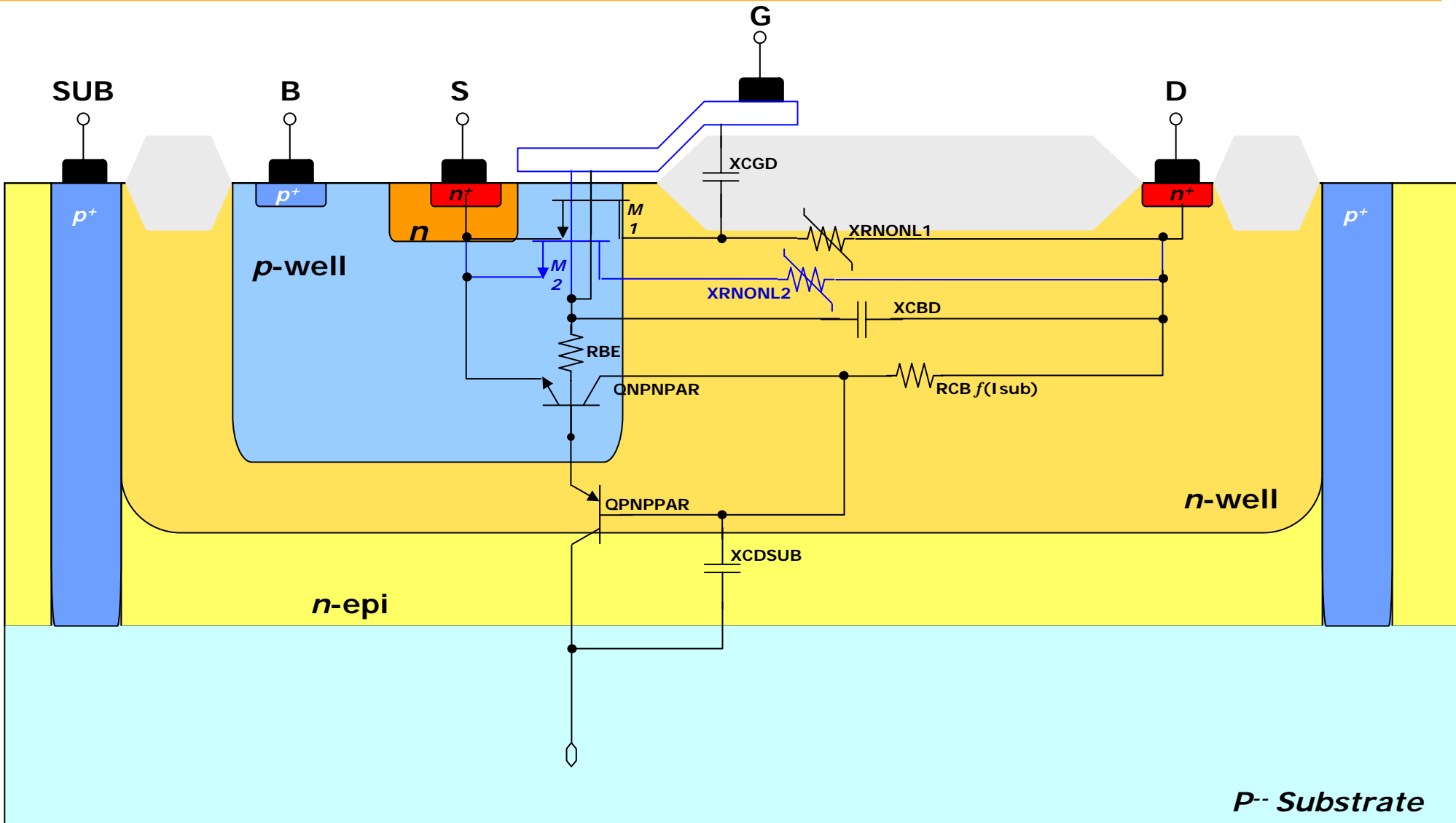
- Extraction and optimization of intrinsic MOS for curvilinear width
 - Number of curve (NC) = 6
 - Linear width negligible

Step 4. *Mickey Mouse* perimeter modeling



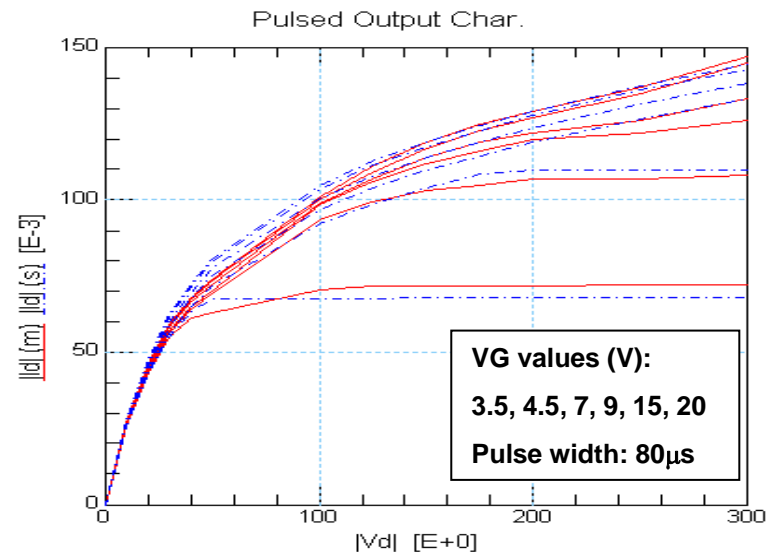
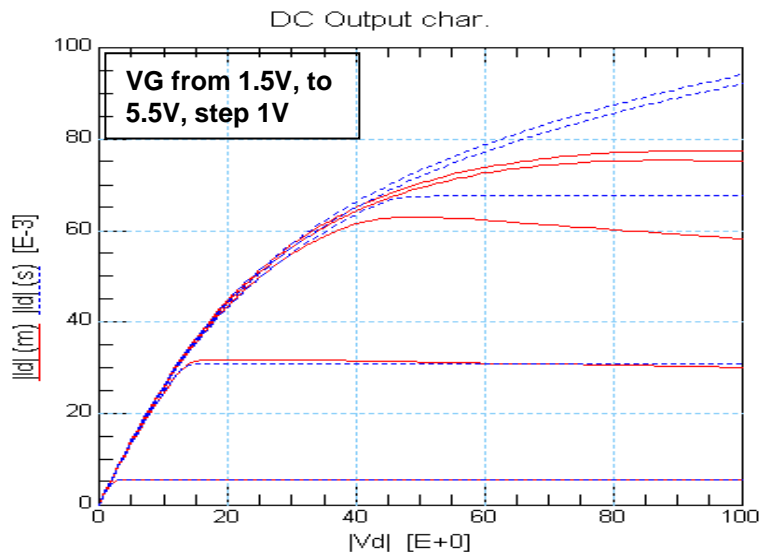
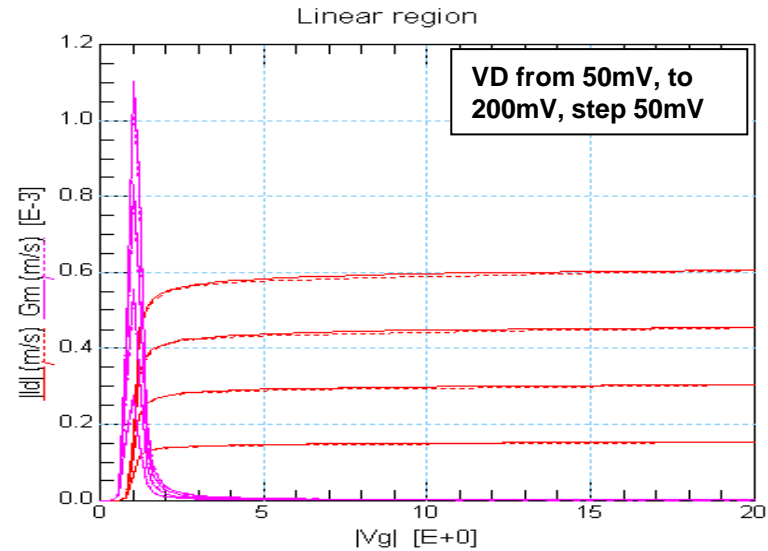
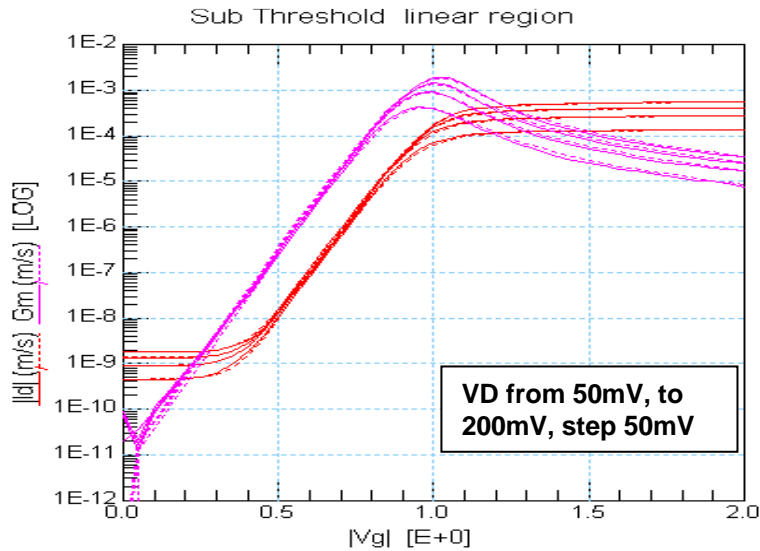
- Extraction and optimization of intrinsic MOS for straight MOS and ΔW
 - Number of curve (NC) = 2
 - Very large linear width

Cross Section



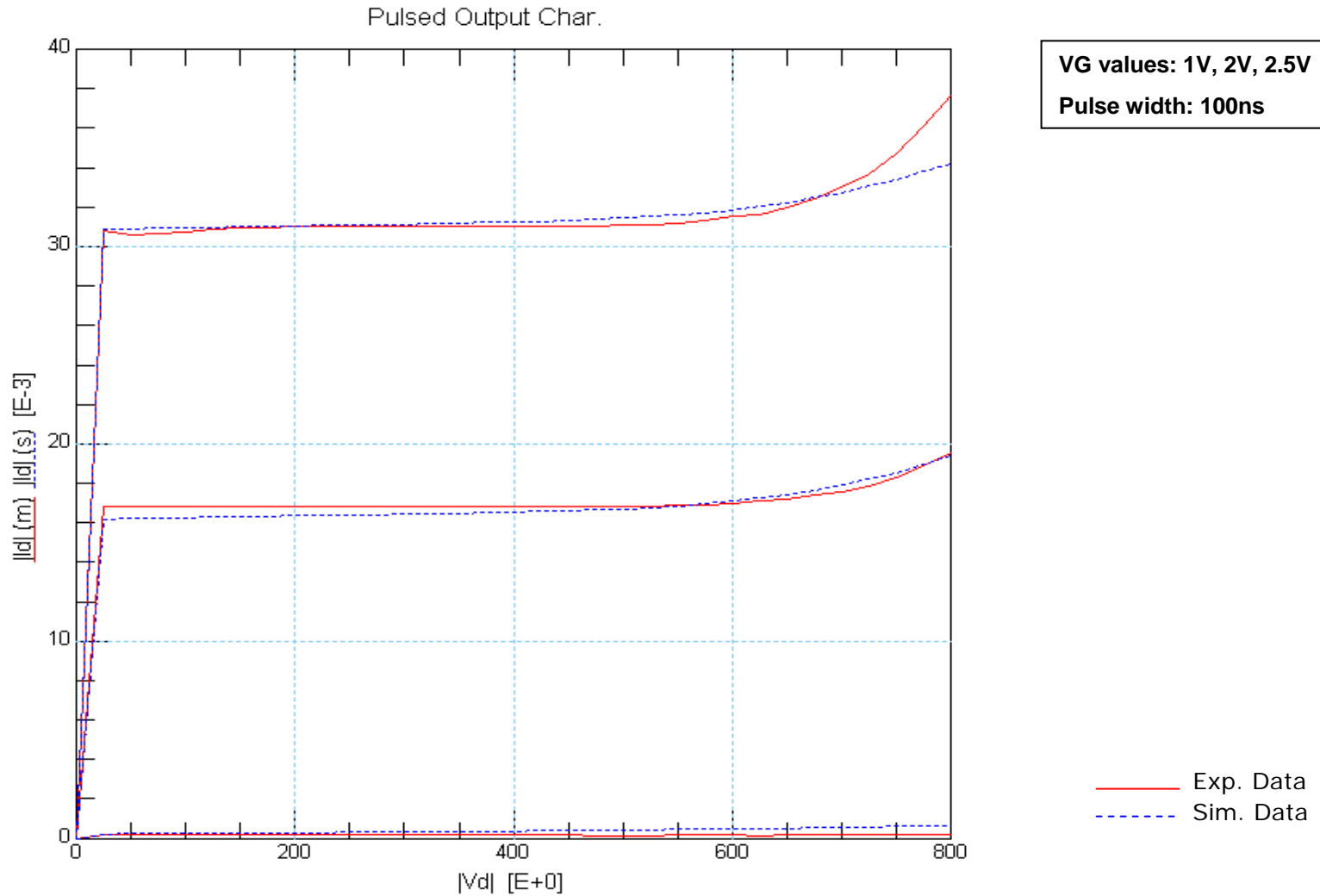
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Round MOS Model Accuracy @ 25°C

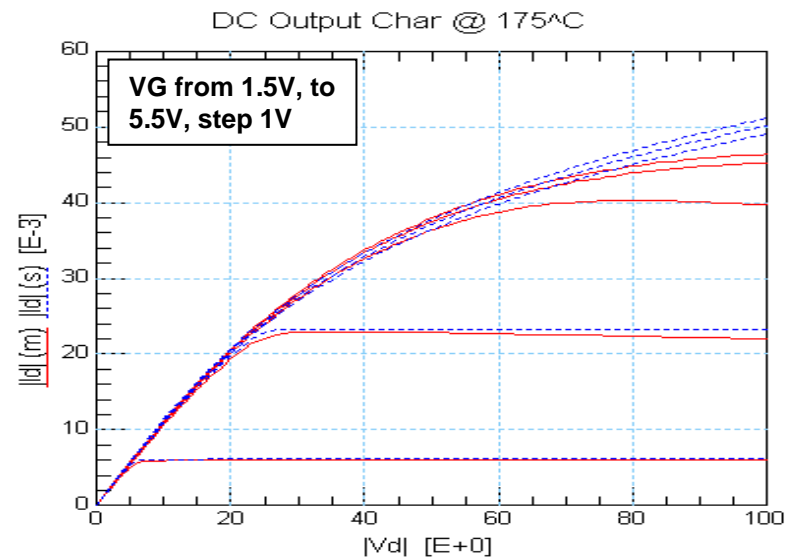
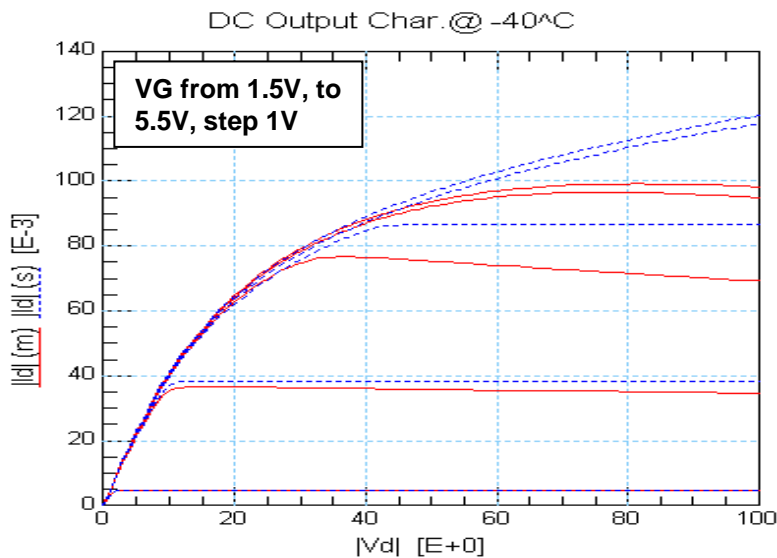
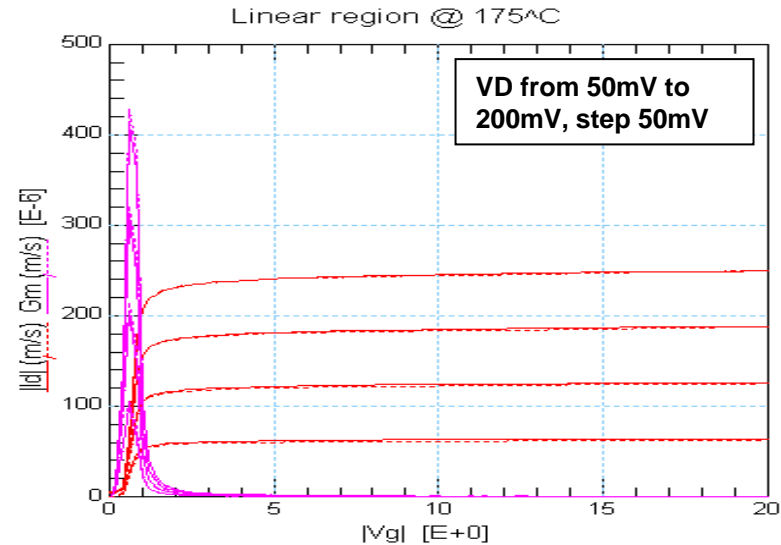
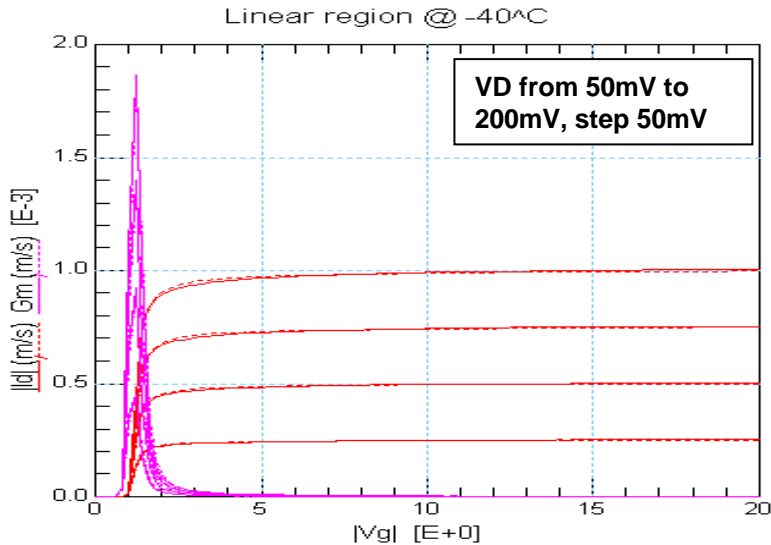


— Exp. Data
- - - Sim. Data

Round MOS Model Accuracy @ High Voltage

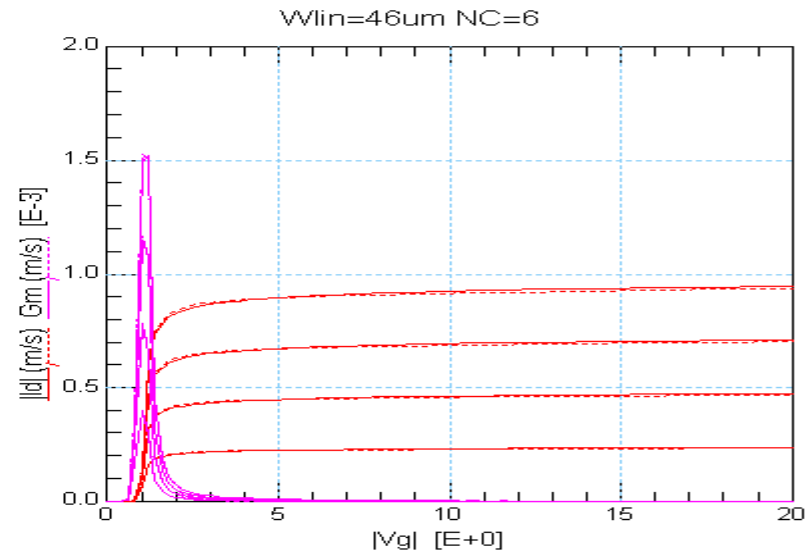
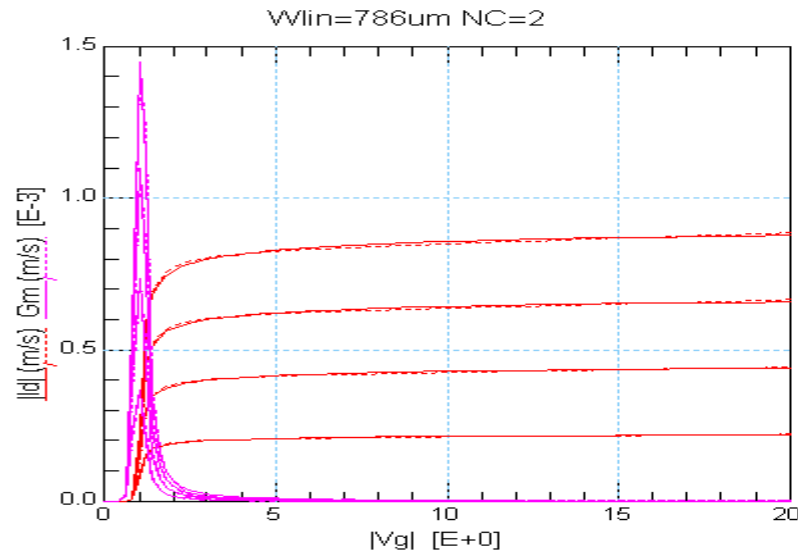


Round MOS Model Accuracy vs Temperature

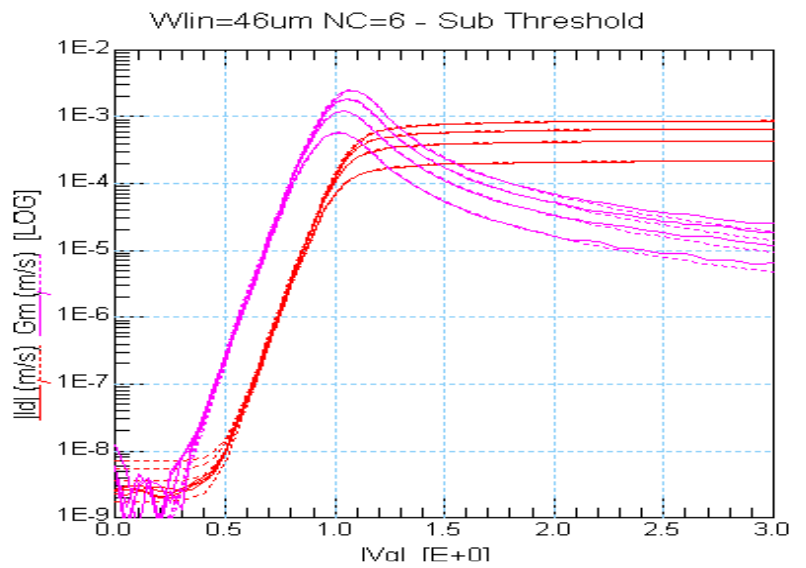
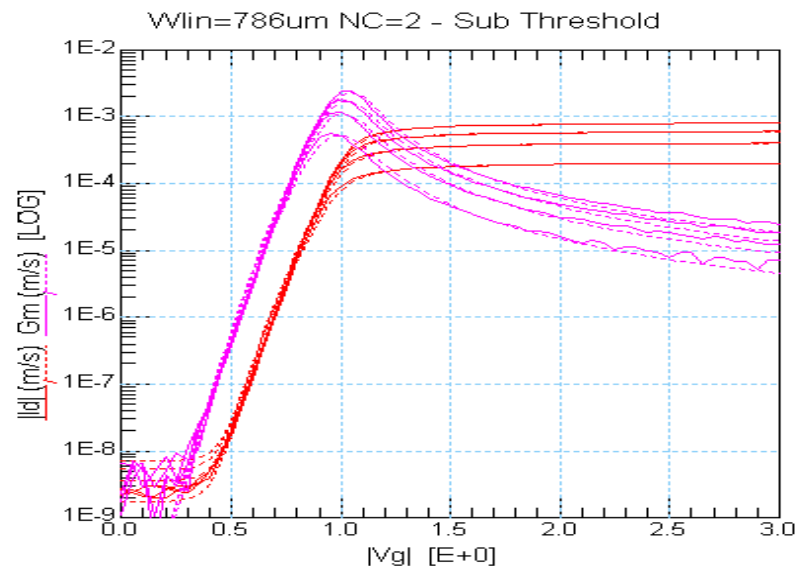


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Mickey Mouse Model Scalability – linear region

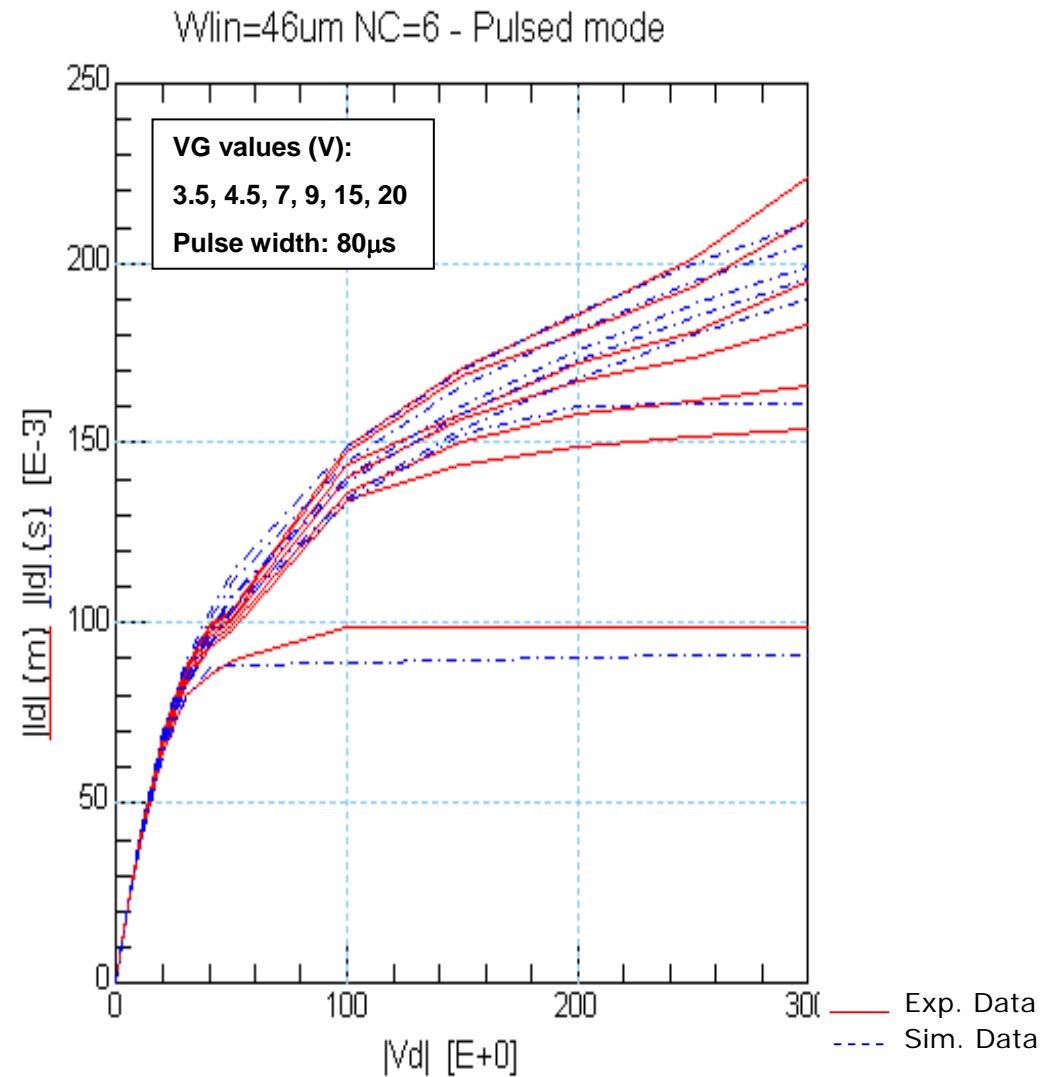
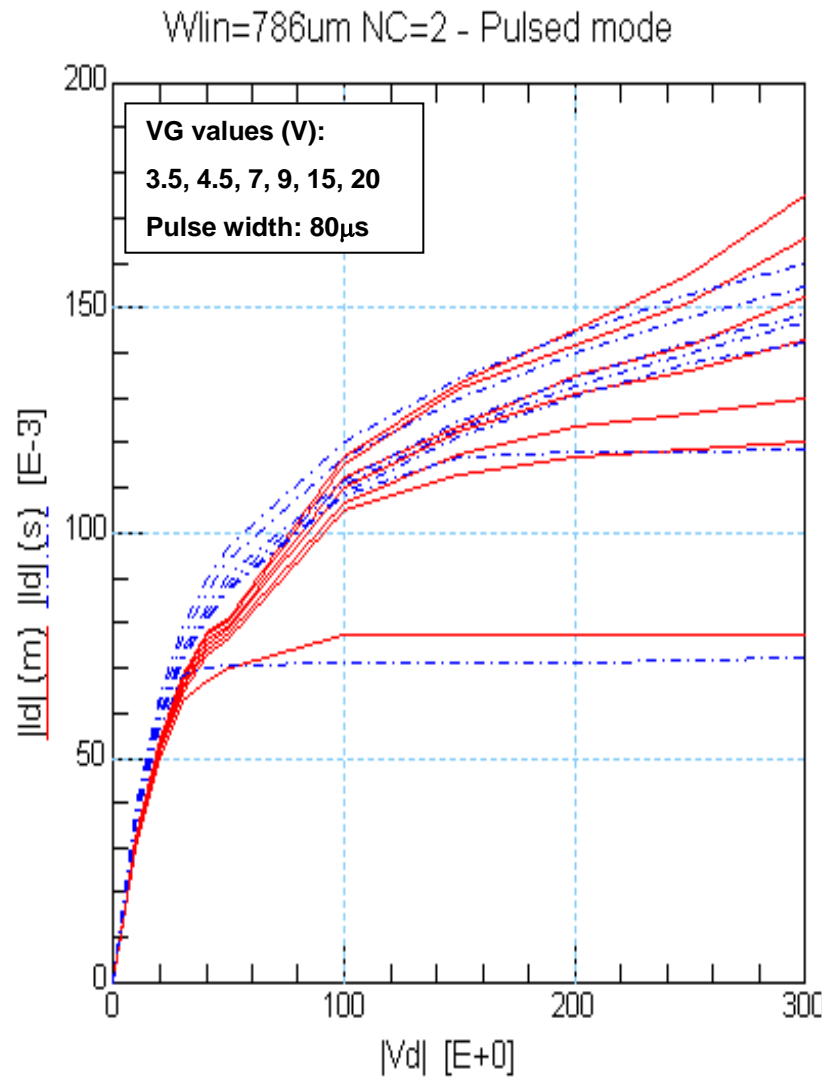


VD from 50mV to 200mV, step 50mV

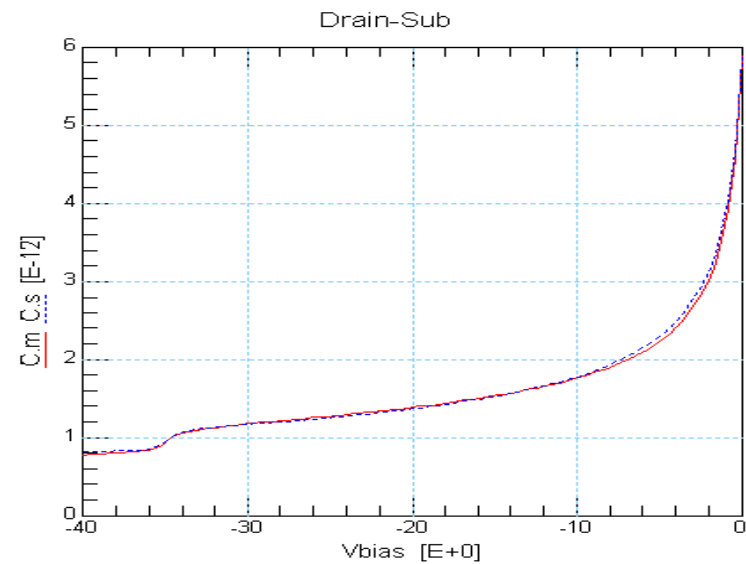
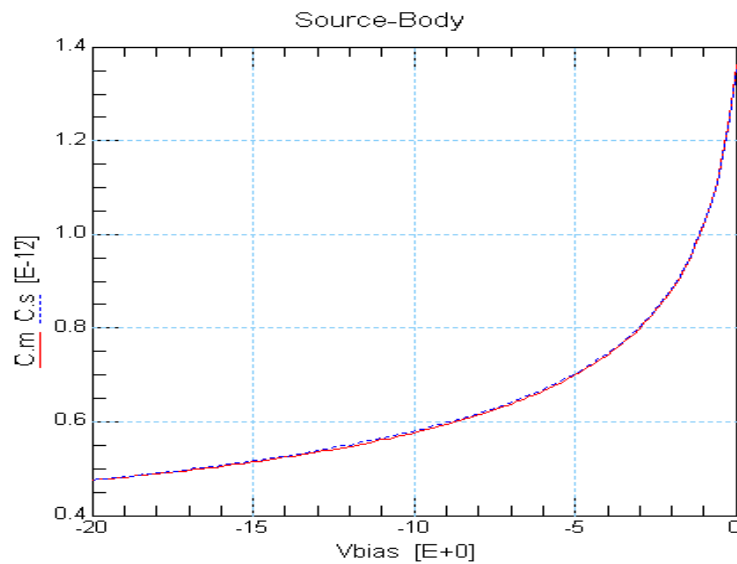
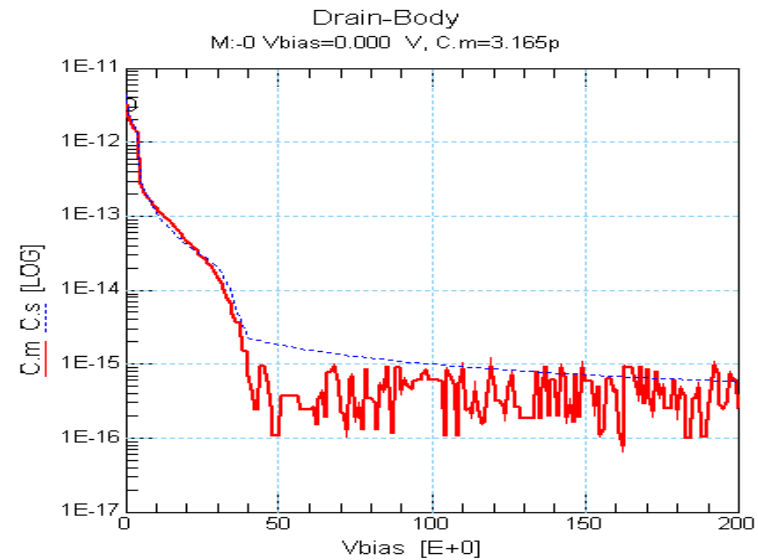
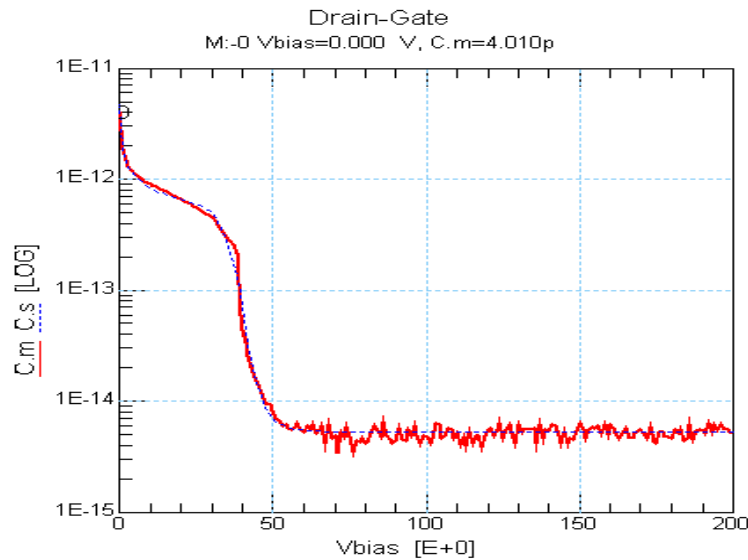


— Exp. Data
- - - Sim. Data

Mickey Mouse Model Scalability – output char.



Parasitic Capacitances



— Exp. Data
- - - Sim. Data

Gate-Drain Capacitance Affected by Resurf

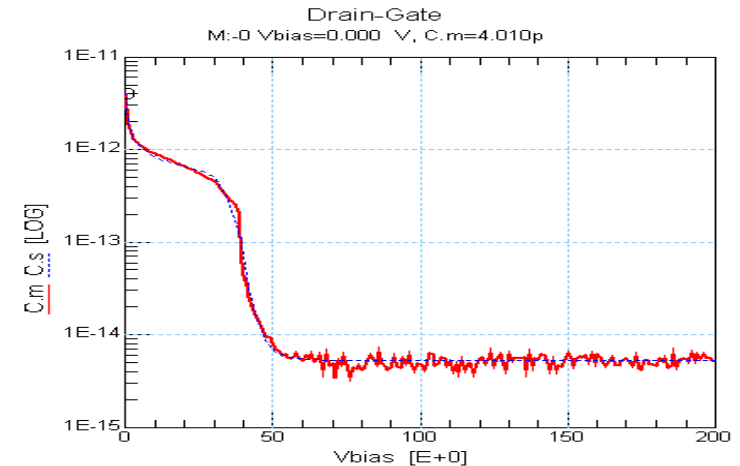


$$C_{DG} = C_{DGL} \cdot f + C_{DGH} \cdot (1 - f) + C_{par}$$

$$C_{DGL} = \frac{C_1}{\left\{ 1 + K1 \cdot \left[well_sgn \cdot x + 0.5 \cdot \left(-well_sgn \cdot x - VFB1 + \sqrt{(well_sgn \cdot x + VFB1)^2 + EPS1^2} \right) \right] \right\}^{MJK1}}$$

$$C_{DGH} = \frac{C_2}{\left\{ 1 + K2 \cdot \left[well_sgn \cdot x + 0.5 \cdot \left(-well_sgn \cdot x - VFB2 + \sqrt{(well_sgn \cdot x + VFB2)^2 + EPS2^2} \right) \right] \right\}^{MJK2}}$$

$$f = 0.5 \cdot \left[1 - \frac{well_sgn \cdot x - VSTEP}{\left((abs(well_sgn \cdot x - VSTEP))^2 \right)^N + (eps^2)^N} \right]^{\frac{1}{2N}}$$



Junction Capacitance Affected by Resurf

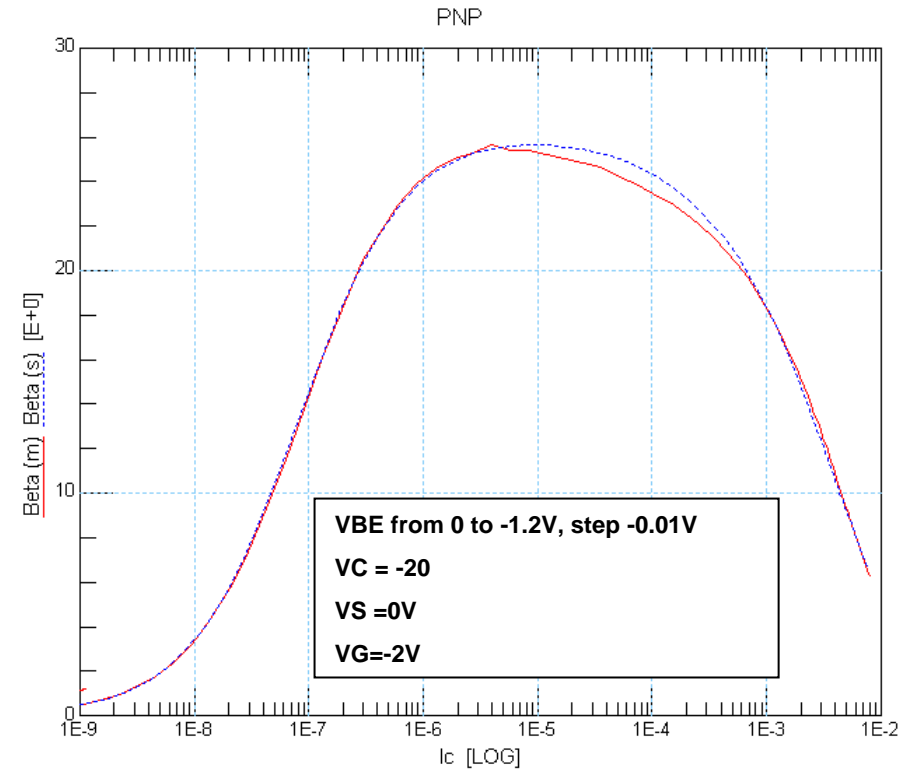
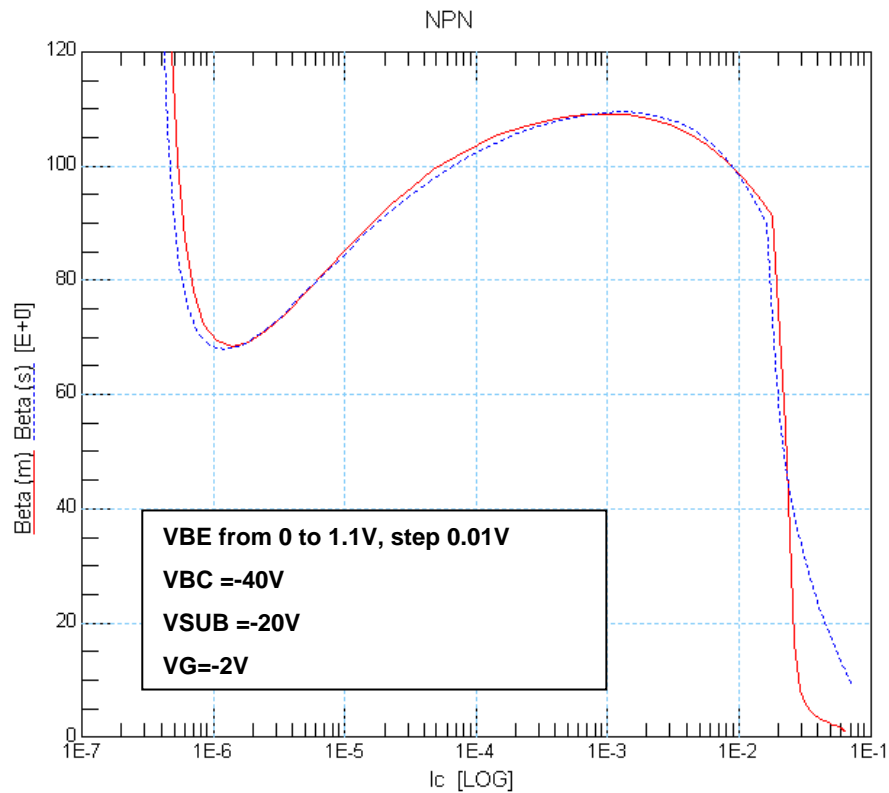


$$C_{JTOT} = C_{J1} + C_{J2}$$

$$C_{J1} = \left[\frac{C_{J01}}{\left(1 + \frac{X}{V_{J1}}\right)^{M_{J1}}} + CK_1 \right] \cdot 0.5 \cdot \left[\left(1 - \frac{X - V_P}{\left(\text{abs}(X - V_P)^{2N} + \text{eps}^{2N}\right)^{\frac{1}{2N}}} \right) \right]$$

$$C_{J2} = \left[\frac{C_{J02}}{\left(1 + \frac{X}{V_{J2}}\right)^{M_{J2}}} + CK_2 \right] \cdot 0.5 \cdot \left[\left(1 + \frac{X - V_P}{\left(\text{abs}(X - V_P)^{2N} + \text{eps}^{2N}\right)^{\frac{1}{2N}}} \right) \right]$$

Parasitic BJTs



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- Two models have been extracted in order to describe the whole level shifter:
 - *Mickey Mouse* perimeter
 - *Mickey Mouse Ears*
- Models are fully scalable with linear W , number of curves and number of *Ears*
- Models fit the whole temperature range: $-40 / 175$ °C.
- Models fully describe parasitic effects
- The highest flexibility for designers is guaranteed

- We want to thank gentlemen Designers, for support and useful discussions:
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End of Presentation

Thank you for your attention