Modeling of High Performance HV MOSFET Transistors in a 40nm Technology Node

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Outline

- Motivation
- HiSIM HV Extraction Flow
- Convergence Issues
- Corners and Statistical Model
- Model Verification
- Conclusion

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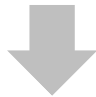
Motivation

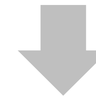
Digital CMOS technology has become a commodity

- Uniform set of requirements
- Foundry offerings with little differentiation

Analogue has diverse requirements

- Use customised technology or make do with digital CMOS devices
- Foundry offerings must be "fool-proof" to meet reliability specs.





IDMs

- **Outsource commoditised** Technology

IDMs

- ***Control technology & device-use to optimise performance***

Fab-Less

- Great for fab-less companies

Fab-Less

- ***Enable specialised devices***
- ***Taylor the device model***
- ***Understand & tightly control the use***

- Deploying specialised devices and models is a competitive advantage for fab-less semiconductor companies doing analogue design.

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CSR HV-MOS in 40nm Low-Power CMOS

- With no control of the use condition, the foundry HV-MOS must be conservative to pass device qual.
  - $R_{DS,ON}$ & capacitances are compromised
- CSR has characterised a customised HV-MOS in TSMC 40LP with performance and reliability tailored to the application in
  - Power management
  - RF applications
- Standard 52Å gate-oxide & well-Implants, triple well
- HiSIM HV was chosen to correctly represent critical DC & AC device properties

Notes:

- 40nm CMOS is a x0.9 shrink of 45nm layout dimensions.
- Electrical data is relative to shrink dimensions

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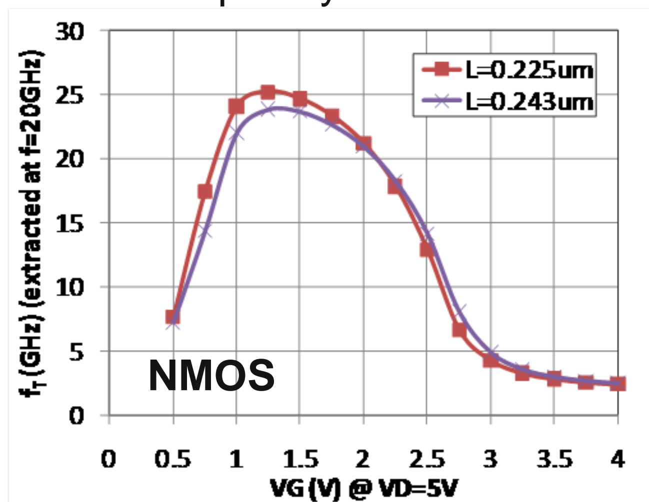
CSR 40nm HV-MOS Device Performance

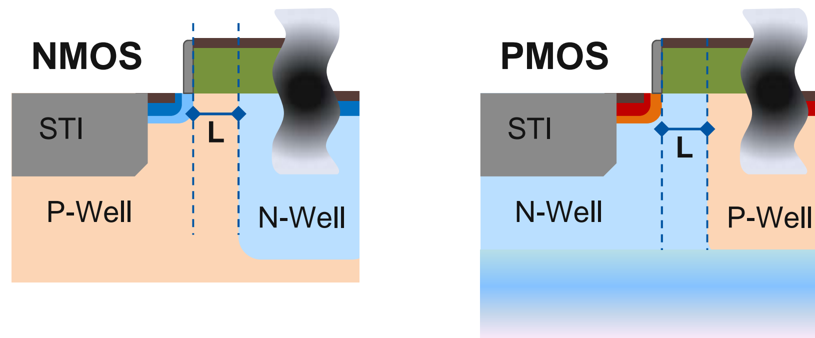
- CSR HV-MOS key device properties:
  - L=0.297um is default for use at V_{DD}=5V
  - For shorter L, reliability must be considered for each use case

	NMOS L=0.225um	NMOS, L=0.297um	PMOS, L=0.225um	PMOS, L=0.297um
BV_{DS}	>10V, limited by well-breakdown			
R_{DSON} @ V_G=2.5V(mΩmm²)	23	25	52	59
Ioff (pA/um)	40	<1	4	<1

Transit-Frequency



Device Cross-section



Notes: L is the length of the inversion channel (model-parameter **C**)

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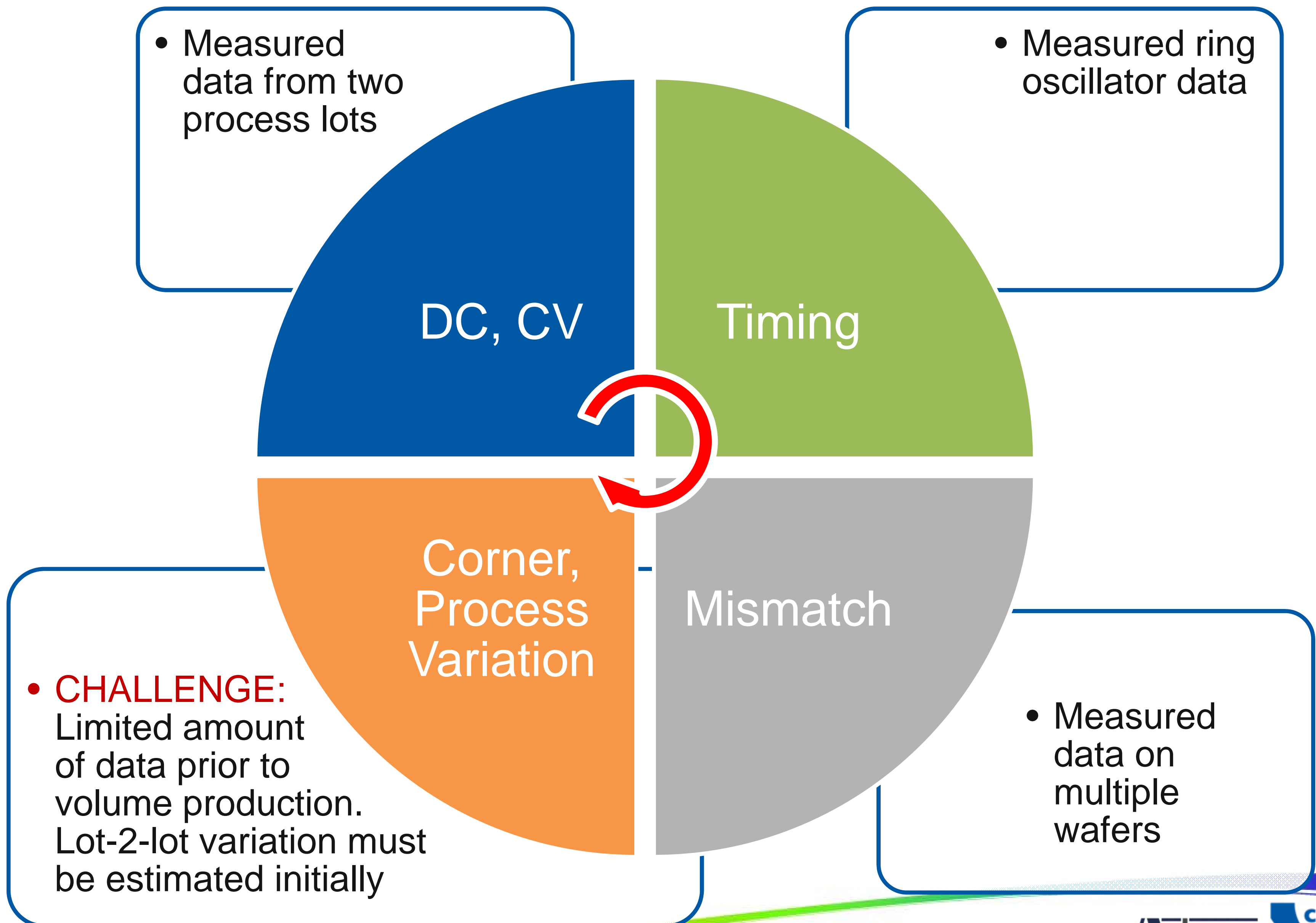
Model Parameter Extraction Flow



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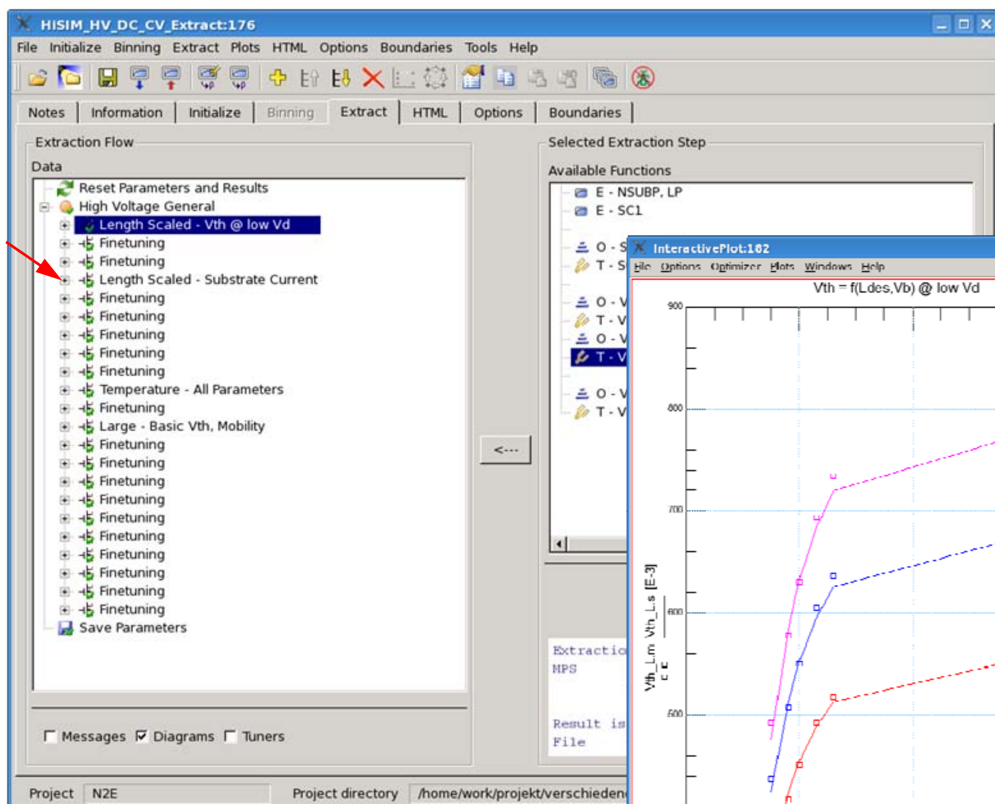
Parameter Extraction Tools



Extraction flow

Single interactive extraction step for Vth=f(L) @ diff. Vb values

- Used Software Tools
  - IC-CAP with ADS, Spectre and HSPICE, all installed and running on a Linux machine
  - HiSIM HV Extraction Tool from AdMOS

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Typical Parameter Extraction Setup

Configurable plot area

Optimizer / Tuner for parameter adjustment

Model complexity and the overlay of many effects (self heating, quasi saturation, velocity saturation, ..) required the simultaneous adjustment of different device characteristics like id-vg, id-vd, gm, gds, …

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Convergence issues – Cadence Spectre versions

- Convergence problems were observed on several circuits:
  - A power stage of a buck switcher
  - 2 LDOs
- Seen in MMSIM Spectre 7.1 & 7.2 up to ISR10 in model cards v0.2-v0.5
- No convergence issue observed in Eldo
- Most convergence issues disappear with MMSIM Spectre 7.2 ISR12 or MMSIM Spectre 10.1

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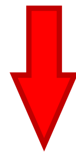
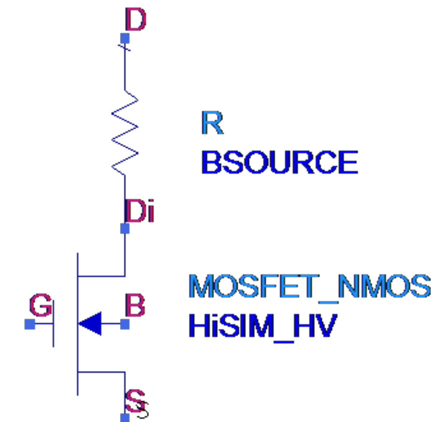
Convergence problems with early model versions (V0.2 – V0.5) forced us to:

- Use only the built-in resistance model in HiSIM HV without extra nodes (CORSRD=2) which is not sufficient to handle the complex drift region resistance with all of its voltage and geometry dependence.
- Switch off the self heating effect (COSELFHEAT=0)
- Use a BSOURCE (behavioral source) to model the drift region resistance as a function of terminal voltages and device dimensions.



- This caused extra effort in developing the BSOURCE equations together with parameter extraction in a "task force style".
- **Most Important: it delayed important design activities due to the need of re-modeling the device !!**



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Model Version History

Library Version	HiSIM HV Version	CORSRD	COSELF HEAT	BSOURCE usage	Comment / Problems
V0.2	1.1.1	3	1	n	• Good DC behaviour • Convergence problem in a small and simple circuit during transient simulations (ring oscillator was o.k. !) • Show stopper for design !
V0.5	1.2.0	3	1	n	• Still convergence problems in some circuits during transient simulations • Show stopper for design !
V0.7	1.2.0	2	0	y	• DC behaviour needs high effort in BSOURCE modeling. • Still minor problems with transient simulation of different circuits (e.g. ring oscillators)
V0.8	1.2.1	2	0	y	• No reported problems with transient simulation of different circuits
V0.x	1.2.1	3	1	n	• Will be investigated

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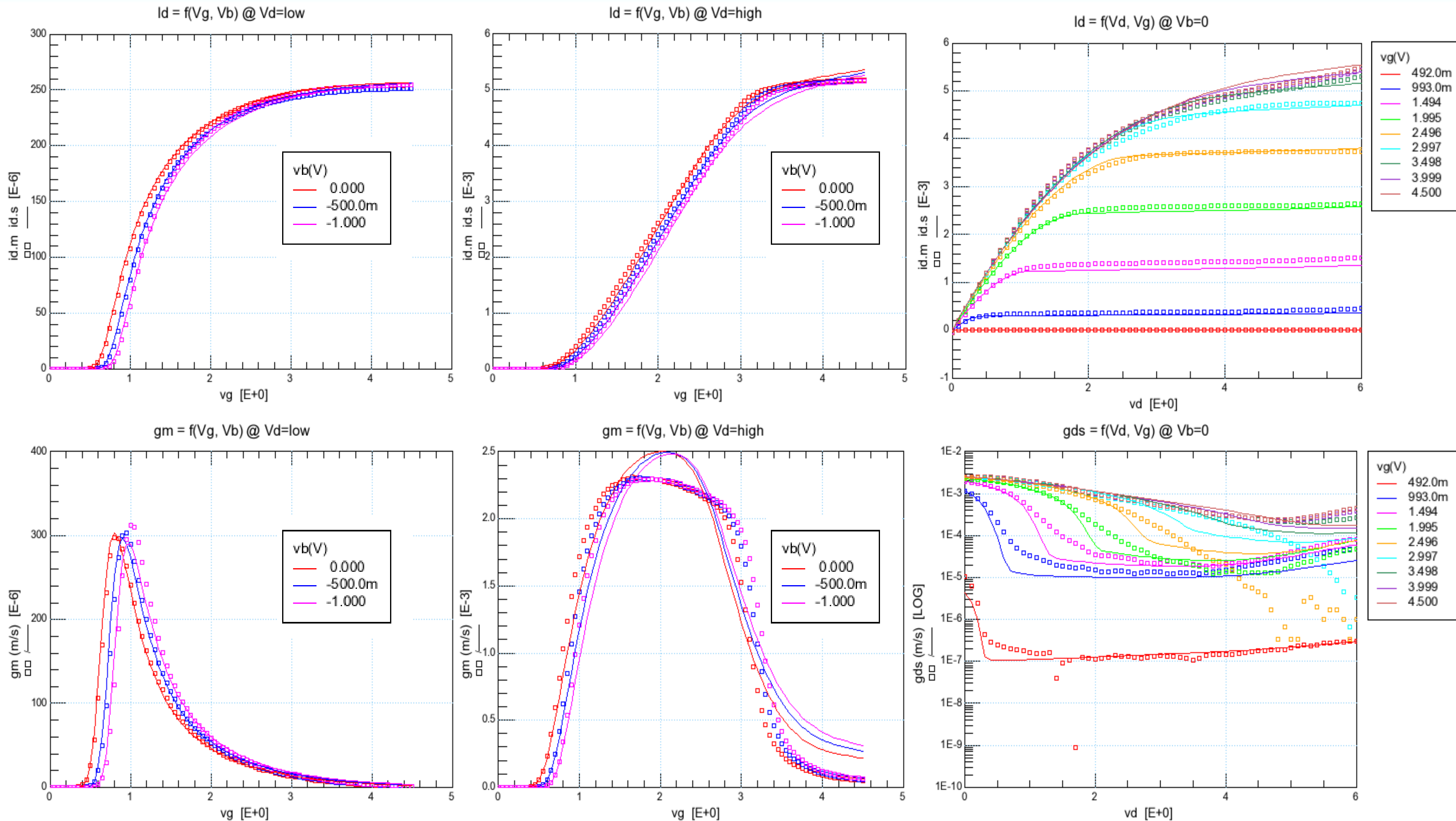
Parameter Extractions Results with CORSRD=3 and COSELFHEAT=1



- Plots show measurement (symbols) vs. simulated curves of an n-type transistor (L=0.27um) (model V0.2)
- The model is a pure HiSIM HV 1.11 model without any external components
- All diagrams show a reasonably good fit.

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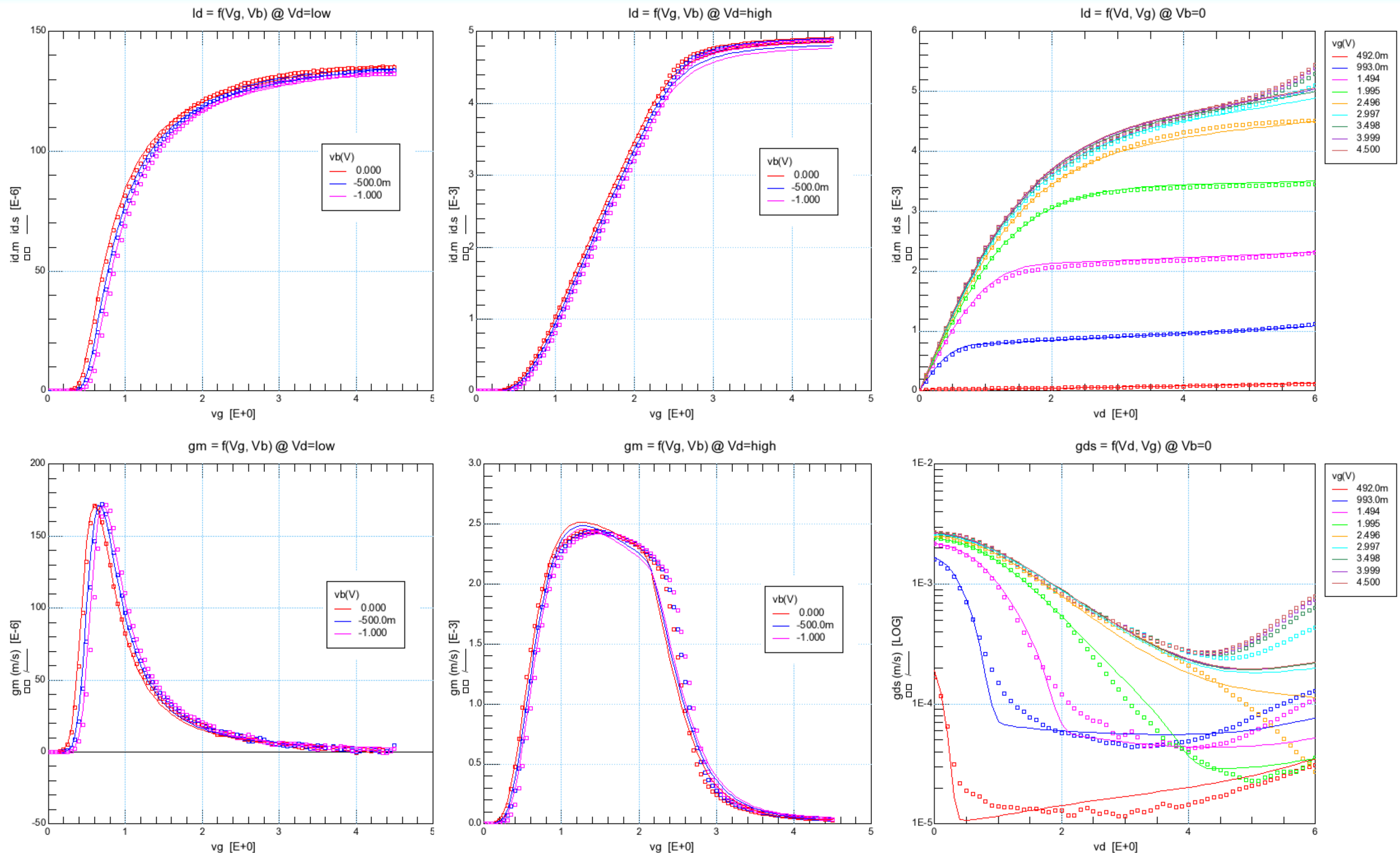
Parameter Extractions Results with CORSRD=2, COSELFHEAT=0 and BSOURCE



- NMOS (L=0.225um), using a bsource element to model the drift region resistance (model V0.8)
- Please note the good agreement of g_m with the bsource implementation compared to the appropriate plot on the previous page with a pure HiSIM HV model

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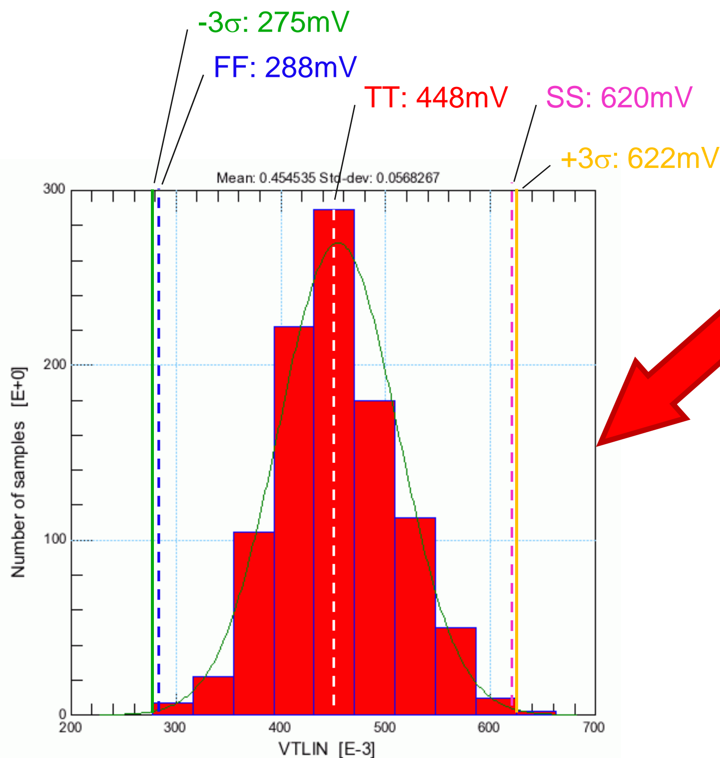
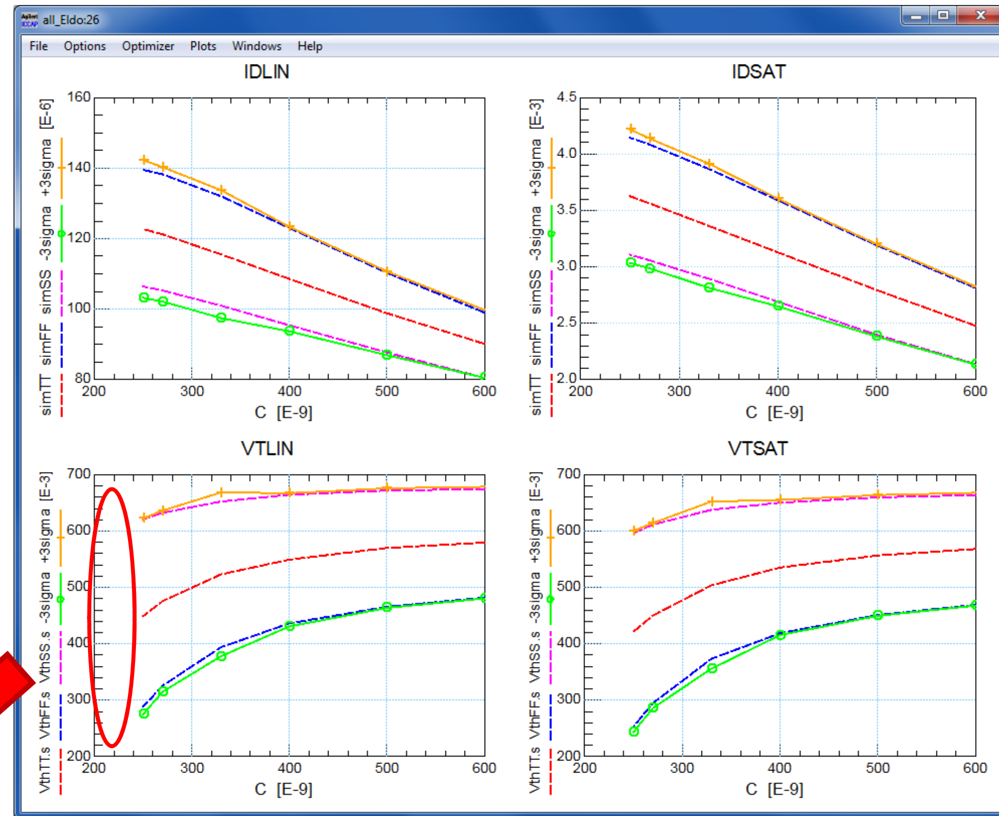
Corner and Process Variations

- Providing a statistical model ahead of volume production relies on engineering judgment.
- Estimating parameter variation of main PCM values like idlin, idsat, vtlin, vtsat, ..





- Adjustment of both, corner cases (SS, FF, TT, SF, FS) and statistical variations to upper and lower values of PCM data versus the effective channel length.

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Parameters for Corner and Process Variation Modeling

Parameter	Description	Effects / Notes
TOX	Physical gate oxide thickness	
NSUBC	Substrate impurity concentration	Note: VFBC has only limited range (-1.2 .. -0.8) and is not suitable to model variation over a wider range.
SC1	Short channel effect of Vth	
MUEPHL	Low field mobility $\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}$ $\mu_{PH} = MUEPH1 \cdot \left(1 + \frac{MUEPHL}{\left(L \cdot 10^6\right)^{MUEPLP}}\right)$	Please note: range of MUEPH0 is very restricted (0.25<MUEPH0<0.35)
MUEPLP		Therefore, MUEPHO is not very useful for corner variations.
NINVD	Reduced resistance effect for low Vds	High field mobility

The parameters in the table above have been selected for both, worst case corner modeling as well as for a statistical model which is feasible for Monte Carlo simulations.

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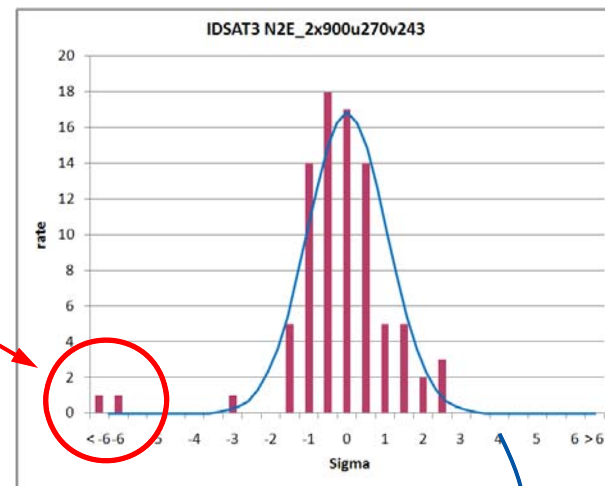
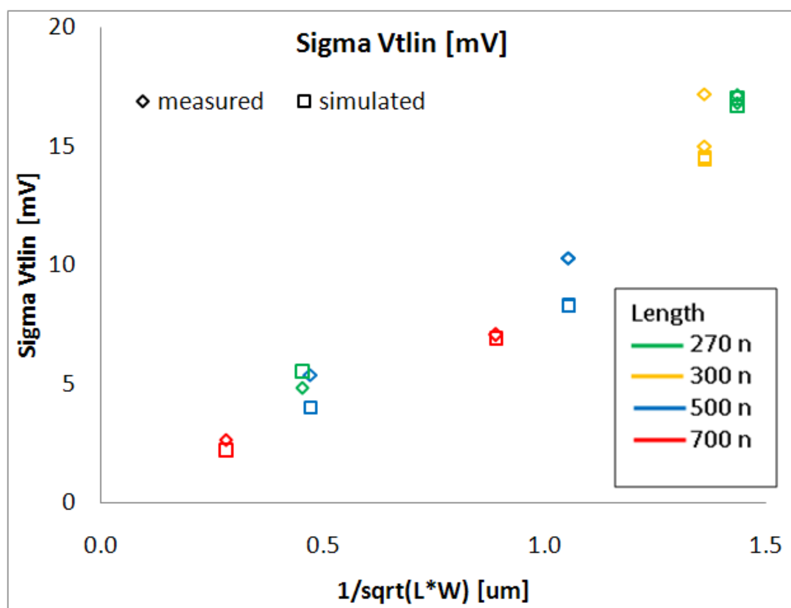
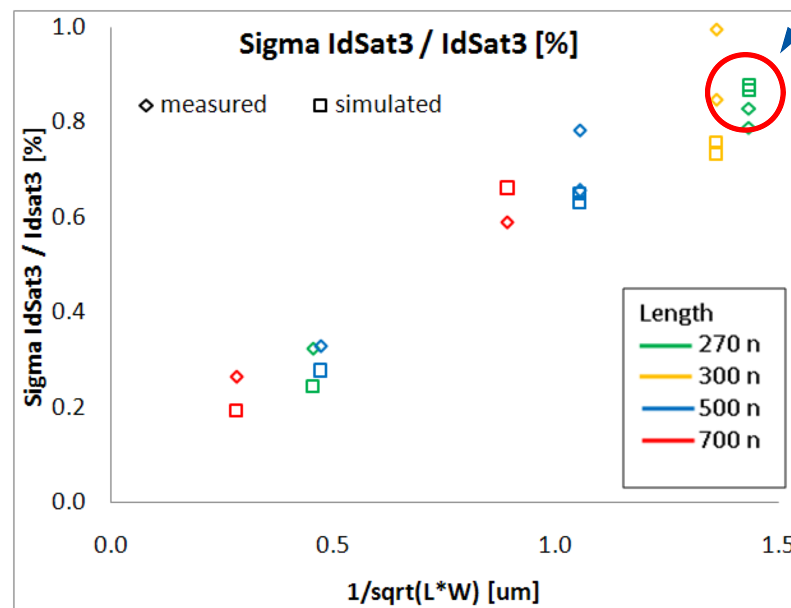
Mismatch Model

- Mismatch test structures with diff. L/W have been evaluated on 2 wafers for typical PCM values: vt_{lin}, vt_{sat}, gm_{max}, id_{lin}, multiple id_{sat}, ...
- To avoid unrealistic values, outliers had to be removed.
- Classic mismatch formula could be applied and resulted in good agreements between measured and simulated values (see vt_{lin} and id_{sat3} below)

Outliers are not taken into account







Note: Idsat3: VG=2.5V, VD=5V

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Parameters applied for Mismatch Variation Modeling

Parameter	Description	Effects / Notes
NSUBC	Substrate impurity concentration	Threshold voltage
SC1	Short channel effect of Vth	
SC2	Short channel effect of Vth at high drain voltage	
MUECB1		Low field mobility
RDEXTVG	Parameters of user defined bsource element which	Saturation region
RDEXTVG1	represents the drift region resistance	

The parameters in the table above have been selected for the modeling of the mismatch behaviour.

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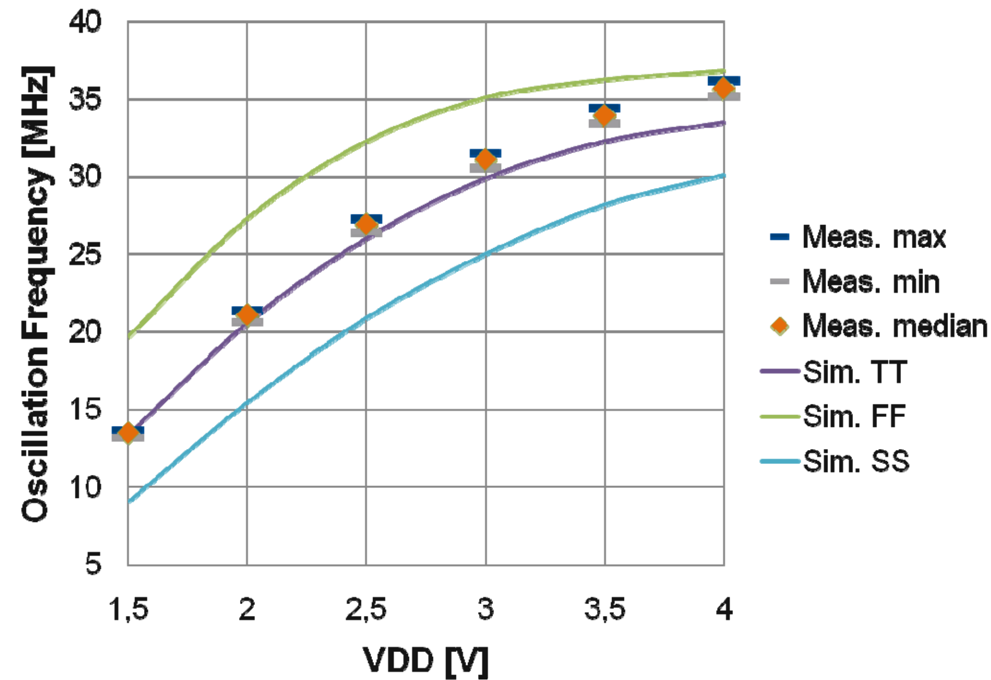
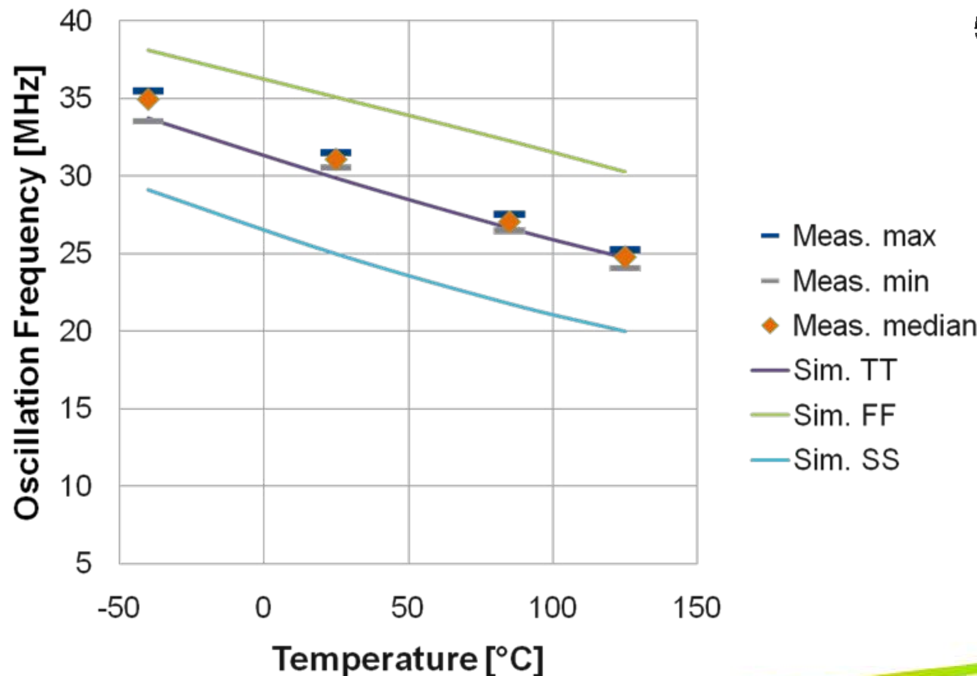
Timing Verification using Ring Oscillator Measurements

- The timing behaviour of the models is evaluated by the simulation of ring oscillator circuits.
- Details:
  - 199 Stages
  - Enable/Disable Feature
  - Output buffer and divider





- Measurements are done at:
  - Temperatures between -40°C and 125°C
  - Supply voltages VDD between 1.5V and 4.0V
- The models fit well without changes inside the given tolerance

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Summary/Conclusion

- Fab-less companies need control over special devices to compete with IDMs in the analogue space
- The presentation describes a complete modeling flow used by a fab-less company
- Limited access to statistical data prior to volume production requires careful estimation of production variation
- Critical convergence problems occurred with HiSIM HV (different model versions) in Spectre (different versions). This caused a delay in very important design activities.
- Workaround: Apply old style solution to model drift region using a resistor.

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