



I-V and C-V Results of the EPFL-High Voltage MOSFET Model

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High Voltage MOSFET Modeling

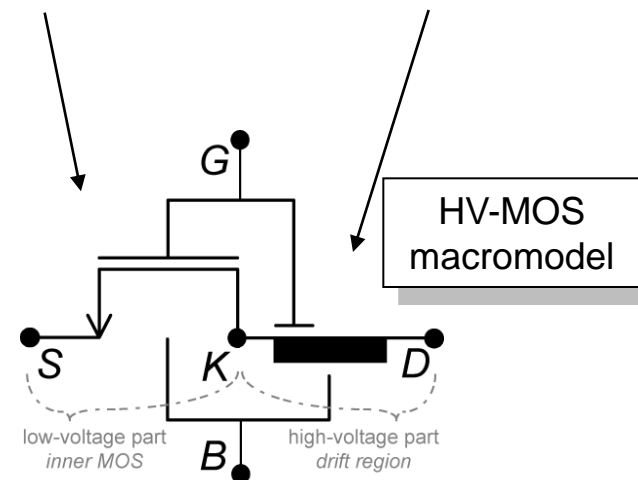
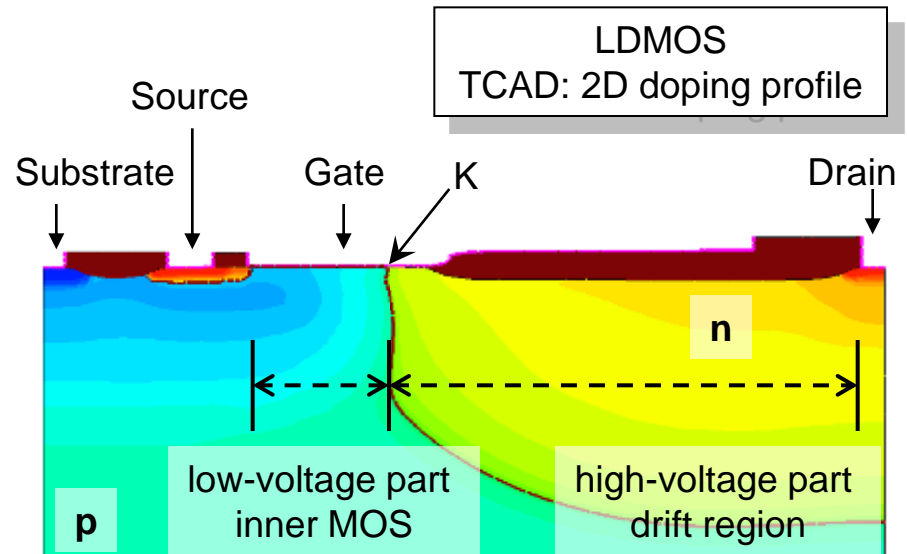
Spring MOS-AK/GSA Workshop,
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Outline

- Description of the HV-MOS device and model
 - Low-Voltage part (LV)
 - Inner MOS
 - High-Voltage part
 - Drift region
- Evaluation of the model
 - I-V
 - C-V
- Implementation of the model
 - Current status
- Next steps

Typical Structure of HV-MOS

- HV-MOS: 2 parts
 - Connection point: ‘K’
 - Doping changes type
 - Between channel and drift
- Low-voltage part [1]
 - inner MOSFET
 - inner drain is ‘K’
- High-voltage part [2]
 - Drift region
 - A physics-based model

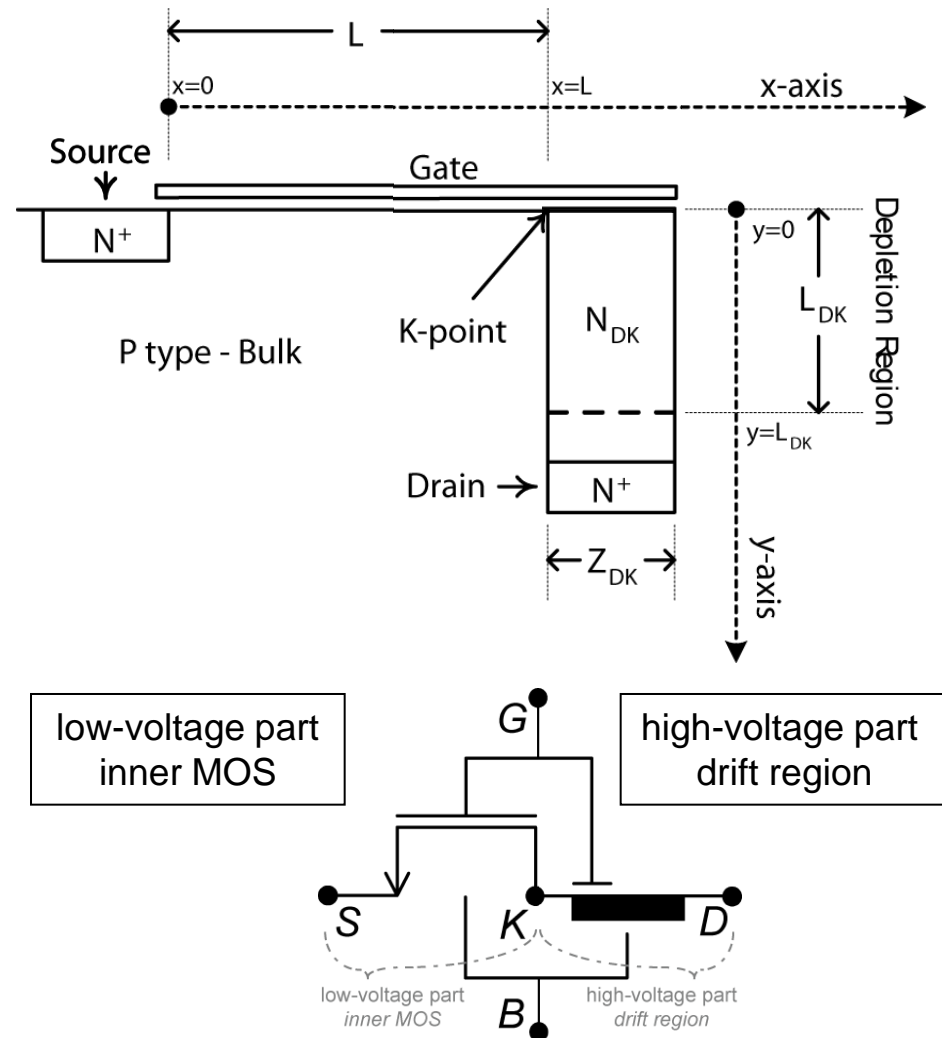


[1] Y. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. Ionescu, “Compact Modeling of Lateral Nonuniform Doping in High-Voltage MOSFETs,” *Electron Devices, IEEE Transactions on*, vol. 54, no. 6, pp. 1527–1539, June 2007.

[2] A. Bazigos, F. Krummenacher, J.-M. Sallese, M. Bucher, E. Seebacher, W. Posch, K. Molnár and M. Tang, “A physics-based analytical compact model for the Drift region of the HV-MOSFET” *Electron Devices, IEEE Transactions on*, Accepted for publication, doi: 10.1109/TED.2011.2119487

From “1×2D” to “2×1D”

- HV-MOS: 2D problem
 - Split into 2 axes
 - x-axis: inner MOS
 - Source to ‘K’
 - y-axis: DRIFT region
 - ‘K’ to Drain
- Simplified HV-MOS: two 1D problems
 - Solution possible



Effects included in the model

- Low-voltage part / Inner MOS
 - Reverse Short Channel Effect
 - Lateral Non-Uniform Doping
 - Velocity Saturation
 - Mobility Reduction due to Vertical Field
 - Sub-threshold barrier lowering
- High-voltage part / DRIFT region
 - Quasi-Saturation
 - Impact Ionization Current
- Both
 - DC and CV behavior
 - Self-Heating
 - Temperature effects
 - Geometrical effects

Evaluation I-V

(published in [2])

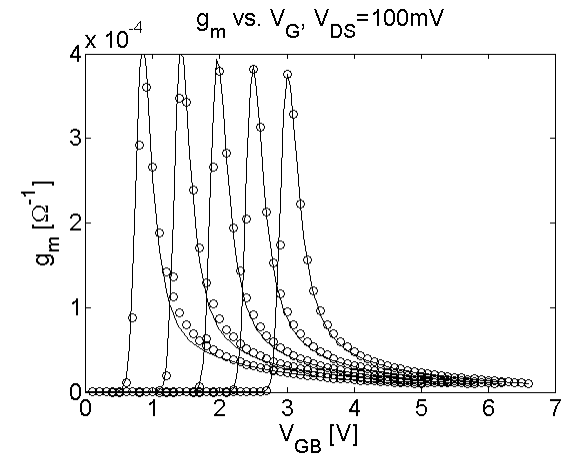
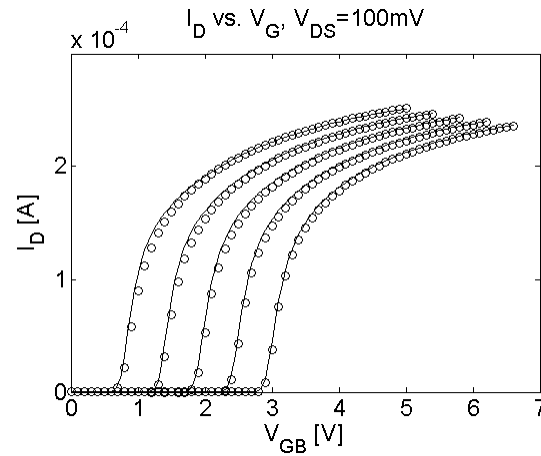
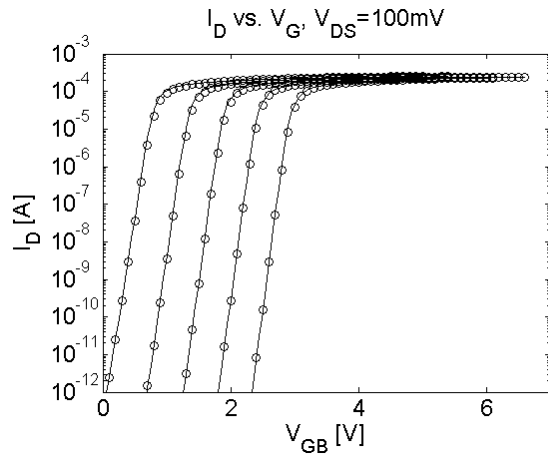
Device: LDMOS

TOX = 15nm

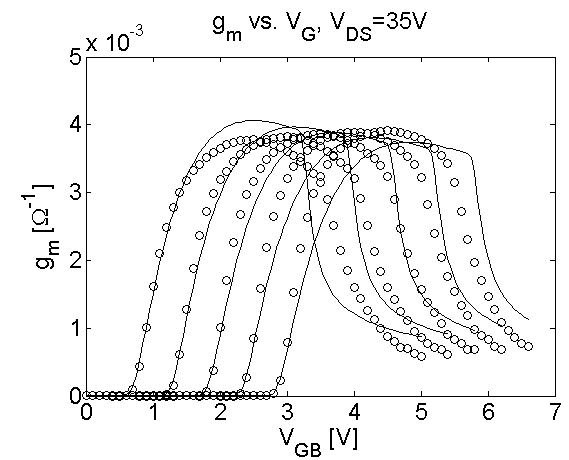
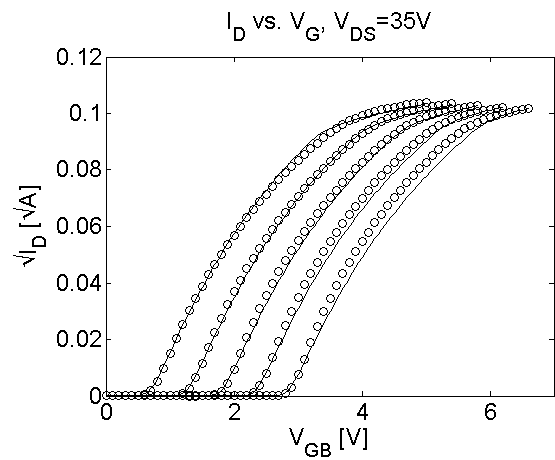
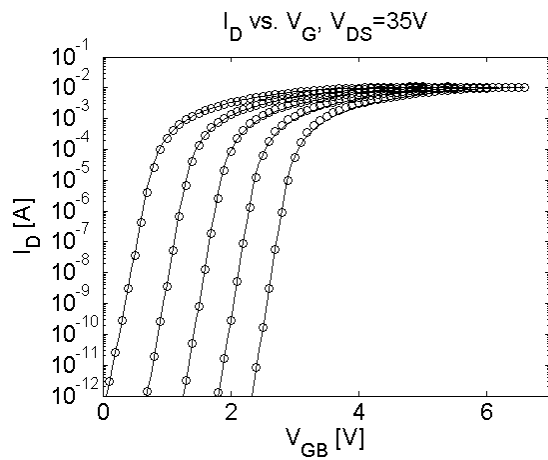
W = 40 μ m

L = 400nm

$V_{DS} = 100\text{mV}$



$V_{DS} = 35\text{V}$



Evaluation C-V

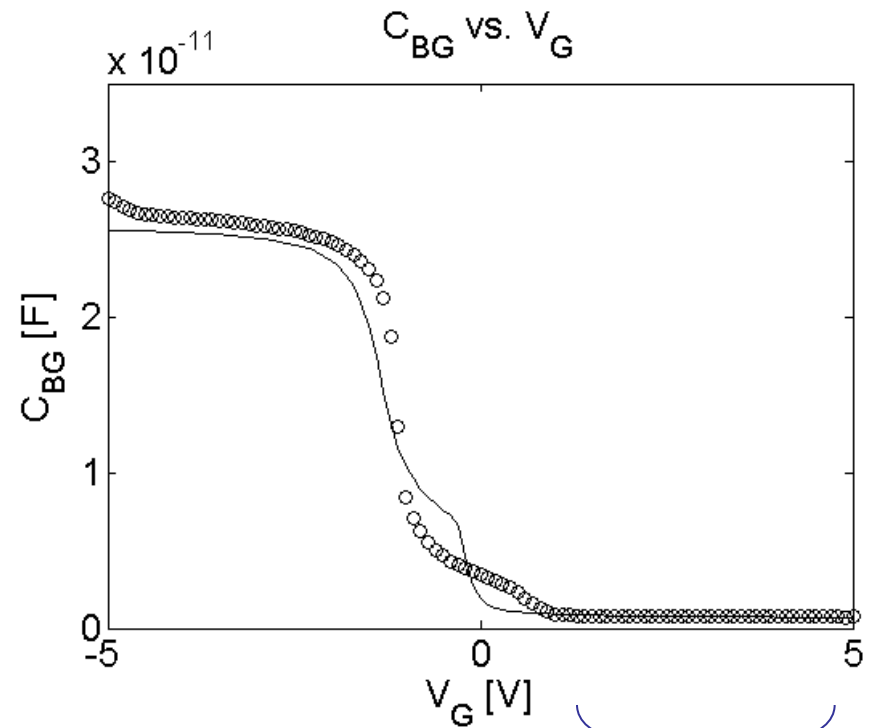
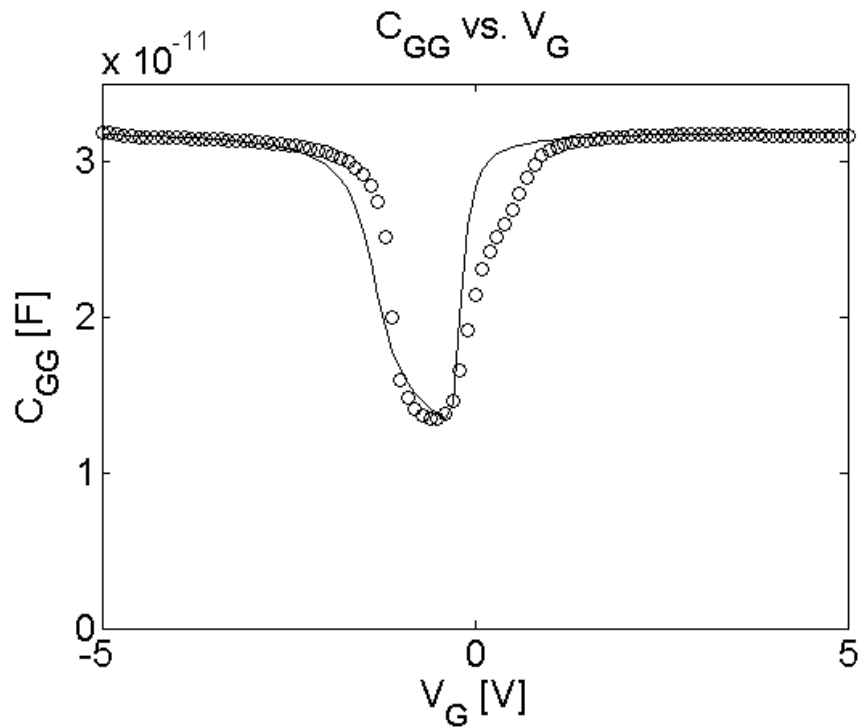
C_{GG}, C_{GB}

Device: LDMOS

TOX = 15nm

W = 4000 μ m

L = 400nm



- $V_{DS} = 0V$

C_{GB} Overlap

Evaluation C-V

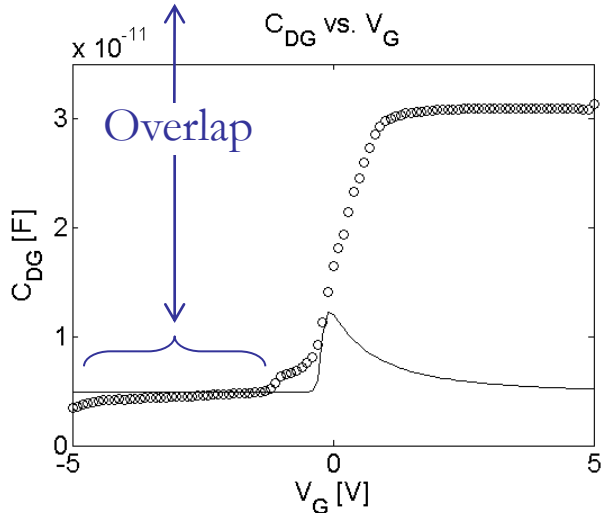
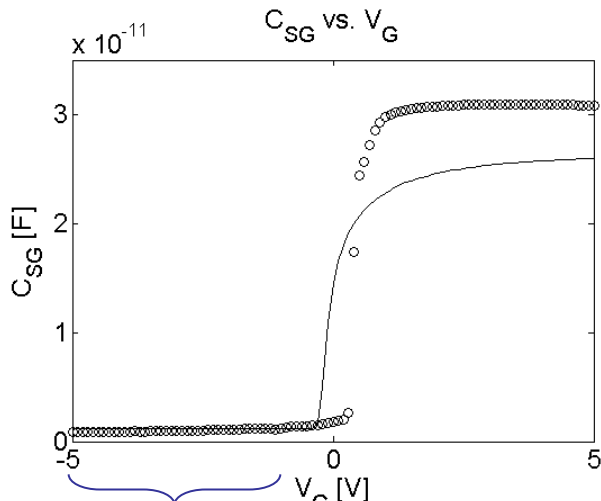
Device: LDMOS

TOX = 15nm

W = 4000μm

L = 400nm

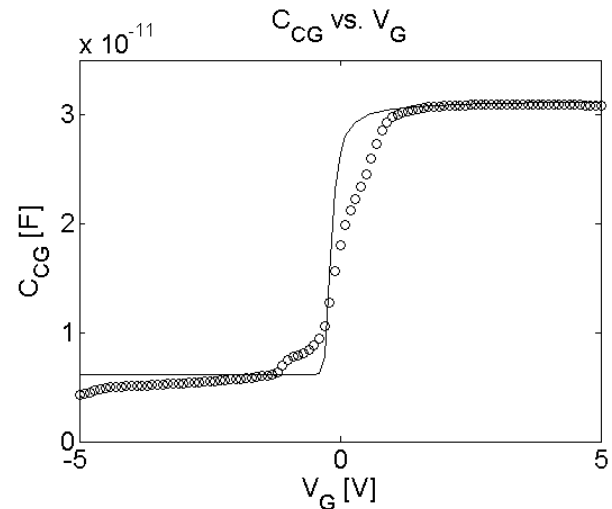
$$C_{GS} + C_{GD} = C_{GC}$$



C_{GS}

+

C_{GD}



- $V_{DS} = 0V$
- “Measured” $C_{GS} = C_{GD}$ in inversion
 - Floating nodes during measurements
- Drain side overlap > Source
- “Simulated” $C_{GD} < C_{GS}$ in inversion

Evaluation C-V (RF)

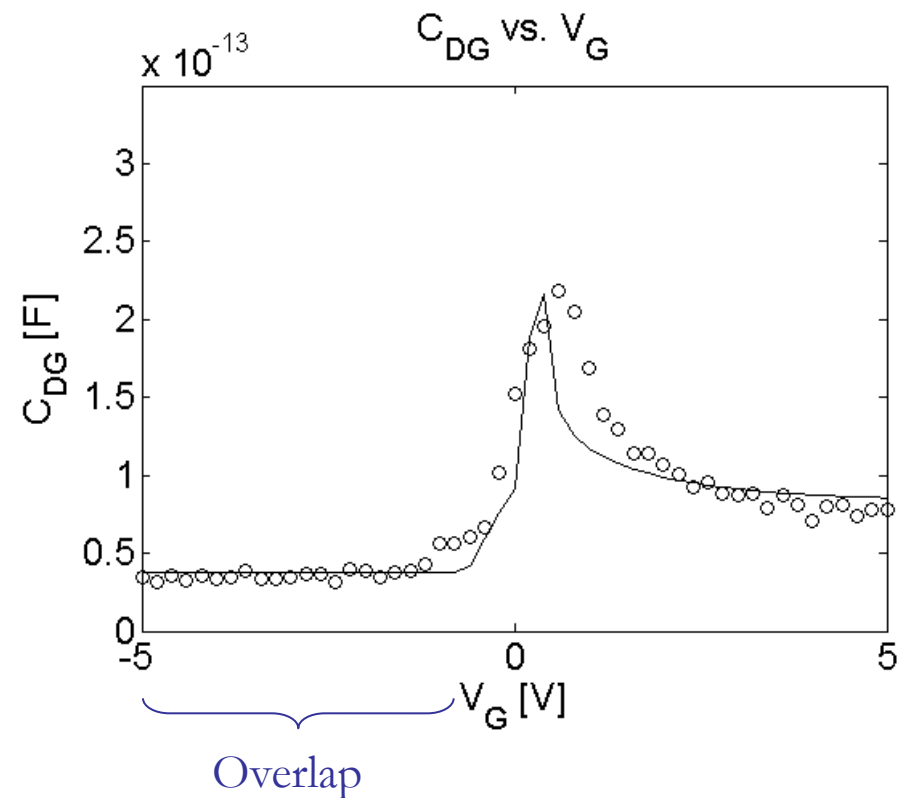
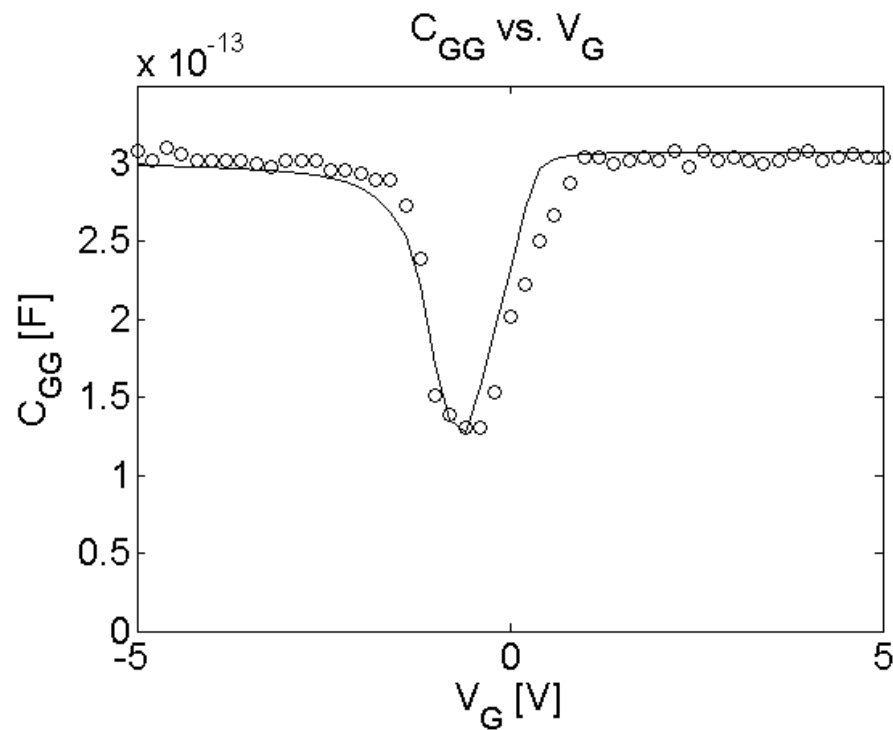
Device: LDMOS

TOX = 15nm

W = 40μm

L = 400nm

$$C_{GG} = \text{Im}(Y_{11}) / 2\pi f_{\text{spot}}, \quad C_{GD} = \text{Im}(Y_{21}) / 2\pi f_{\text{spot}}$$



- $V_{DS} = 0V$
- $f_{\text{spot}} = 50\text{MHz}$

Implementation

- Verilog-A code
 - Current, under development Version: 1.105
 - Includes CV behavior
 - Released Version: 1.101 (25 May 2010)
 - Draft documentation available for v1.101
 - Includes: Parameter extraction general guidelines
 - Hierarchical structure
 - 1 main file (~800 lines)
 - 9 called-in include files (~2100 lines)
 - variables, parameters, helping and debugging functions

Parameter list

(1/2, from the draft documentation)

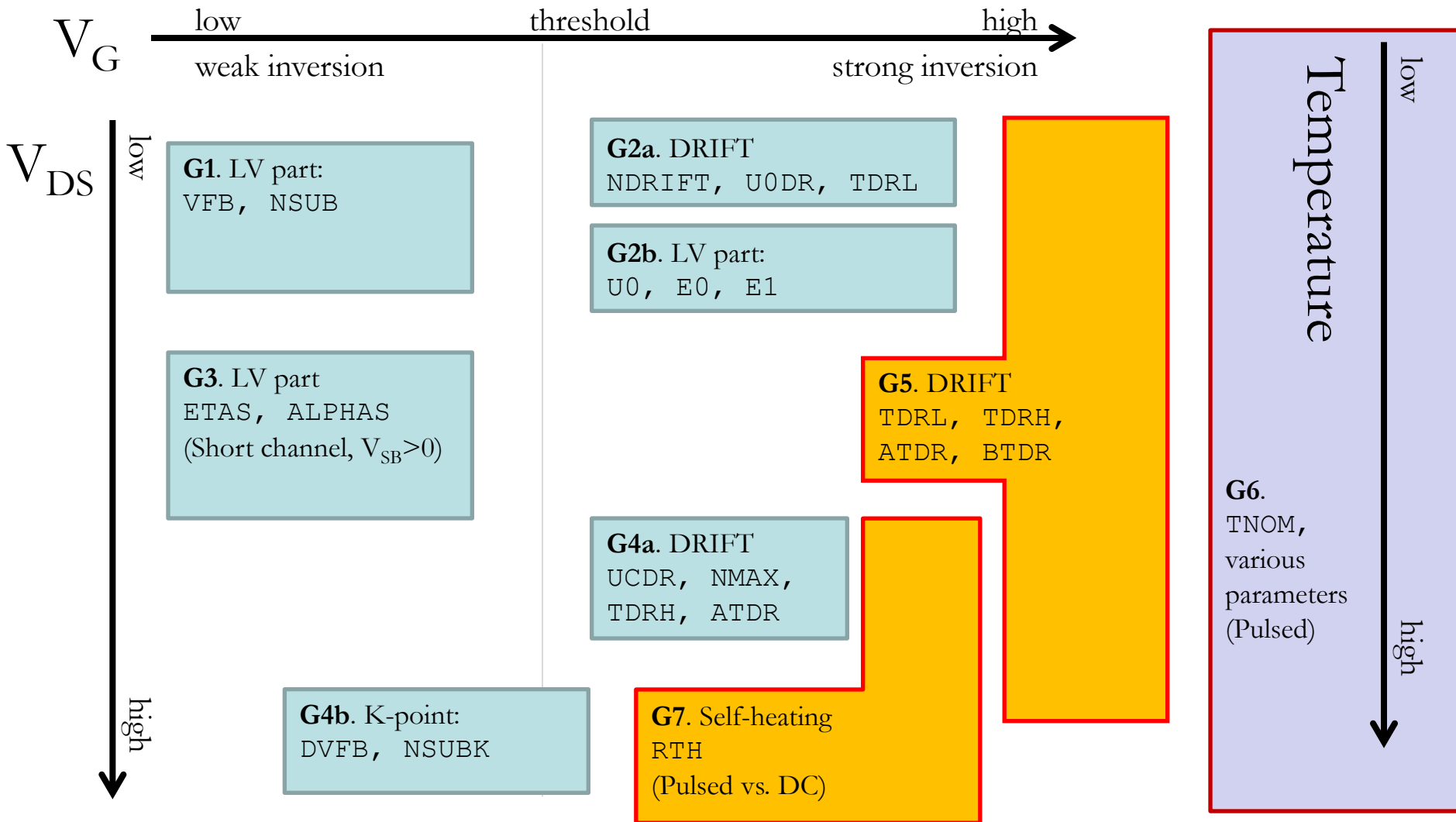
Name	Value	Min	Max	Short Description / Notes	Unit	Name	Value	Min	Max	Short Description / Notes	Unit
Instance Parameters						Mobility Parameters					
W	40·10 ⁻⁶	0	∞	Drawn device Width (Width of gate region).	m	U0	600	0	∞	Low-field mobility. If U0 = 0 then KP is used.	cm ² /Vs
L	10 ⁻⁶	0	∞	Drawn device Length (Length of gate region).	m	KP	0	0	∞	Low-field transconductance factor.	A/V ²
Flags and Setup Parameters						Mobility Reduction due to Vertical Field					
TYPE	1	-1	1	Channel type selector, TYPE = +1 for NMOS, TYPE = -1 for PMOS.	-	E0	150·10 ⁶	1	∞	1st-order mobility reduction characteristic field.	V/m
SHNET	1	0	1	Internal Self-Heating network: SHNET = 0 for Self-Heating OFF, SHNET = 1 for Self-Heating ON.	-	E1	200·10 ⁶	1	∞	2nd-order mobility reduction characteristic field.	V/m
Main Physical and Electrical Parameters						Bias Dependence and Length Scaling of Equivalent Pinch-Off Voltage Gradient					
TOX	50·10 ⁻⁹	0	∞	Gate oxide thickness. If TOX = 0 then COX is used.	m	DGC1	0.25	0	1	Bulk doping gradient 1st-order inversion scaling coefficient.	-
COX	0.7·10 ⁻³	0	∞	Gate oxide capacitance per unit area.	F/m ²	DGC2	0	0	1	Bulk doping gradient 2nd-order inversion scaling coefficient.	-
VFB	-1.1	-∞	∞	Flat-Band voltage at source end of channel. If VFB = -10 ³ then VT0 is used.	V	DGE	0.5	0	1	Bulk doping gradient length scaling exponent.	-
VT0	0.8	-∞	∞	Zero-bias Threshold voltage.	V	Non-Uniform Doping Length Scaling Factor for Intermediate and Long Channel Devices					
NSUB	10 ¹⁷	0	∞	Bulk doping concentration at source end of channel. If NSUB = 0 then GAMMA is used.	cm ⁻³	LDG	10 ⁻⁶	10 ⁻⁹	∞	Bulk doping gradient characteristic length.	m
GAMMA	0.5	0	∞	Body effect factor at source side of channel.	V ^{1/2}	Geometrical Parameters (Short and Narrow Channel Corrections)					
PHIF	0	0	∞	Bulk Fermi potential at source end of channel. If PHIF = 0 then NSUB or GAMMA is used for the Fermi potential calculation.	V	DL	0	0	∞	Length offset of gate oxide region.	m
DVFB	0	-∞	∞	Flat-Band voltage offset between source and drain end of channel. If DVFB = -10 ³ then DVT is used, but then VT0 must also be used.	V	DW	0	0	∞	Width offset of gate oxide region.	m
DVT0	0	-∞	∞	Threshold voltage offset between source and drain end of channel.	V	DWD	0	0	∞	Width offset of drift region.	m
NSUBK	10 ¹⁷	0	∞	Bulk doping concentration at drain end of channel (K-Point). If NSUBK = 0 then GAMMAK is used.	cm ⁻³	Reverse Short Channel Effect					
GAMMAK	0.5	0	∞	Body effect factor at drain end of channel (K-Point).	V ^{1/2}	LR	0.1·10 ⁻⁶	0	∞	Reverse short channel characteristic length.	m
PHIFK	0	0	∞	Bulk Fermi potential at drain end of channel. If PHIFK = 0 then NSUBK or GAMMAK is used for the Fermi potential calculation.	V	QLR	0	-∞	∞	Reverse short channel Threshold voltage coefficient.	C/m ²
						Subthreshold Barrier Lowering					
						ETAS					
						SIGMAS					
						ALPHAS					
						BETAS					
						Velocity Saturation					
						VSAT					
						UCRIT					
						Channel Length Modulation					
						LAMBDA					
						LC					

Parameter list

(2/2, from the draft documentation)

Name	Value	Min	Max	Short Description / Notes	Unit	Name	Value	Min	Max	Short Description / Notes	Unit
Drift Region						Impact Ionization Current					
Geometrical Parameters						IBA	0	0	∞	First impact ionization coefficient.	1/m
LDR	$4 \cdot 10^{-6}$	0	∞	Length of depleted drift region.	m	IBB	$50 \cdot 10^6$	10^6	∞	Second impact ionization coefficient.	V/m
TDRL	$0.8 \cdot 10^{-6}$	0	∞	Current flow thickness in drift region at low V_{DS} .	m	IBN	1	0	∞	Saturation voltage factor for impact ionization.	-
TDRH	$0.5 \cdot 10^{-6}$	0	∞	Current flow thickness in drift region at high V_{DS} .	m	IBH1	1	0	∞	High-current roll-off factor for impact ionization.	-
TDRLS	0	$-\infty$	∞	Low V_{DS} body bias sensitivity of drift current flow thickness.	1/V	IBH2	1	0	∞	High-current roll-off exponent for impact ionization.	-
TDRHS	0	$-\infty$	∞	High V_{DS} body bias sensitivity of drift current flow thickness.	1/V	Self-Heating					
Gate Overlap Length Over The Drift Region (used in AC behaviour)						RTH	0	0	∞	Thermal resistance at zero injected power.	$^{\circ}\text{C}/\text{W}$
						CTH	0	0	∞	Thermal capacitance.	s \cdot W/ $^{\circ}$ C
Charge-Sheet Accumulation Layer Thickness (used in AC behaviour)						Temperature Parameters					
						TCVT0	0	$-\infty$	$:\infty$	Temperature coefficient of threshold voltage (VT0).	V/ $^{\circ}$ C
DACC	$20 \cdot 10^{-9}$	10^{-9}	LDR	Charge-sheet accumulation layer thickness.	m	TCDVTO	0	$-\infty$	∞	Temperature coefficient of threshold voltage offset between source and drain end of channel (DVT0).	V/ $^{\circ}$ C
Main Physical and Electrical Parameters						TCVFB	0	$-\infty$	∞	Temperature coefficient of Flat-Band Voltage (VFB).	V/ $^{\circ}$ C
						NDRIFT	$5 \cdot 10^{16}$	0	∞	Drift region doping concentration. If NDRIFT = 0 then GAMMAD is used.	cm $^{-3}$
GAMMAD	0	0	∞	Drift region modulation factor.	$\sqrt{1/2}$	TCRTH	0	-1	1	Temperature coefficient of RTH.	$^{\circ}\text{C}^{-1}$
PHIFD	0	0	∞	Drift region Fermi potential. If PHIFD = 0 then NDRIFT or GAMMAD is used for the Fermi Potential calculation.	V	BEX	-1.5	$-\infty$	∞	Mobility temperature exponent (U0).	-
Mobility Parameters						BDREX	-1.5	$-\infty$	∞	Drift region mobility temperature exponent (U0DR).	-
						U0DR	600	0	∞	Drift region low-field mobility. If U0DR = 0 then KPDR is used.	cm 2 /V
KPDR	0	0	∞	Drift region low-field transconductance factor.	A/V 2	UCDREX	1	$-\infty$	∞	Drift region longitudinal critical field temperature exponent (UCDR).	-
Velocity Saturation						E0EX	0	$-\infty$	∞	Temperature exponent for E0.	-
						VSATDR	0	0	∞	Saturation velocity in drift. If VSATDR = 0 then UCDR is used.	m/s
UCDR	$3 \cdot 10^6$	1.0	∞	Longitudinal critical field in drift region.	V/m	TCNMAX	0	-1	1	Temperature coefficient of NMAX.	$^{\circ}\text{C}^{-1}$
Quasi-Saturation						TCETAS	0	-1	1	Temperature coefficient of ETAS.	$^{\circ}\text{C}^{-1}$
						ATDR	1	0	∞	Quasi-saturation smoothing factor.	-
BTDR	0.3	0	∞	Quasi-saturation fine-tuning coefficient.	-	TCTDRH	0	-1	1	Temperature coefficient of TDRH.	$^{\circ}\text{C}^{-1}$
Maximum Doping at the Drain Side						TCATDR	0	-1	1	Temperature coefficient of ATDR.	$^{\circ}\text{C}^{-1}$
						NMAX	10	0	∞	Maximum relative carrier concentration in the drift.	-
						IBBT	0	-1	1	Temperature coefficient of IBB.	$^{\circ}\text{C}^{-1}$

Parameter Extraction Guidelines



Next Steps

- Finalization of the CV model
 - Study of CV via RF measurements with positive V_{DS}
 - Preparation of publication on the CV model
 - Release of the next version of the model
- Update of the documentation
 - Parameter extraction procedure
- Transient analysis
- RF model
 - NQS behaviour

References

- [1] Y. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. Ionescu, “**Compact Modeling of Lateral Nonuniform Doping in High-Voltage MOSFETs**,” *Electron Devices, IEEE Transactions on*, vol. 54, no. 6, pp. 1527–1539, June 2007.
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- [3] A. Bazigos, F. Krummenacher, J.-M. Sallese, “**Recent Developments on the EPFL - High Voltage MOSFET Model (EPFL-HVMOS)**”, Poster Presentation at MOS-AK/GSA ESSDERC/ESSCIRC Workshop 2010, Sept. 17, Seville
- [4] Yogesh Singh Chauhan, “**Compact modeling of high voltage MOSFETs**”, Thèse EPFL, no 3915 (2007).
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- [6] W. Grabinski and T. Gneiting, (Eds.) “**POWER/HVMOS Devices Compact Modeling**”, 1st Edition. 2010, Springer, ISBN: 978-90-481-3045-0

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