I-V and C-V Results of the EPFL-High Voltage MOSFET Model

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COmpact MOdelling Network
Work Group 2
High Voltage MOSFET Modeling

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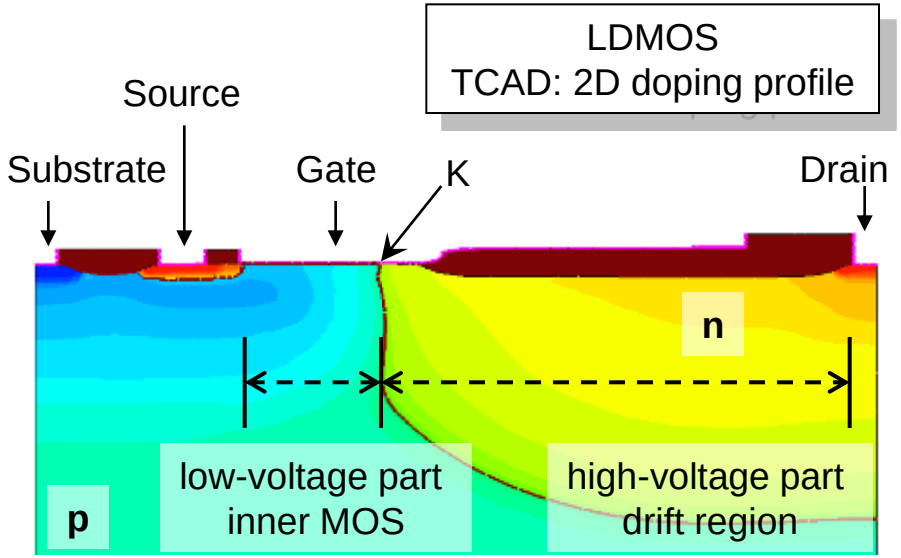
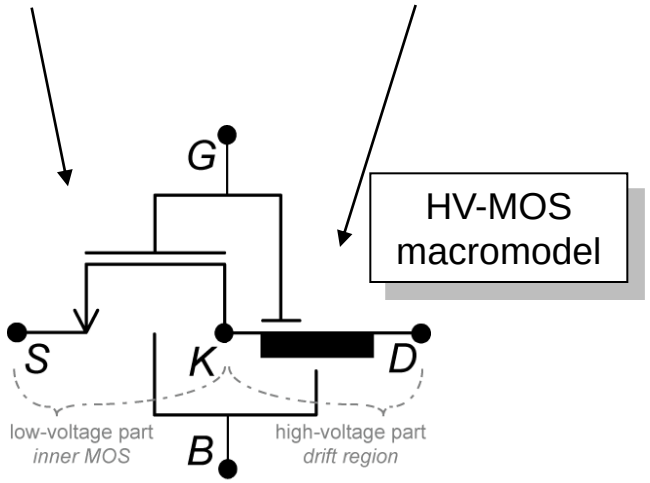
Outline

- Description of the HV-MOS device and model
  - Low-Voltage part (LV)
    - Inner MOS
  - High-Voltage part
    - Drift region
- Evaluation of the model
  - I-V
  - C-V
- Implementation of the model
  - Current status
- Next steps

Typical Structure of HV-MOS

- HV-MOS: 2 parts
  - Connection point: 'K'
  - Doping changes type
  - Between channel and drift
- Low-voltage part [1]
  - inner MOSFET
    - inner drain is 'K'
- High-voltage part [2]
  - Drift region
    - A physics-based model



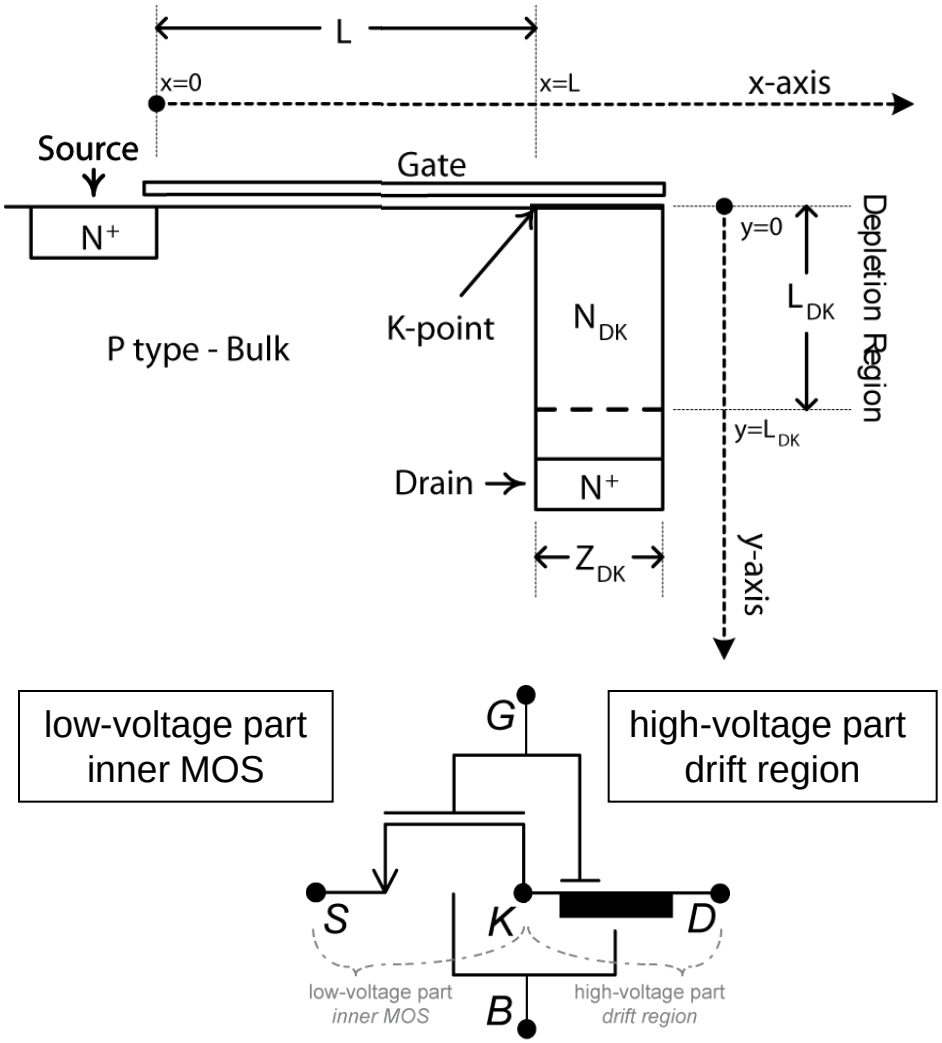


[1] Y. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. Ionescu, "**Compact Modeling of Lateral Nonuniform Doping in High-Voltage MOSFETs**," Electron Devices, IEEE Transactions on, vol. 54, no. 6, pp. 1527–1539, June 2007.

[2] A. Bazigos, F. Krummenacher, J.-M. Sallese, M. Bucher, E. Seebacher, W. Posch, K. Molnár and M. Tang, "**A physics-based analytical compact model for the Drift region of the HV-MOSFET**" Electron Devices, IEEE Transactions on, Accepted for publication, doi: 10.1109/TED.2011.2119487

From “1×2D” to “2×1D”

- HV-MOS: 2D problem
  - Split into 2 axes
  - x-axis: inner MOS
    - Source to ‘K’
  - y-axis: DRIFT region
    - ‘K’ to Drain
- Simplified HV-MOS: two 1D problems
  - Solution possible



Effects included in the model

- Low-voltage part / Inner MOS
  - Reverse Short Channel Effect
  - Lateral Non-Uniform Doping
  - Velocity Saturation
  - Mobility Reduction due to Vertical Field
  - Sub-threshold barrier lowering
- High-voltage part / DRIFT region
  - Quasi-Saturation
  - Impact Ionization Current
- Both
  - DC and CV behavior
  - Self-Heating
  - Temperature effects
  - Geometrical effects

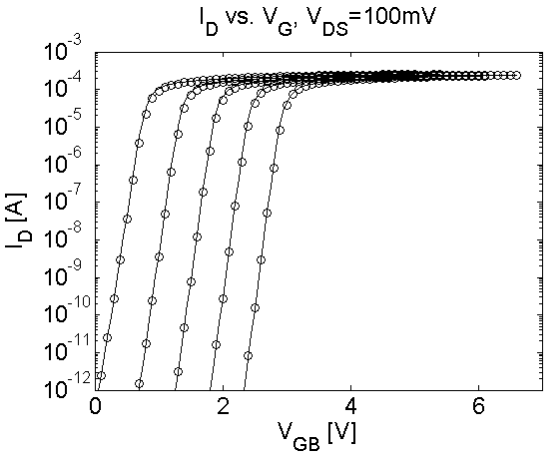
Evaluation I-V

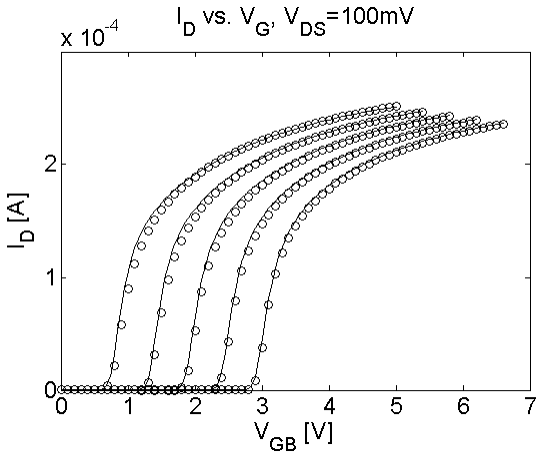
(published in [2])

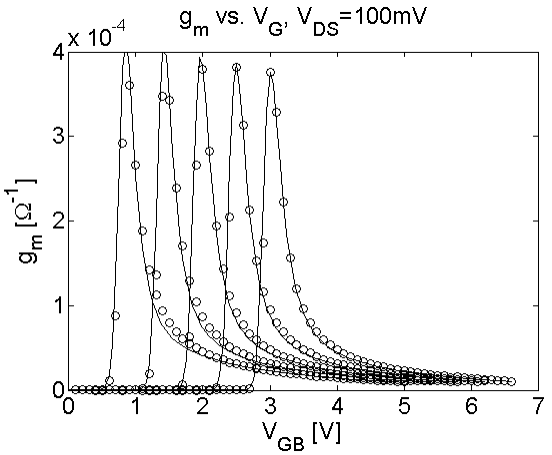
Device: LDMOS

TOX = 15nm
W = **40**µm
L = 400nm

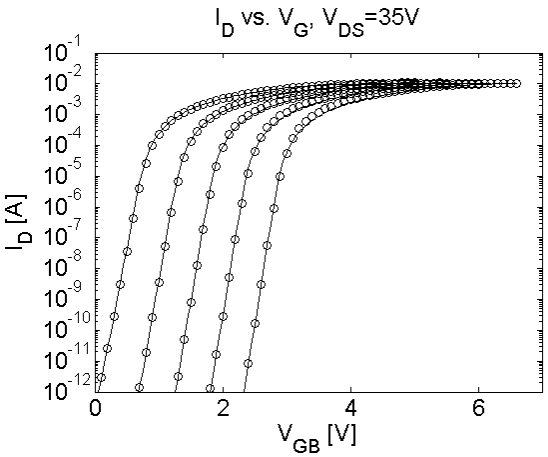
V_{DS} = 100mV

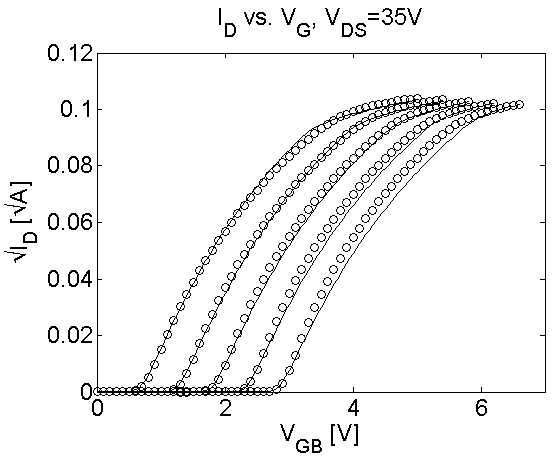


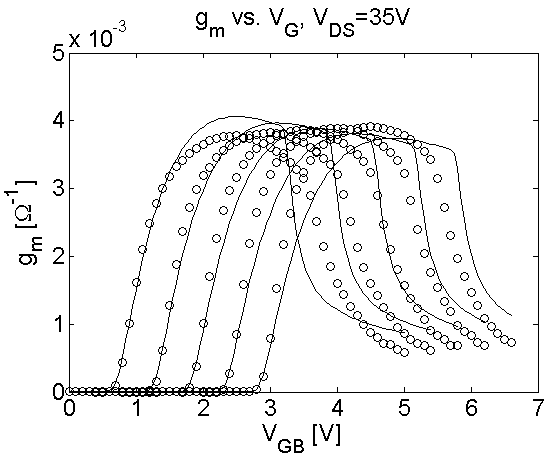




V_{DS} = 35V





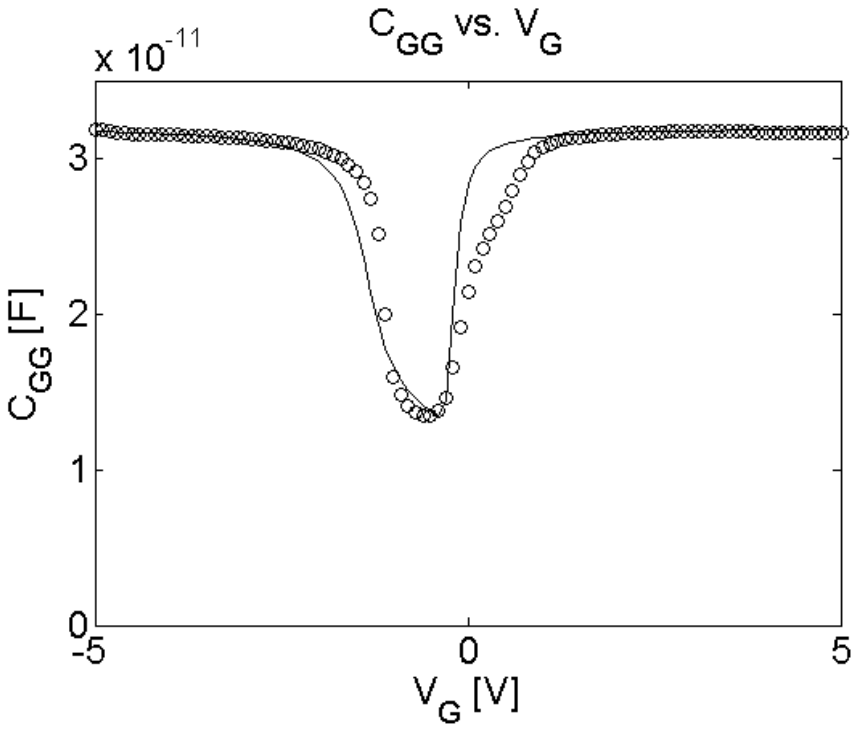


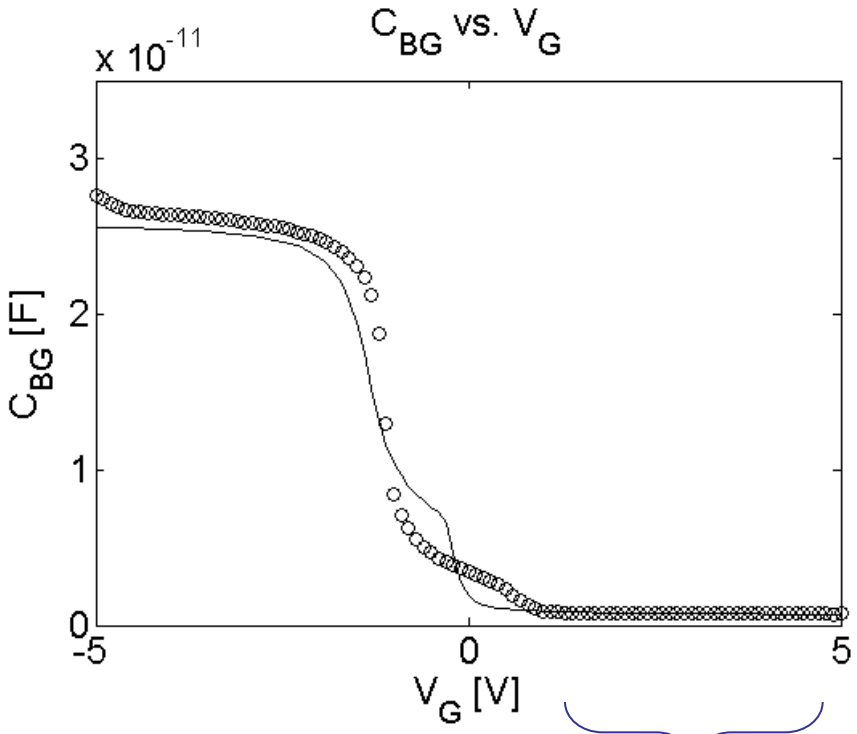
Evaluation C-V

C_{GG}, C_{GB}

Device: LDMOS

TOX = 15nm
W = **4000**µm
L = 400nm





- V_{DS} = 0V

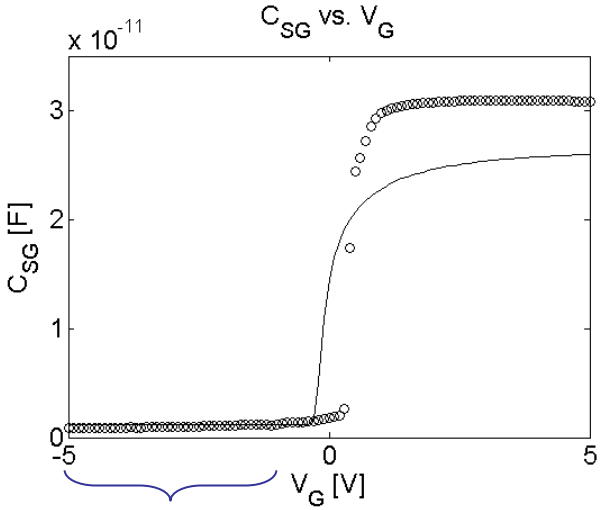
C_{GB} Overlap

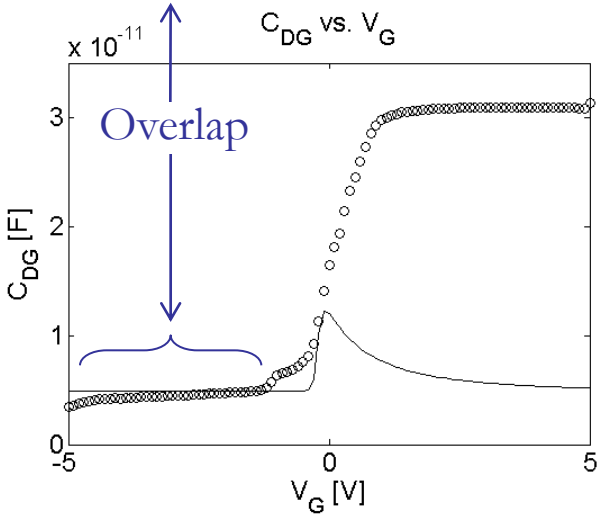
Evaluation C-V

$C_{GS} + C_{GD} = C_{GC}$

Device: LDMOS

TOX = 15nm
W = **4000**µm
L = 400nm

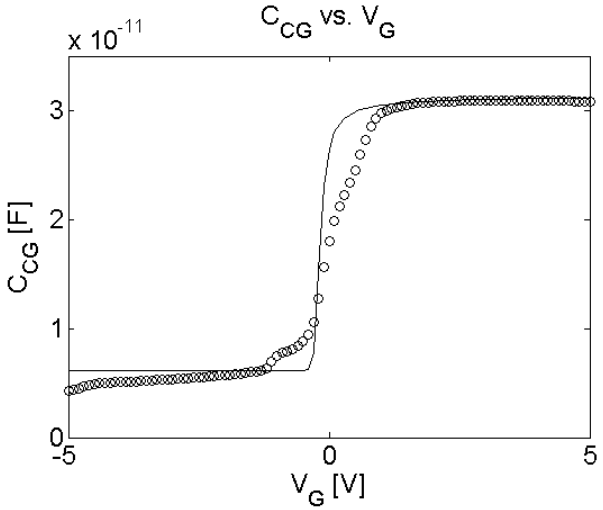




C_{GS}

+

C_{GD}



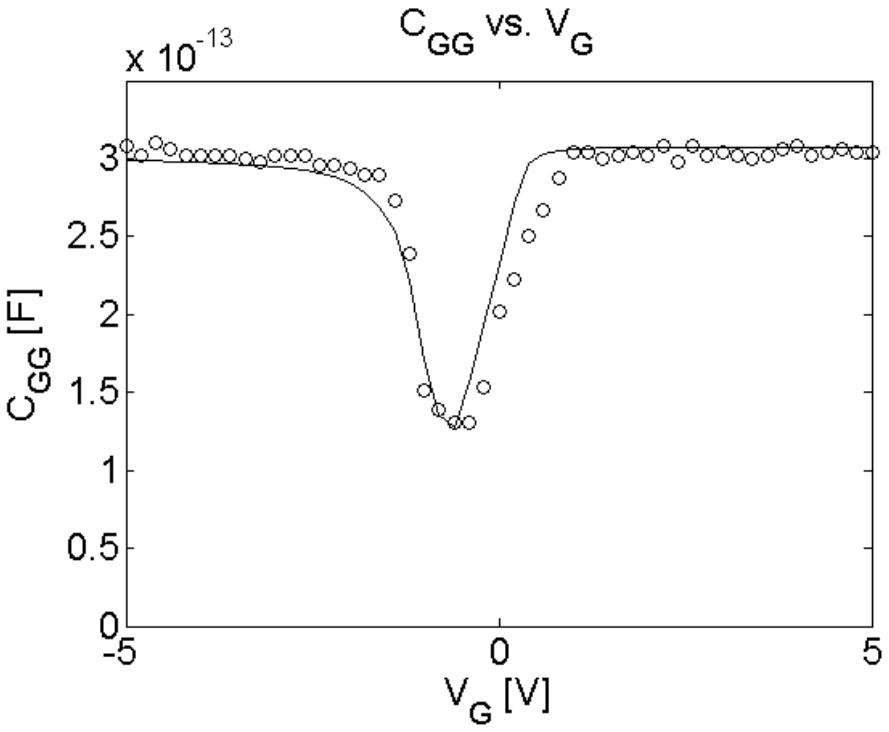
- $V_{DS} = 0V$
- "Measured" $C_{GS} = C_{GD}$ in inversion
  - Floating nodes during measurements
- Drain side overlap > Source
- "Simulated" $C_{GD} < C_{GS}$ in inversion

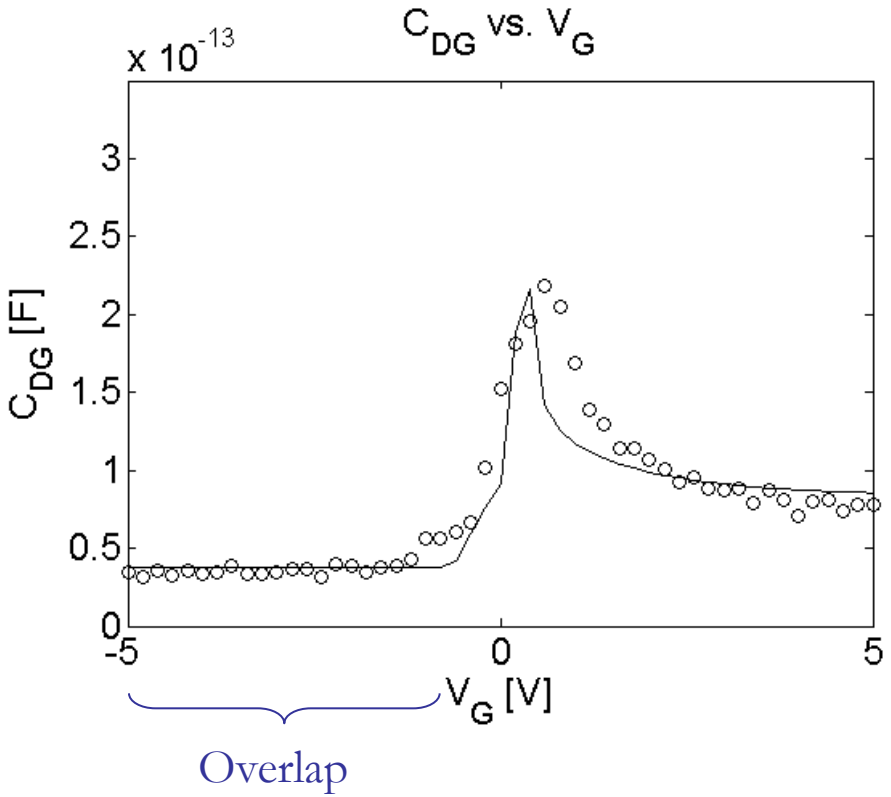
Evaluation C-V (RF)

$C_{GG} = Im(Y_{11})/2\pi f_{spot}$, $C_{GD} = Im(Y_{21})/2\pi f_{spot}$

Device: LDMOS

TOX = 15nm
W = **40**µm
L = 400nm





- $V_{DS} = 0V$
- $f_{spot} = 50MHz$

Implementation

- Verilog-A code
  - Current, under development Version: 1.105
    - Includes CV behavior
  - Released Version: 1.101 (25 May 2010)
    - Draft documentation available for v1.101
      - Includes: Parameter extraction general guidelines
  - Hierarchical structure
    - 1 main file (~800 lines)
    - 9 called-in include files (~2100 lines)
      - variables, parameters, helping and debugging functions

Parameter list

(1/2, from the draft documentation)

Name	Value	Min	Max	Short Description / Notes	Unit
Instance Parameters					
W	$40 \cdot 10^{-6}$	0	∞	Drawn device Width (Width of gate region).	m
L	10^{-6}	0	∞	Drawn device Length (Length of gate region).	m
Flags and Setup Parameters					
TYPE	1	-1	1	Channel type selector, TYPE = +1 for NMOS, TYPE = -1 for PMOS.	-
SHNET	1	0	1	Internal Self-Heating network: SHNET = 0 for Self-Heating OFF, SHNET = 1 for Self-Heating ON.	-
				Low Voltage Part	
Main Physical and Electrical Parameters					
TOX	$50 \cdot 10^{-9}$	0	∞	Gate oxide thickness. If TOX = 0 then COX is used.	m
COX	$0.7 \cdot 10^{-3}$	0	∞	Gate oxide capacitance per unit area.	F/m^2
VFB	-1.1	-∞	∞	Flat-Band voltage at source end of channel. If VFB = -10^3 then VT0 is used.	V
VT0	0.8	-∞	∞	Zero-bias Threshold voltage.	V
NSUB	10^{17}	0	∞	Bulk doping concentration at source end of channel. If NSUB = 0 then GAMMA is used.	cm^{-3}
GAMMA	0.5	0	∞	Body effect factor at source side of channel.	$V^{1/2}$
PHIF	0	0	∞	Bulk Fermi potential at source end of channel. If PHIF = 0 then NSUB or GAMMA is used for the Fermi potential calculation.	V
DVFB	0	-∞	∞	Flat-Band voltage offset between source and drain end of channel. If DVFB = -10^3 then DVT is used, but then VT0 must also be used.	V
DVT0	0	-∞	∞	Threshold voltage offset between source and drain end of channel.	V
NSUBK	10^{17}	0	∞	Bulk doping concentration at drain end of channel (K-Point). If NSUBK = 0 then GAMMAK is used.	cm^{-3}
GAMMAK	0.5	0	∞	Body effect factor at drain end of channel (K-Point).	$V^{1/2}$
PHIFK	0	0	∞	Bulk Fermi potential at drain end of channel. If PHIFK = 0 then NSUBK or GAMMAK is used for the Fermi potential calculation.	V

Name	Value	Min	Max	Short Description / Notes	Unit
Mobility Parameters					
U0	600	0	∞	Low-field mobility. If U0 = 0 then KP is used.	cm^2/Vs
KP	0	0	∞	Low-field transconductance factor.	A/V^2
Mobility Reduction due to Vertical Field					
E0	$150 \cdot 10^6$	1	∞	1st-order mobility reduction characteristic field.	V/m
E1	$200 \cdot 10^6$	1	∞	2nd-order mobility reduction characteristic field.	V/m
ETA	0.6	0	1	Q_b vs. Q_i weight coefficient for the vertical field calculation.	-
Bias Dependence and Length Scaling of Equivalent Pinch-Off Voltage Gradient					
DGC1	0.25	0	1	Bulk doping gradient 1st-order inversion scaling coefficient.	-
DGC2	0	0	1	Bulk doping gradient 2nd-order inversion scaling coefficient.	-
DGE	0.5	0	1	Bulk doping gradient length scaling exponent.	-
Non-Uniform Doping Length Scaling Factor for Intermediate and Long Channel Devices					
LDG	10^{-6}	10^{-9}	∞	Bulk doping gradient characteristic length.	m
Geometrical Parameters (Short and Narrow Channel Corrections)					
DL	0	0	∞	Length offset of gate oxide region.	m
DW	0	0	∞	Width offset of gate oxide region.	m
DWD	0	0	∞	Width offset of drift region.	m
Reverse Short Channel Effect					
LR	$0.1 \cdot 10^{-6}$	0	∞	Reverse short channel characteristic length.	m
QLR	0	-∞	∞	Reverse short channel Threshold voltage coefficient.	C/m^2
NLR	0	-∞	∞	Reverse short channel body effect coefficient.	F/m^2
Subthreshold Barrier Lowering					
ETAS	0.5	0	2	Subthreshold barrier lowering characteristic length coefficient.	-
SIGMAS	0.1	0	2	Subthreshold barrier lowering body bias coefficient.	-
ALPHAS	1	0	5	Subthreshold barrier lowering smoothing coefficient.	-
BETAS	0.1	0	1	Subthreshold barrier lowering scaling factor.	-
Velocity Saturation					
VSAT	0	0	∞	Saturation velocity. If VSAT = 0 then UCRIT is used.	m/s
UCRIT	$3 \cdot 10^{-6}$	1	∞	Longitudinal critical field.	V/m
Channel Length Modulation					
LAMBDA	0	0	∞	Lambda factor for channel length modulation.	-
LC	$30 \cdot 10^{-9}$	0	∞	Characteristic length for channel length modulation.	m

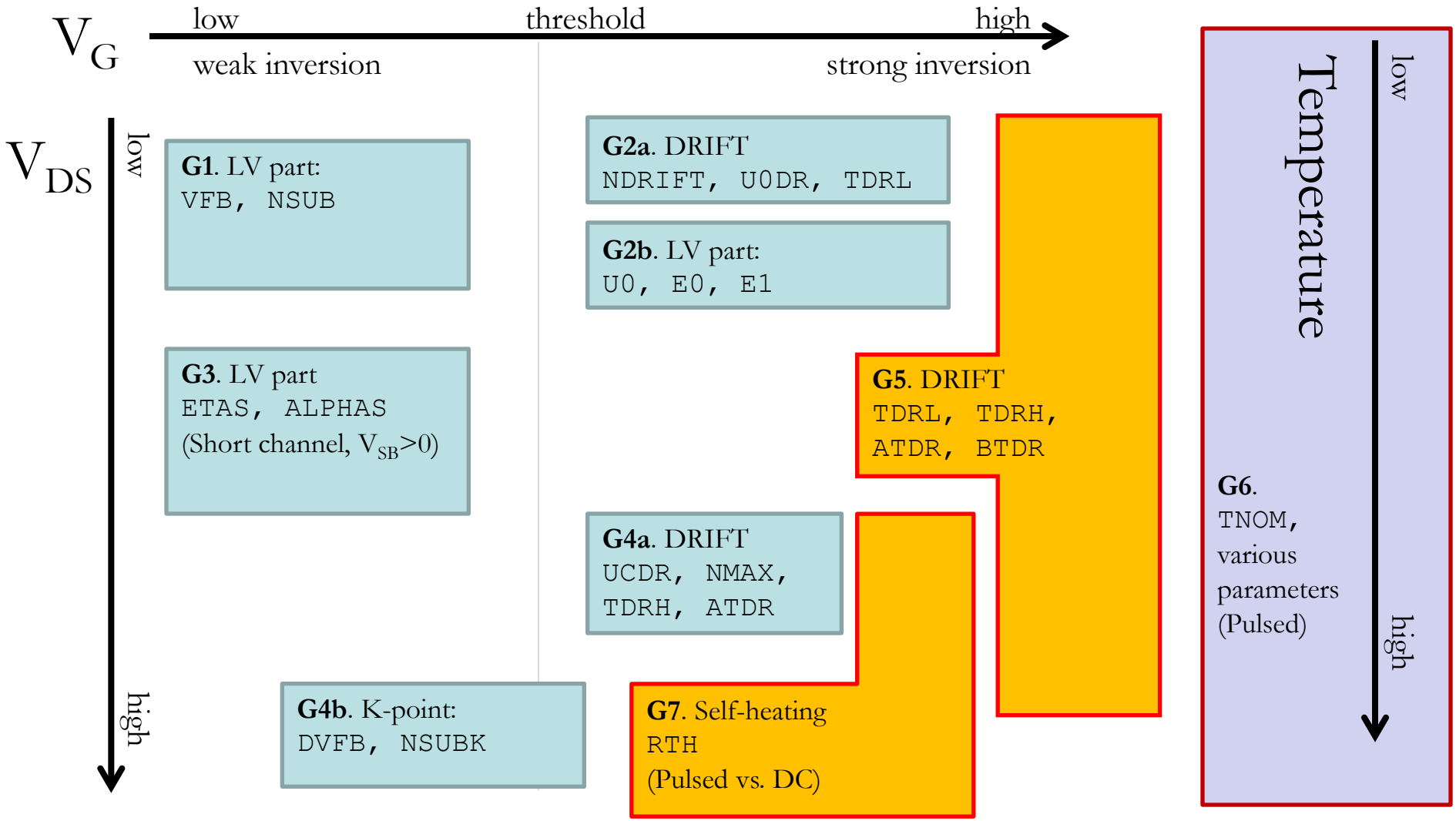
Parameter list

(2/2, from the draft documentation)

Name	Value	Min	Max	Short Description / Notes	Unit
				Drift Region	
Geometrical Parameters					
LDR	$4 \cdot 10^{-6}$	0	∞	Length of depleted drift region.	m
TDRL	$0.8 \cdot 10^{-6}$	0	∞	Current flow thickness in drift region at low V_{DS}.	m
TDRH	$0.5 \cdot 10^{-6}$	0	∞	Current flow thickness in drift region at high V_{DS}.	m
TDRLS	0	-∞	∞	Low V_{DS} body bias sensitivity of drift current flow thickness.	1/V
TDRHS	0	-∞	∞	High V_{DS} body bias sensitivity of drift current flow thickness.	1/V
Gate Overlap Length Over The Drift Region (used in AC behaviour)					
LOVD	0	0	∞	Thin oxide gate extension over drift region.	m
Charge-Sheet Accumulation Layer Thickness (used in AC behaviour)					
DACC	$20 \cdot 10^{-9}$	10^{-9}	LDR	Charge-sheet accumulation layer thickness.	m
Main Physical and Electrical Parameters					
NDRIFT	$5 \cdot 10^{16}$	0	∞	Drift region doping concentration. If NDRIFT = 0 then GAMMAD is used.	cm^{-3}
GAMMAD	0	0	∞	Drift region modulation factor.	$V^{1/2}$
PHIFD	0	0	∞	Drift region Fermi potential. If PHIFD = 0 then NDRIFT or GAMMAD is used for the Fermi Potential calculation.	V
Mobility Parameters					
U0DR	600	0	∞	Drift region low-field mobility. If U0DR = 0 then KPDR is used.	$cm^2/V s$
KPDR	0	0	∞	Drift region low-field transconductance factor.	A/V^2
Velocity Saturation					
VSATDR	0	0	∞	Saturation velocity in drift. If VSATDR = 0 then UCDR is used.	m/s
UCDR	$3 \cdot 10^6$	1.0	∞	Longitudinal critical field in drift region.	V/m
Quasi-Saturation					
ATDR	1	0	∞	Quasi-saturation smoothing factor.	-
BTDR	0.3	0	∞	Quasi-saturation fine-tuning coefficient.	-
Maximum Doping at the Drain Side					
NMAX	10	0	∞	Maximum relative carrier concentration in the drift.	-

Name	Value	Min	Max	Short Description / Notes	Unit
Impact Ionization Current					
IBA	0	0	∞	First impact ionization coefficient.	1/m
IBB	$50 \cdot 10^6$	10^6	∞	Second impact ionization coefficient.	V/m
IBN	1	0	∞	Saturation voltage factor for impact ionization.	-
IBH1	1	0	∞	High-current roll-off factor for impact ionization.	-
IBH2	1	0	∞	High-current roll-off exponent for impact ionization.	-
Self-Heating					
RTH	0	0	∞	Thermal resistance at zero injected power.	°C/W
CTH	0	0	∞	Thermal capacitance.	s·W/°C
Temperature Parameters					
TNOM	27	-273.15	∞	Reference temperature.	°C
TCVT0	0	-∞	:∞	Temperature coefficient of threshold voltage (VT0).	V/°C
TCDVT0	0	-∞	∞	Temperature coefficient of threshold voltage offset between source and drain end of channel (DVT0).	V/°C
TCVFB	0	-∞	∞	Temperature coefficient of Flat-Band Voltage (VFB).	V/°C
TCDVFB	0	-∞	∞	Temperature coefficient of Flat-Band Voltage offset between source and drain end of channel (DVFB).	V/°C
TCRTH	0	-1	1	Temperature coefficient of RTH.	$°C^{-1}$
BEX	-1.5	-∞	∞	Mobility temperature exponent (U0).	-
BDREX	-1.5	-∞	∞	Drift region mobility temperature exponent (U0DR).	-
UCEX	1.5	-∞	∞	Longitudinal critical field temperature exponent (UCRIT).	-
UCDREX	1	-∞	∞	Drift region longitudinal critical field temperature exponent (UCDR).	-
E0EX	0	-∞	∞	Temperature exponent for E0.	-
E1EX	0	-∞	∞	Temperature exponent for E1.	-
TCNMAX	0	-1	1	Temperature coefficient of NMAX.	$°C^{-1}$
TCETAS	0	-1	1	Temperature coefficient of ETAS.	$°C^{-1}$
TCTDRL	0	-1	1	Temperature coefficient of TDRL.	$°C^{-1}$
TCTDRH	0	-1	1	Temperature coefficient of TDRH.	$°C^{-1}$
TCATDR	0	-1	1	Temperature coefficient of ATDR.	$°C^{-1}$
TCBTDR	0	-1	1	Temperature coefficient of BTDR.	$°C^{-1}$
IBBT	0	-1	1	Temperature coefficient of IBB.	$°C^{-1}$

Parameter Extraction Guidelines



Next Steps

- Finalization of the CV model
  - Study of CV via RF measurements with positive V_{DS}
  - Preparation of publication on the CV model
  - Release of the next version of the model
- Update of the documentation
  - Parameter extraction procedure
- Transient analysis
- RF model
  - NQS behaviour

References

[1] Y. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. Ionescu, "**Compact Modeling of Lateral Nonuniform Doping in High-Voltage MOSFETs**," Electron Devices, IEEE Transactions on, vol. 54, no. 6, pp. 1527–1539, June 2007.

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[3] A. Bazigos, F. Krummenacher, J.-M. Sallese, "**Recent Developments on the EPFL - High Voltage MOSFET Model (EPFL-HVMOS)**", Poster Presentation at MOS-AK/GSA ESSDERC/ESSCIRC Workshop 2010, Sept. 17, Seville

[4] Yogesh Singh Chauhan, "**Compact modeling of high voltage MOSFETs**", Thèse EPFL, no 3915 (2007).

[5] Costin Anghel, "**High voltage devices for standard MOS technologies: characterisation and modelling**", Thèse EPFL, no 3116 (2004).

[6] W. Grabinski and T. Gneiting, (Eds.) "**POWER/HVMOS Devices Compact Modeling**", 1st Edition. 2010, Springer, ISBN: 978-90-481-3045-0

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