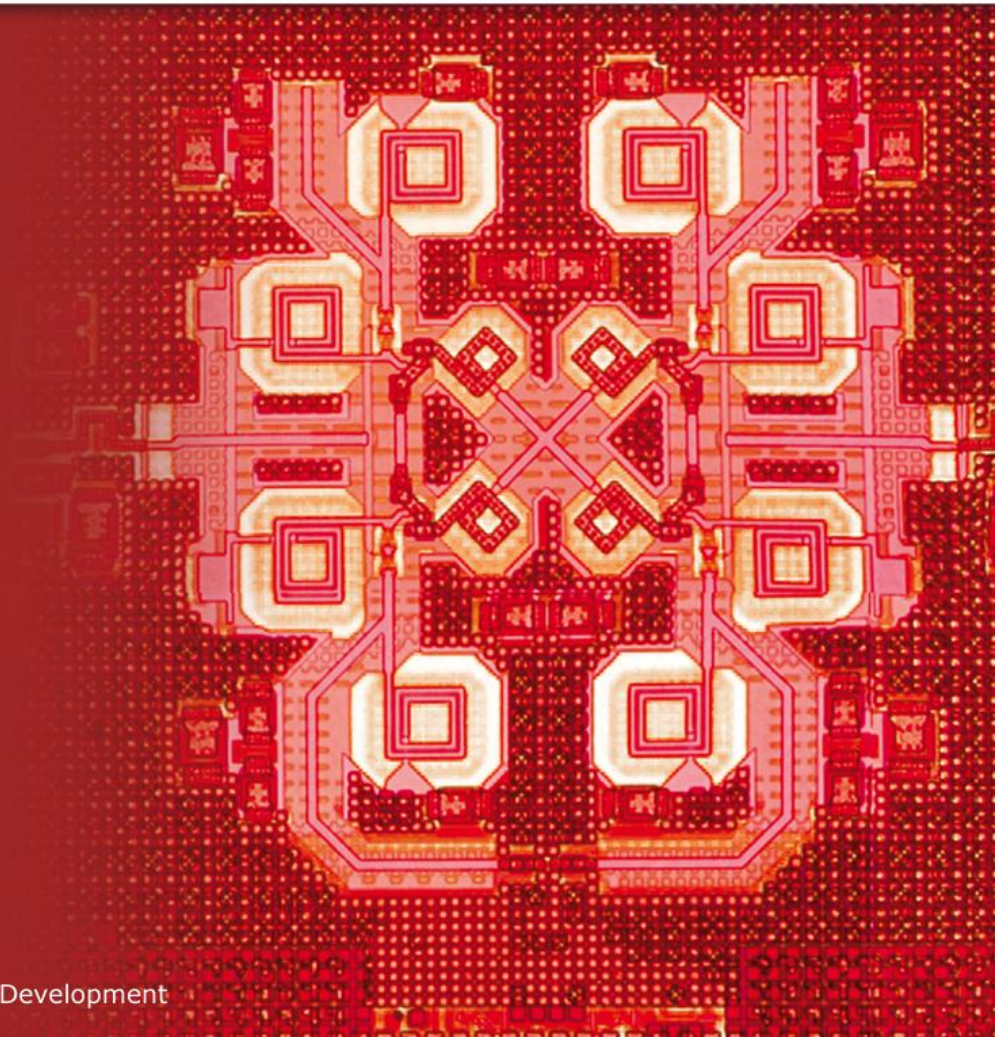
Investigation of De-embedding procedures up to 110GHz



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Outline

- Introduction
- Calibration
- De-embedding steps
  - OPEN-SHORT
  - 3 steps
  - 4 steps
  - 5 steps
  - 6 steps
- Two-step de-embedding
- Conclusion

Introduction

- Deembedding importance:
  - For process engineers (technology performance f_T, f_{max})
  - Highly important for compact device modeling
  - S parameter perfectly corrected

- Main issues
  - What is an accurate deembedding technique?

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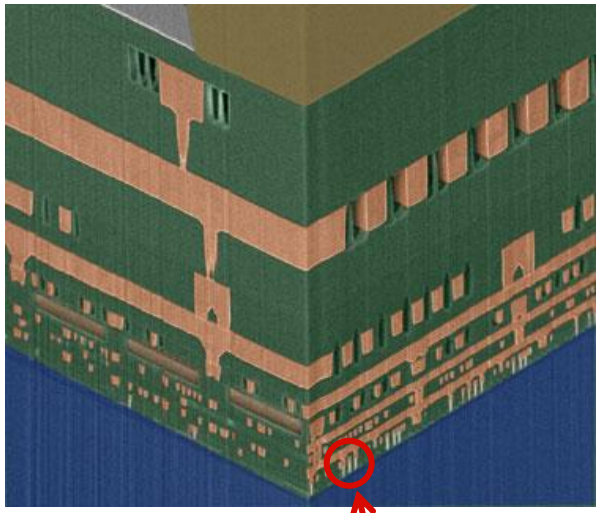
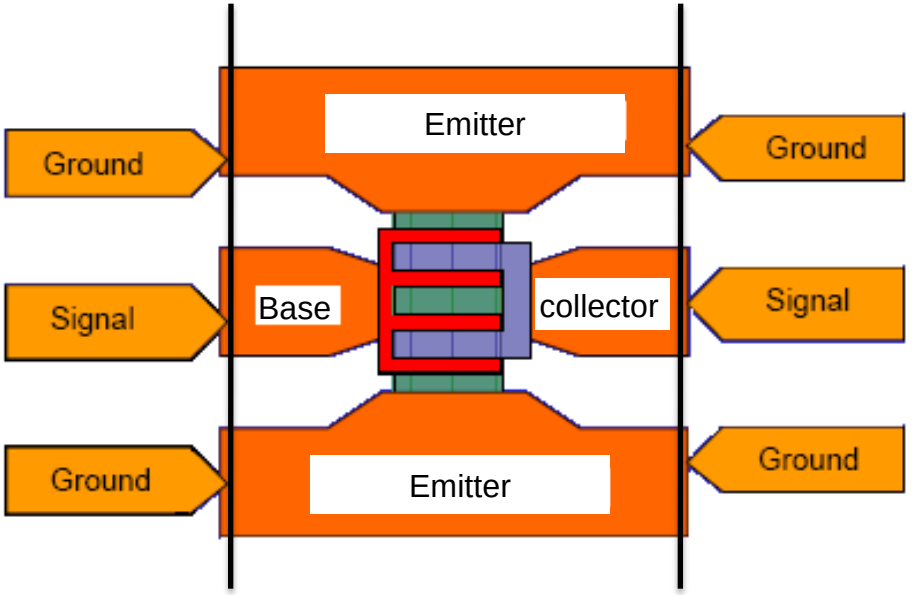
Calibration

- Takes into account parasitic between VNA and Probe tips
- After calibration the reference planes are at the probe tips



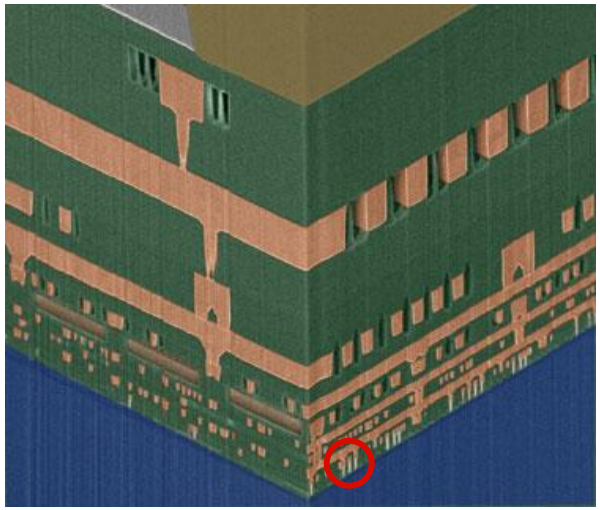
Source: IBM IEEE Spectrum

DUT



De-embedding

- Retrieve intrinsic device performance → de-embedding
- How?!!



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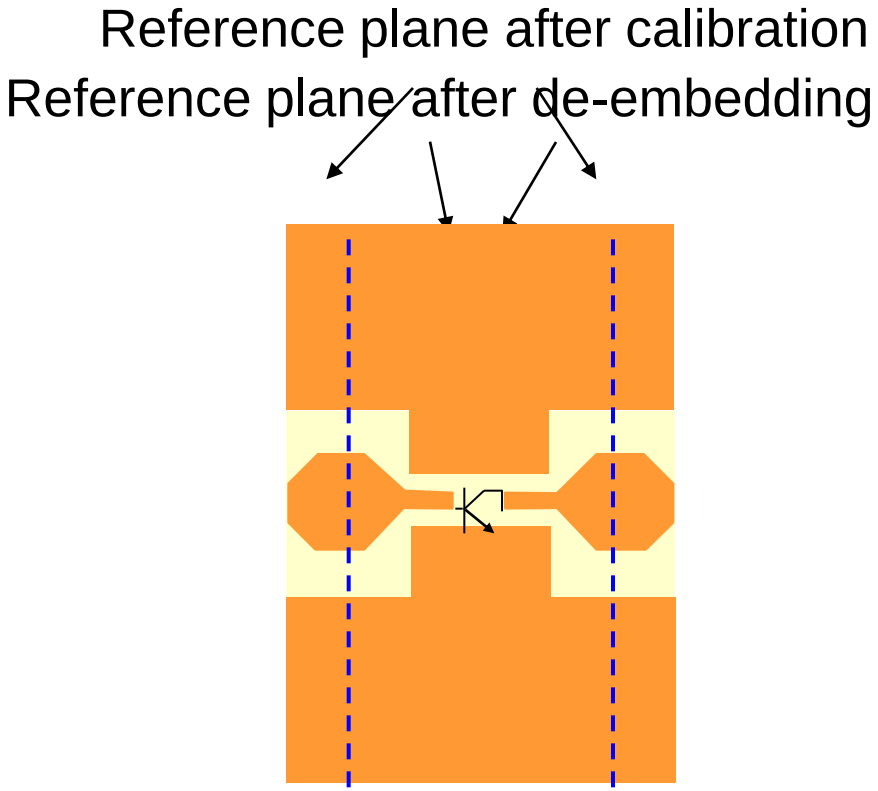

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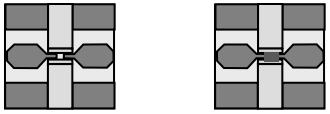
De-embedding steps

- Open-Short

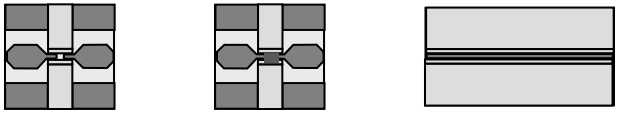
Open Short



*Koolen, Bipolar Circuits and Technology Meeting, Sep. 1991

- 3 Steps

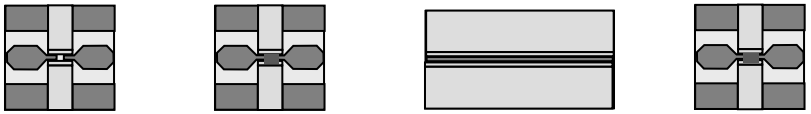
Open Short Line



*H. Cho and al., IEEE Trans. Electron Devices, June 1991

- 4 Steps

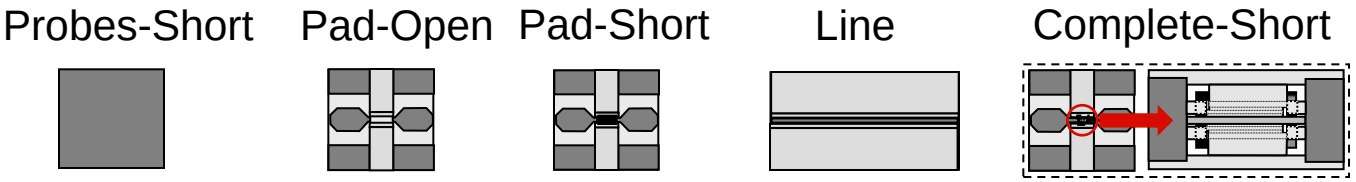
Open Short Line Short



* T.E.Kolding, IEEE Trans. Electron Devices, April 2000

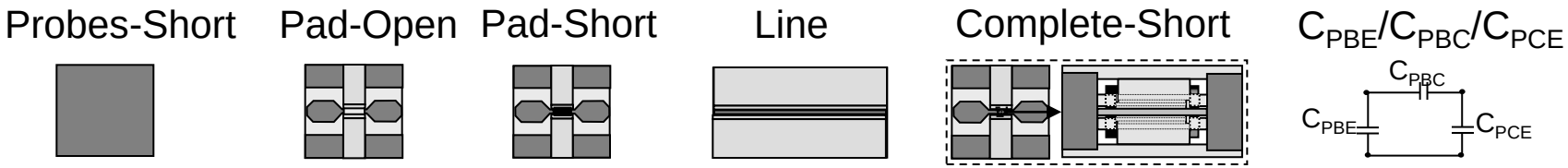
De-embedding steps

- 5 Steps



* F. Pourchon et al, BCTM 08, Invited talk

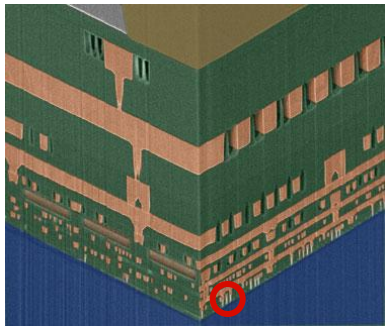
- 6 Steps



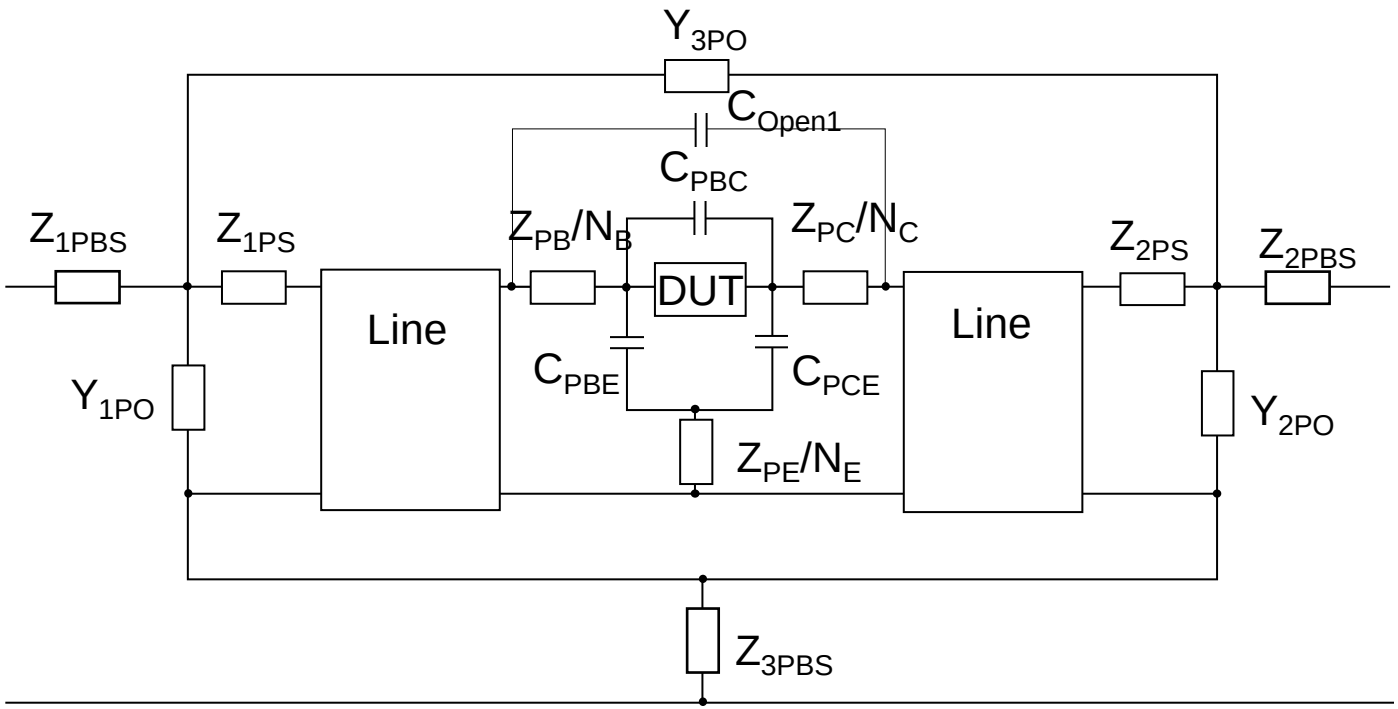
* C. Raya et al, HICUM Workshop 08

De-embedding Steps

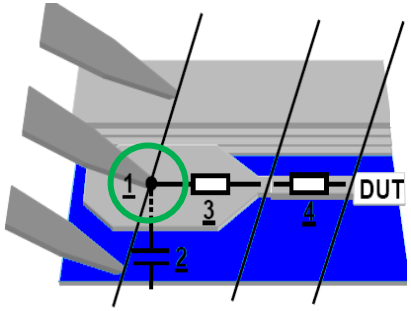
- 5 de-embedding steps

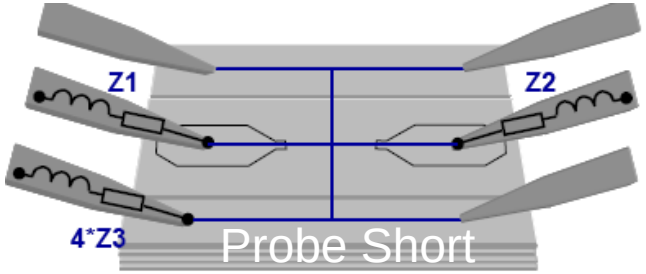


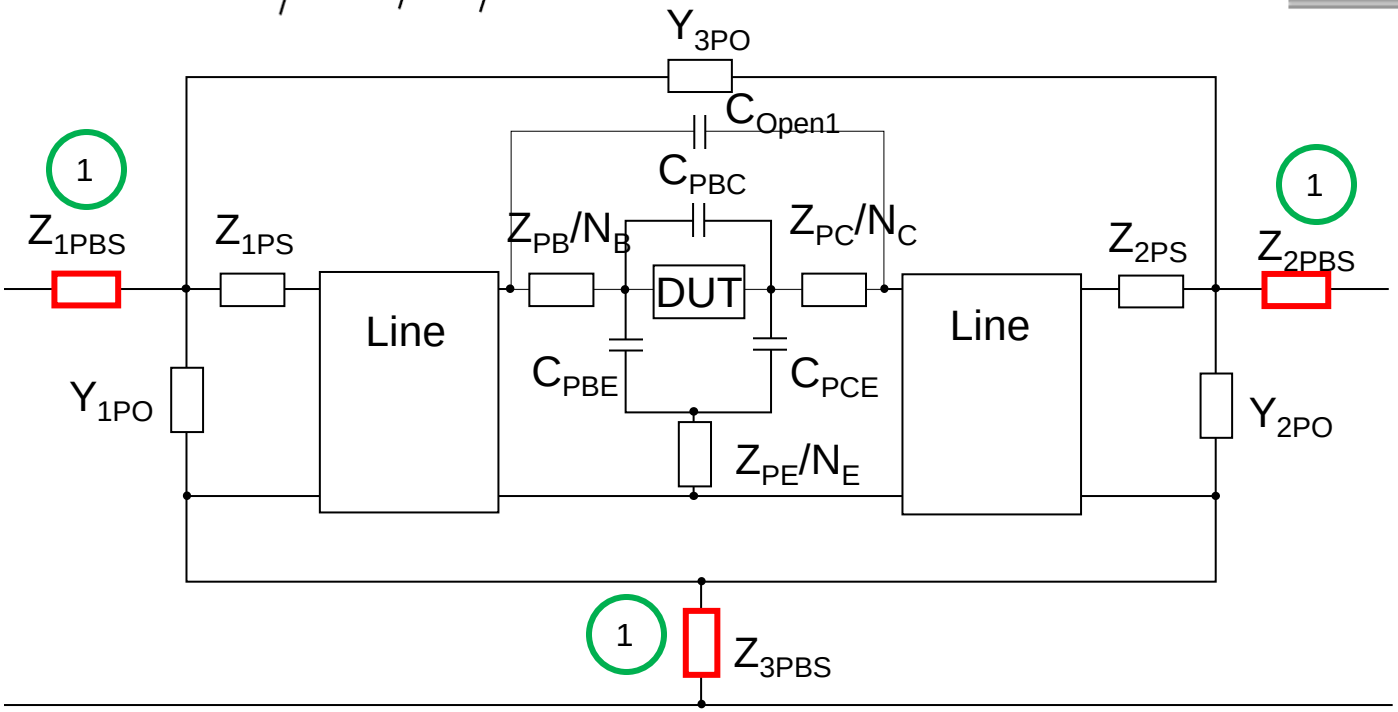
Source: IBM IEEE Spectrum



De-embedded equivalent circuit (1): Probe Short

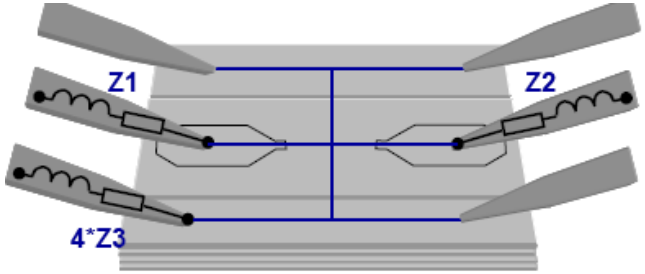


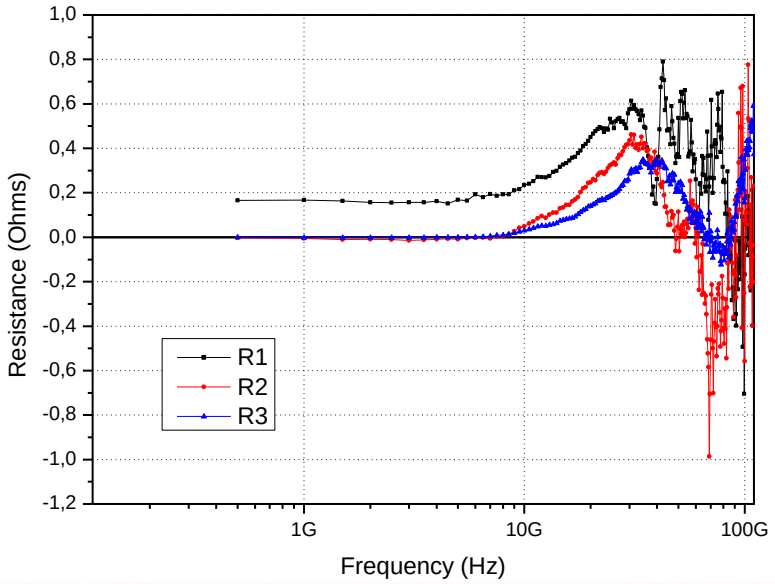


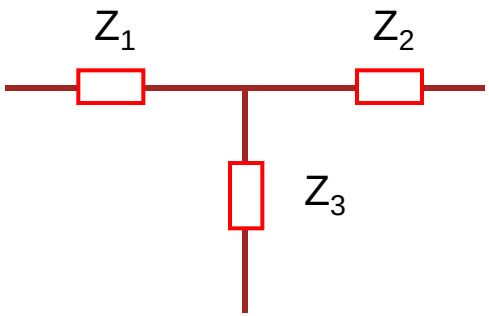


Results

- Probe short:
  - short circuit for the probes
  - Correct the probe contact resistance

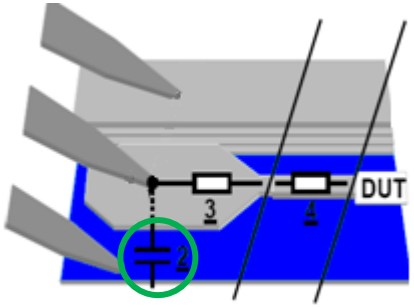


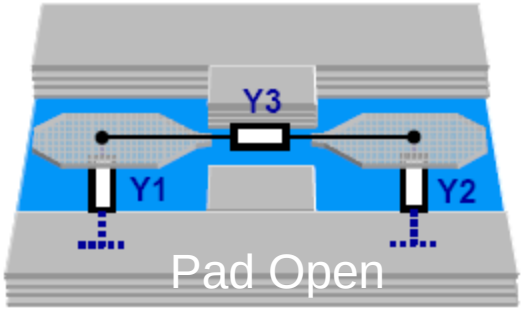


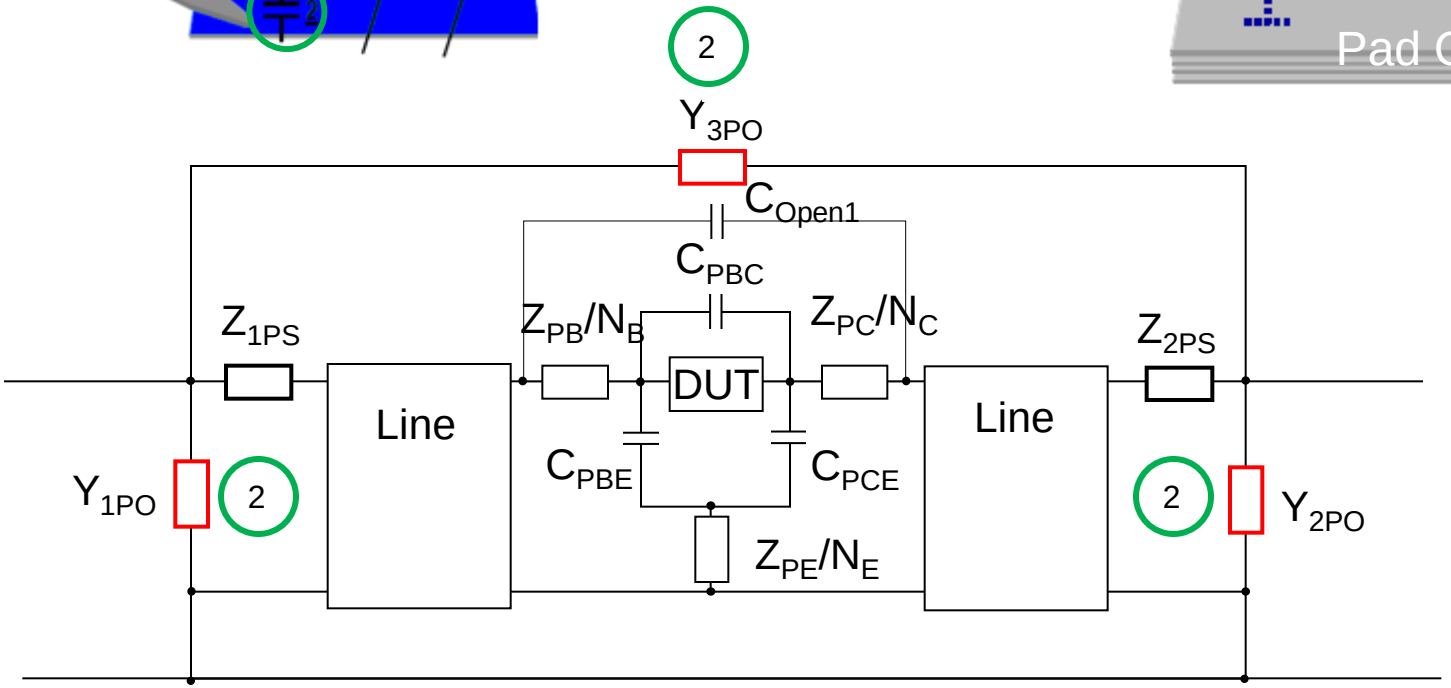


Attention: probe contact problem at Port 1
Manual probing !!!

De-embedded equivalent circuit (2): Pad Open

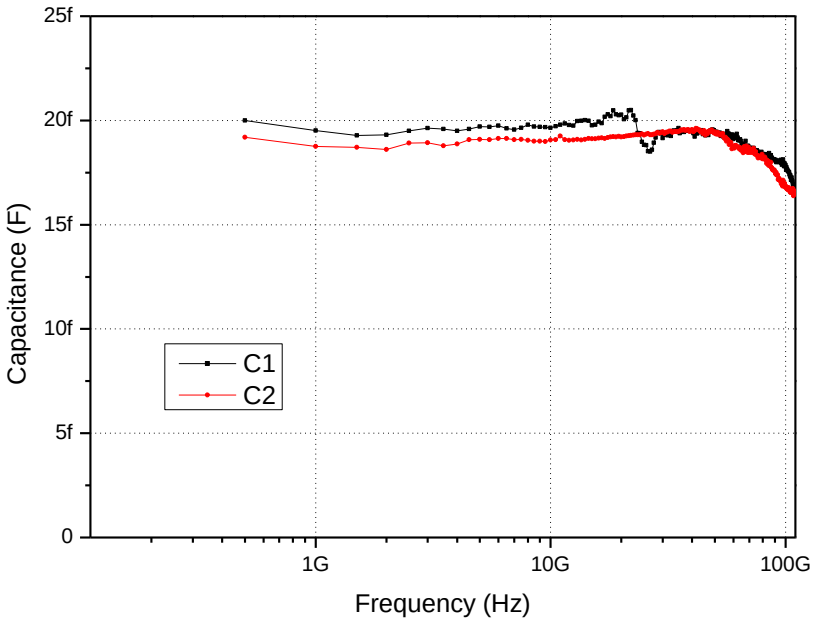




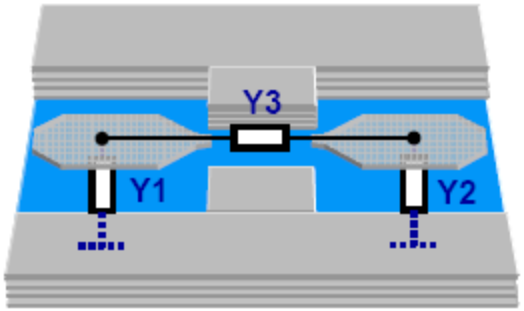


De-embedded equivalent circuit (2): Pad Open

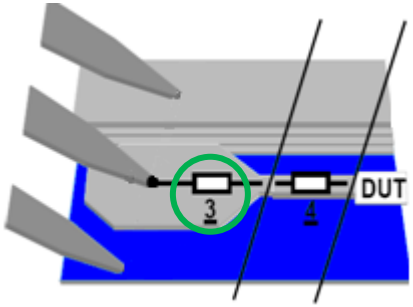
- Pad capacitance

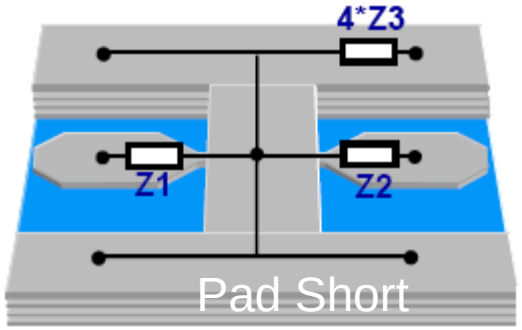


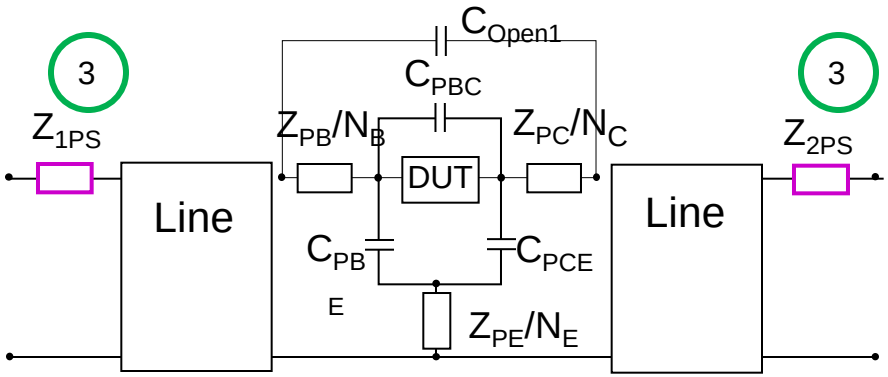
- Equivalent circuit (2)



De-embedded equivalent circuit (3): Pad Short

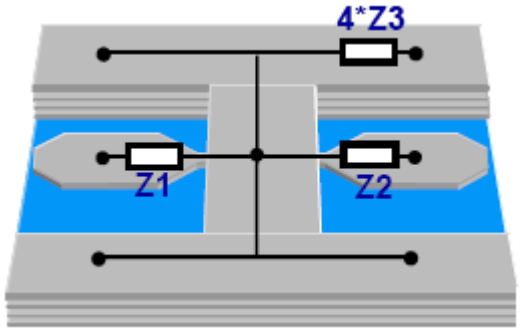


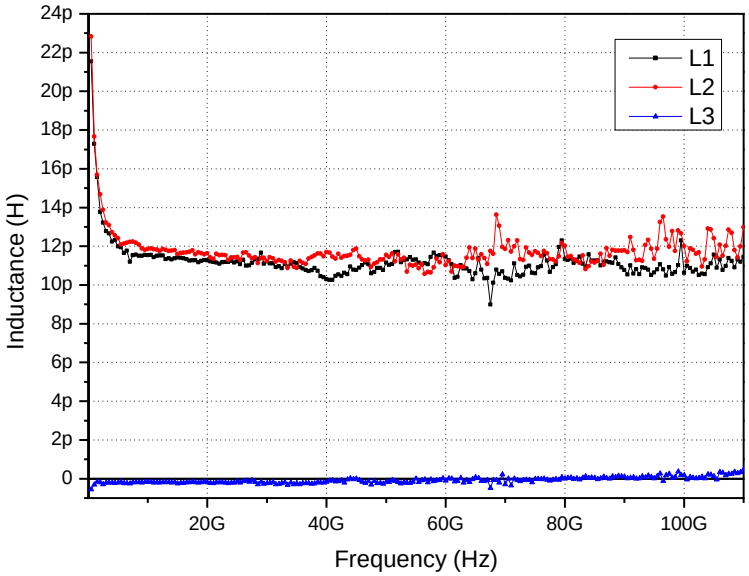


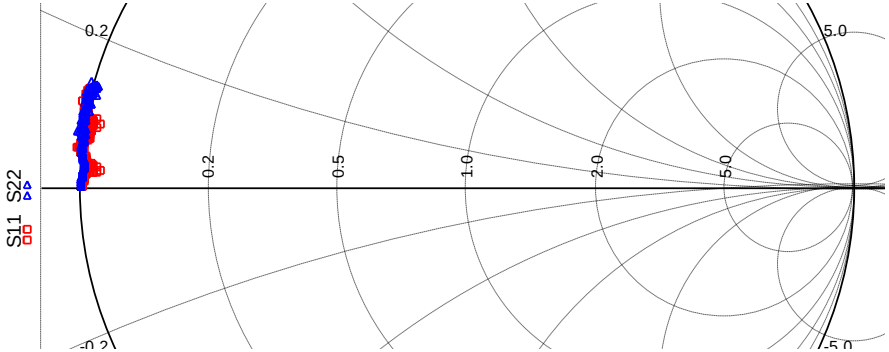


De-embedded equivalent circuit (3): Pad Short

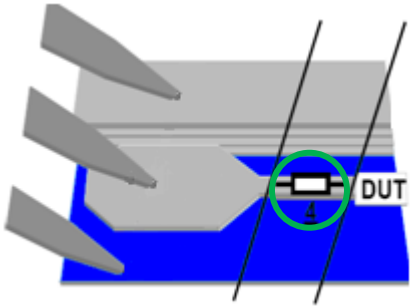
- Pad short:
  - short circuit at the edge of the signal pad.

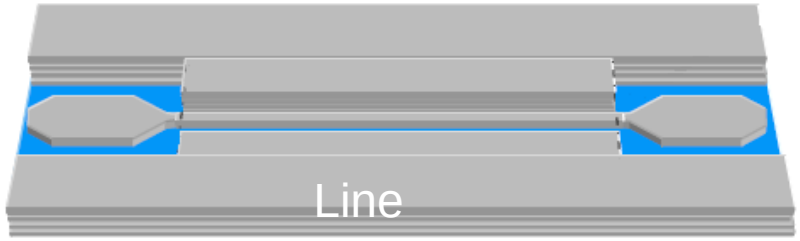


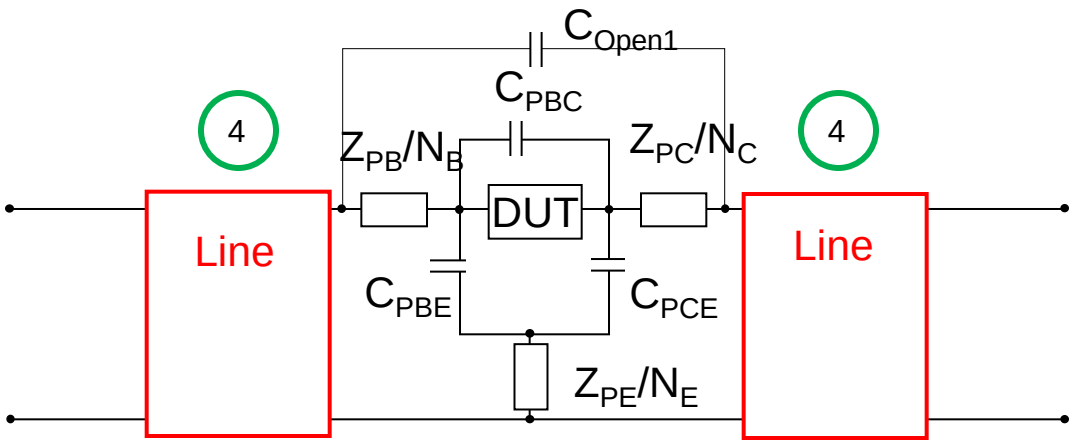




De-embedded equivalent circuit (4): Line scalable

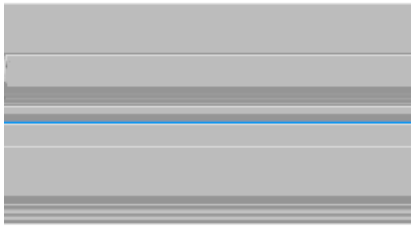




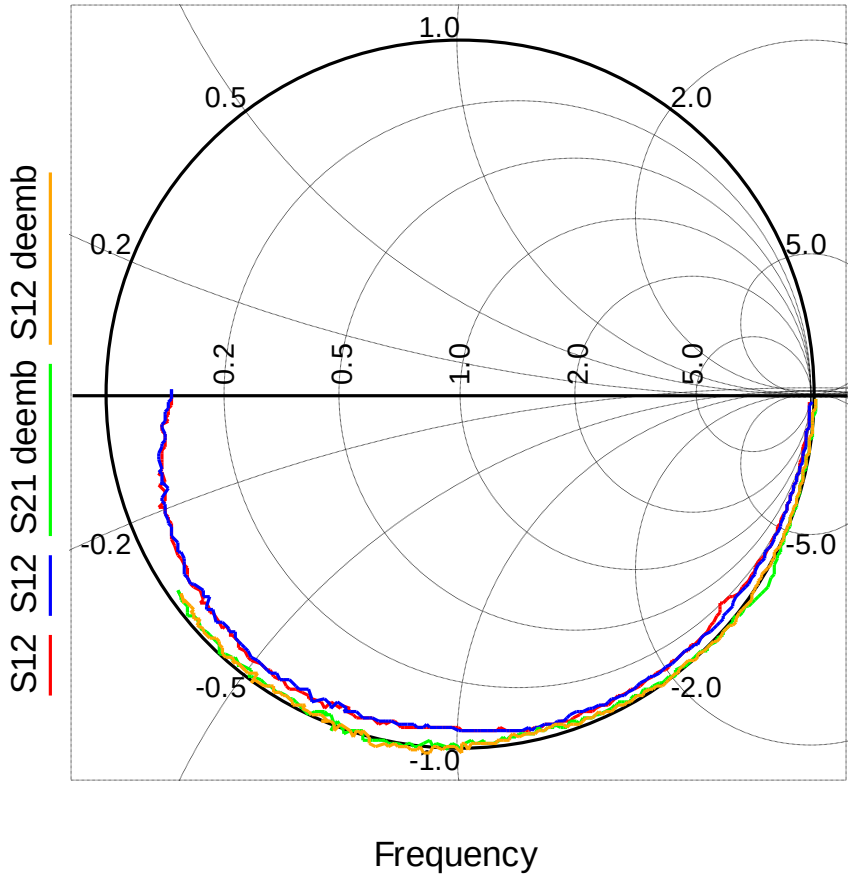


De-embedded equivalent circuit (4): Line scalable

- First: measure and de-embed a long line:

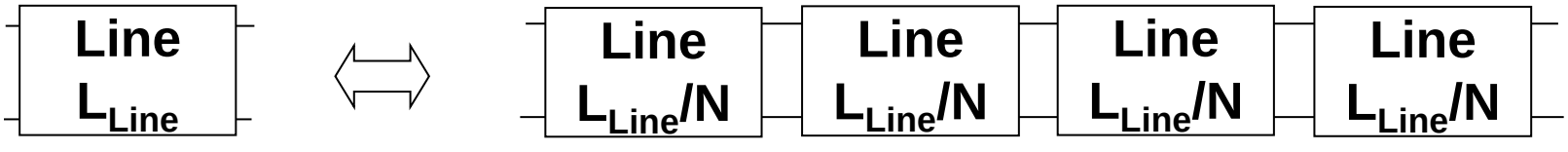


Line de-embedding



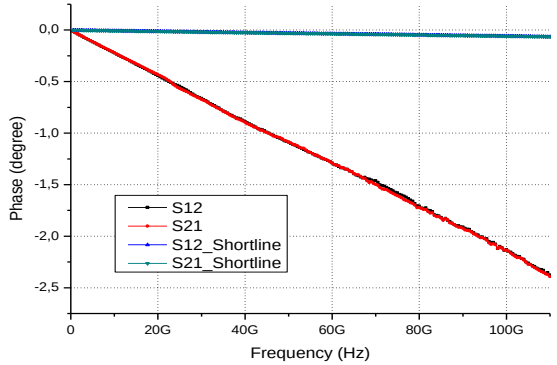
Re-dimensioning the line

N=4

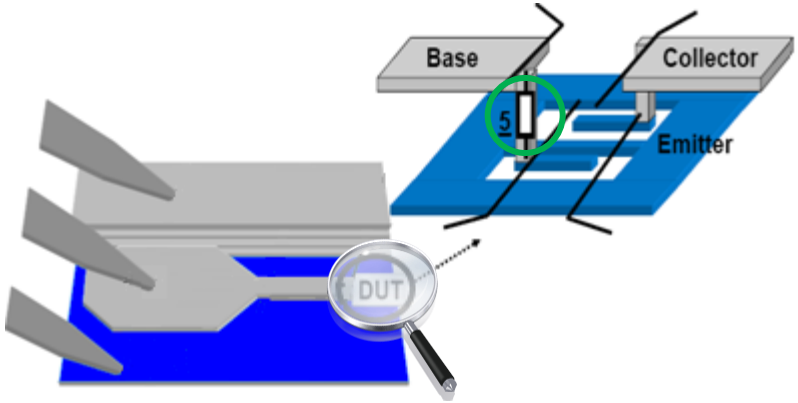


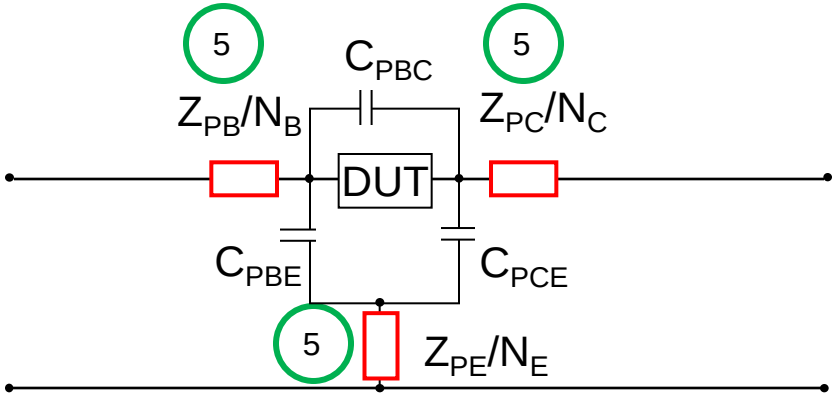
$$T = a + d \quad K = a - d \quad \Delta = K^2 + 4bc \quad \delta = \sqrt{\Delta} \text{ si } \Delta \geq 0 \text{ ou } \delta = i\sqrt{|\Delta|} \text{ si } \Delta < 0 \qquad n = L_1 / L_{Line}$$

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix}^n = \frac{1}{\delta} \cdot \begin{bmatrix} \frac{(\delta+K)(T+\delta)^n + (\delta-K)(T-\delta)^n}{2^{n+1}} & b\left(\frac{(T+\delta)^n - (T-\delta)^n}{2^n}\right) \\ c\left(\frac{(T+\delta)^n - (T-\delta)^n}{2^n}\right) & \frac{(\delta-K)(T+\delta)^n + (\delta+K)(T-\delta)^n}{2^{n+1}} \end{bmatrix}$$

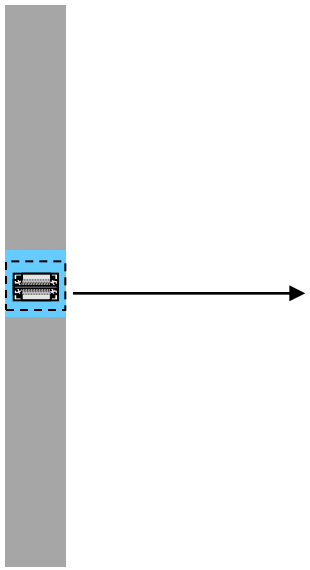


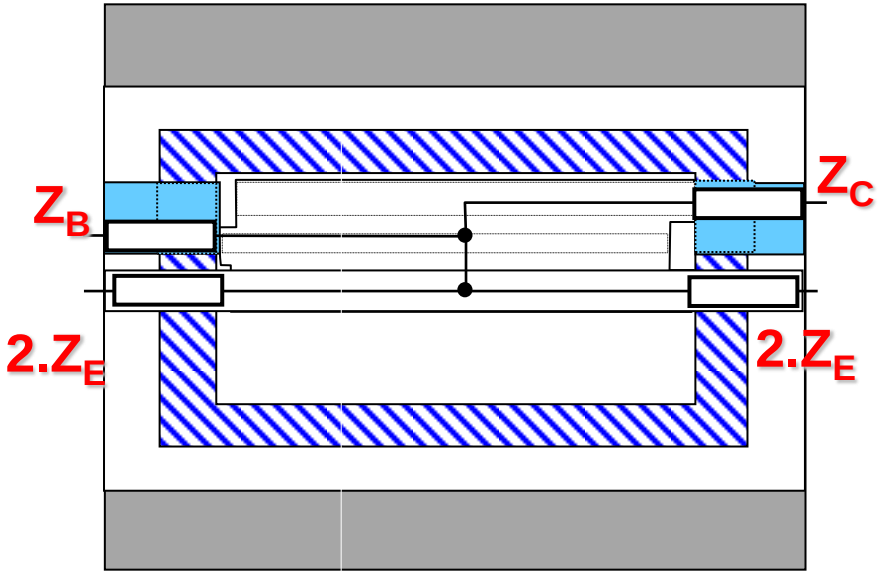
De-embedded equivalent circuit (5): Complete short

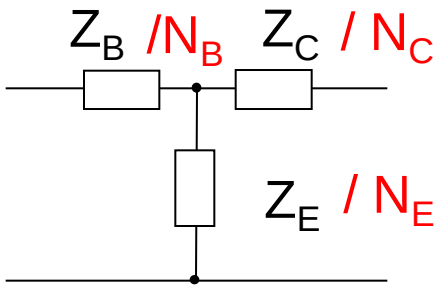




De-embedded equivalent circuit (5): Complete short

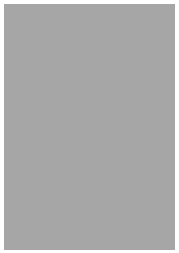




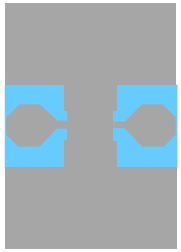


Z_B: Base impedance
Z_C: Collector impedance
Z_E: Emitter impedance

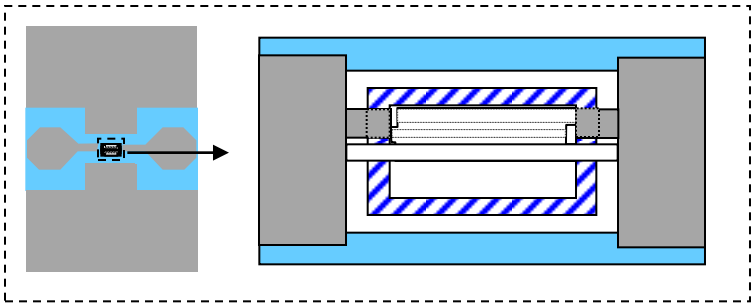
The three shorts:



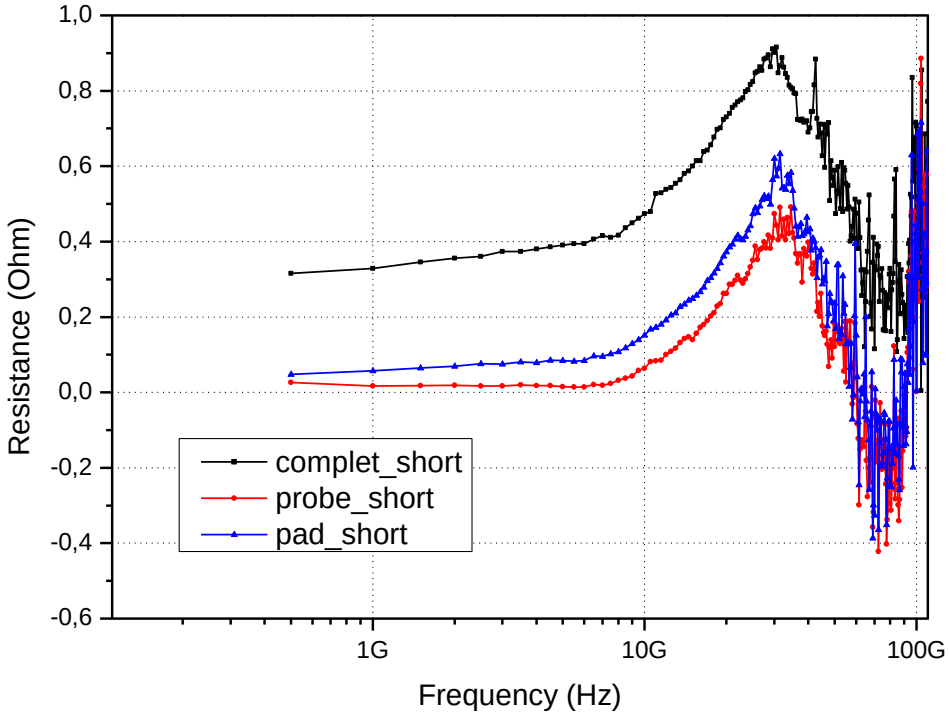
Probes-Short



Pad-Short

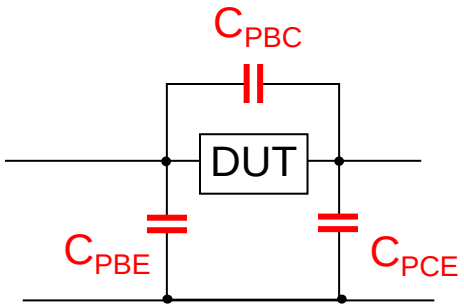


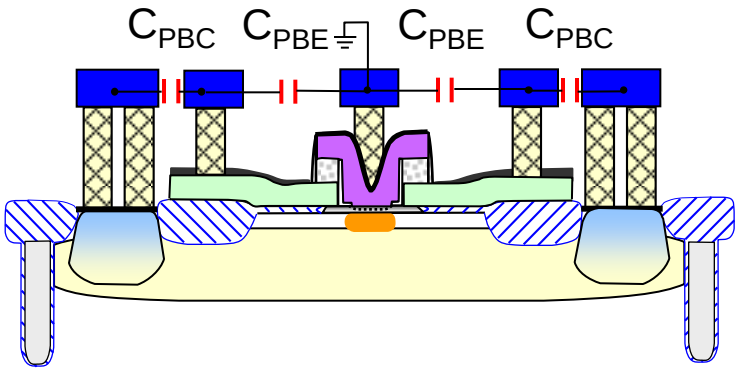
Complete Short

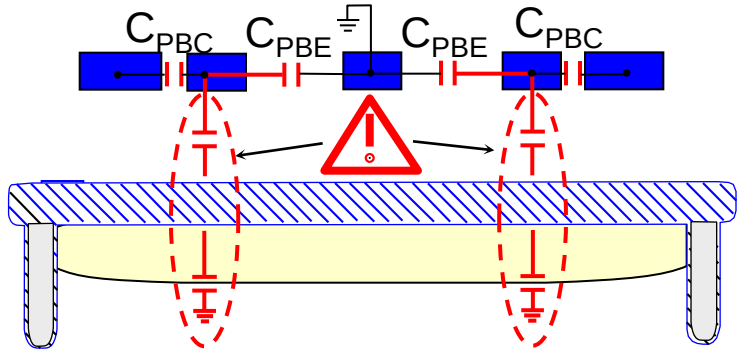


De-embedded equivalent circuit (6): Capacitances

- 6 de-embedding steps





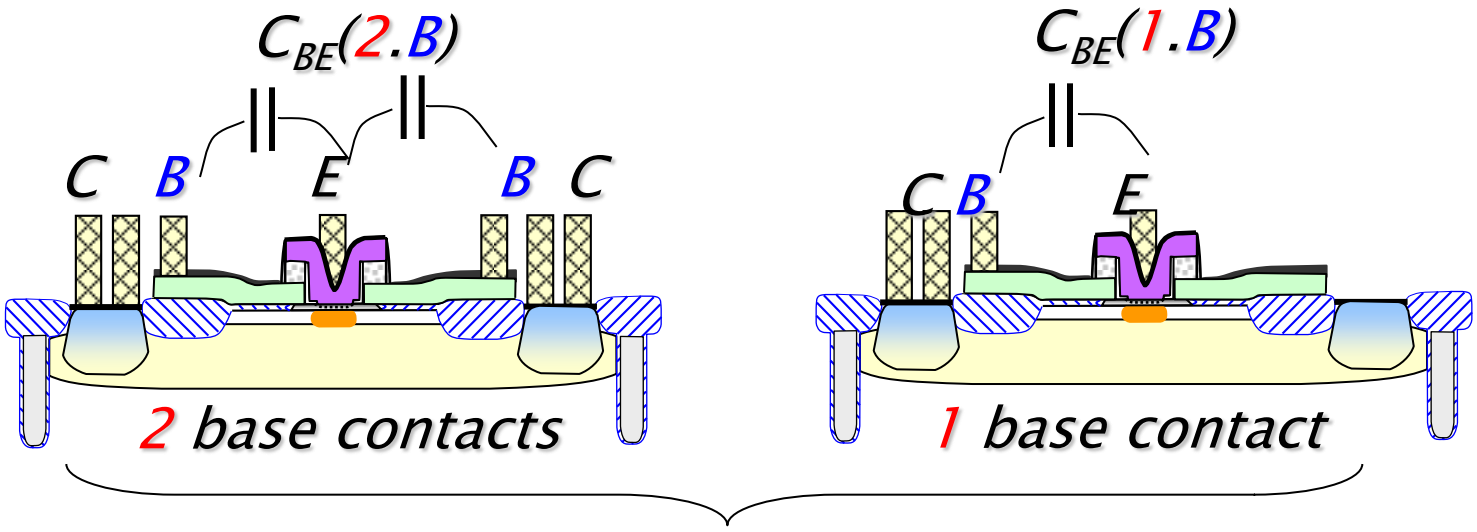


Open2

Specific open could be used only between port 1 & 2 (C_{PBC} capacitance)

De-embedded equivalent circuit (6): Capacitances

Symmetrical test structures

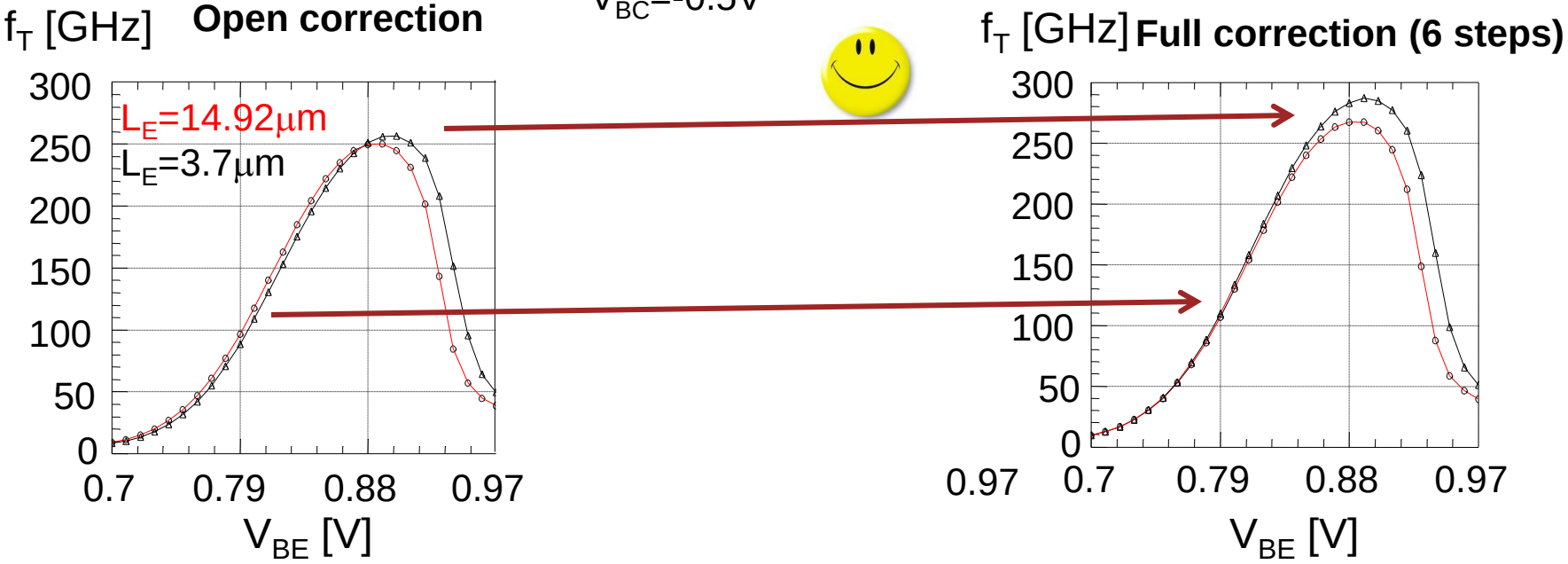


$$C_{backend}(1.B) \simeq C_{BE}(2.B) - C_{BE}(1.B)$$

Comparison (Open Vs 6 steps):

BiCMOS9MW CBEBC W_E=0.3µm, L_E=14.92µm et L_E=3.7µm

V_{BC}=-0.5V

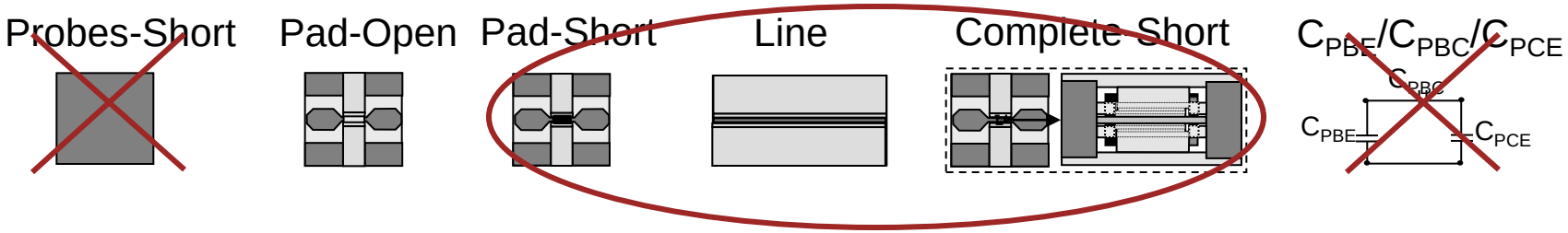


f_T extracted from measurements @10GHz

Discussion

- Good correction for 6 steps
- Different type of dummies → processing is more complex
- More de-embedding dummies for one DUT
  - Large set of devices end by doubling or tripling the number of dummies → Si area

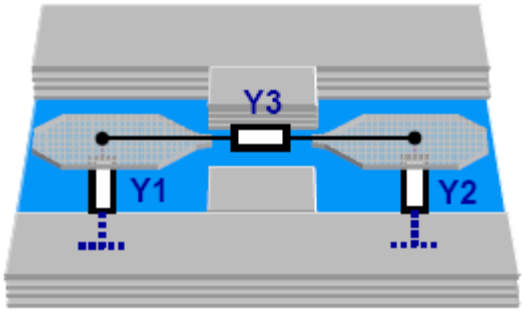
6 steps very complex → Specified approach, Two steps

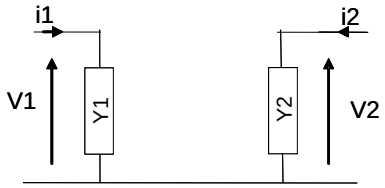


R, L circuit

Two-Step de-embedding

- Pad Open

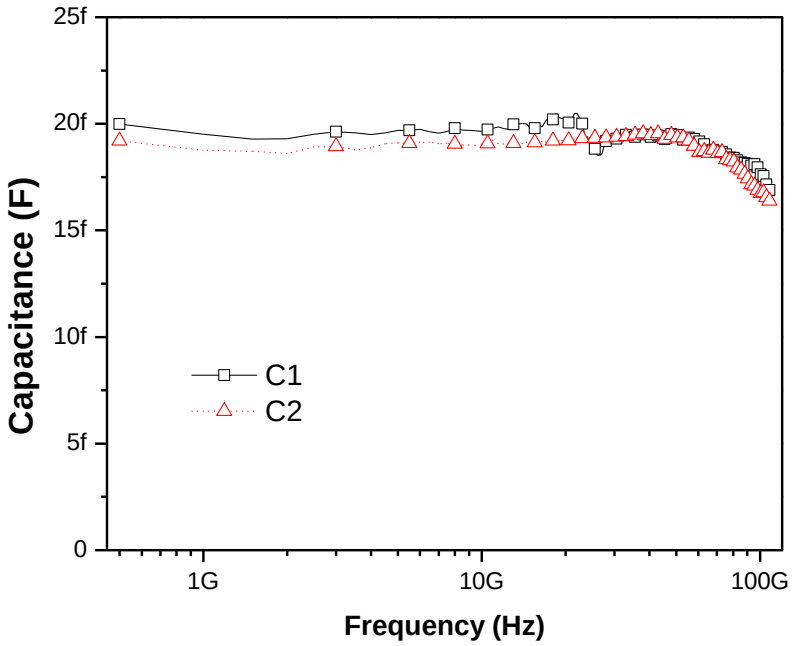




$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix}$$

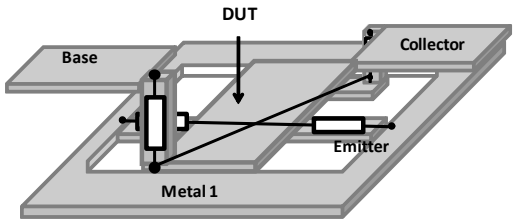
$$C_1 = \left(\frac{1}{2 * \pi * f} \right) \mathrm{Im}\left(Y_{11}\right)$$

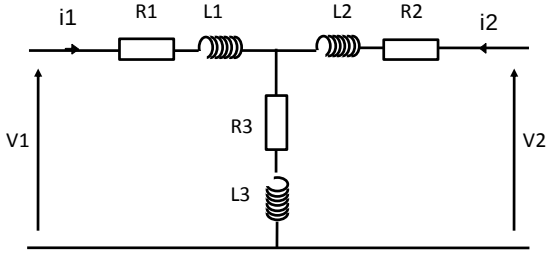
$$C_2 = \left(\frac{1}{2 * \pi * f} \right) \mathrm{Im}\left(Y_{22}\right)$$



Two-Step de-embedding

- Complete-Short



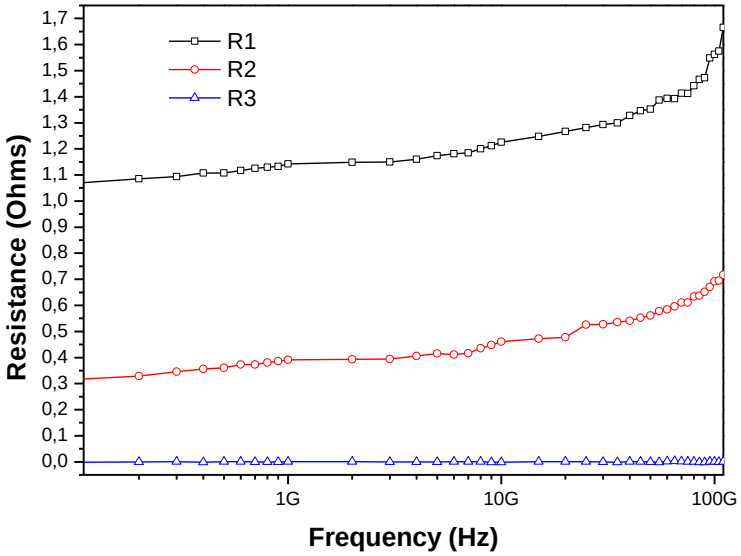


$$\begin{pmatrix} v_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}$$

$$R_1 = \mathrm{Re}(Z_{11}) - \mathrm{Re}(Z_{12})$$

$$R_2 = \mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{21})$$

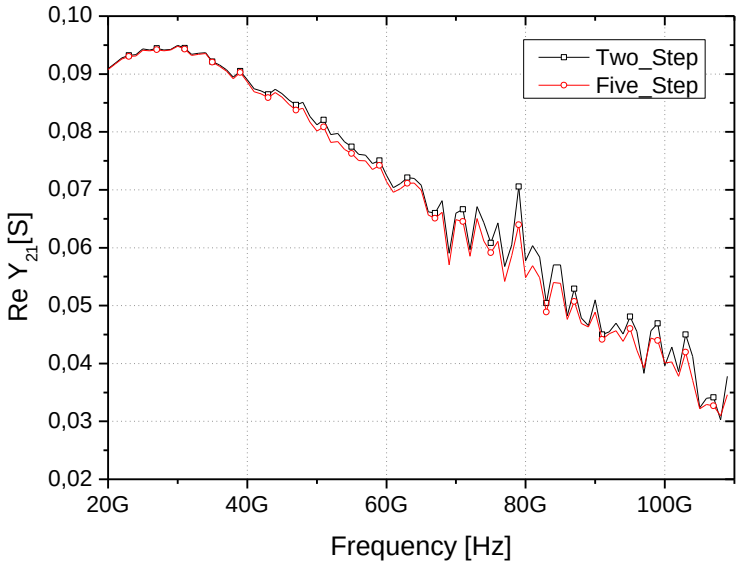
$$R_3 = \left(\mathrm{Re}(Z_{12}) - \mathrm{Re}(Z_{21})\right)/2$$

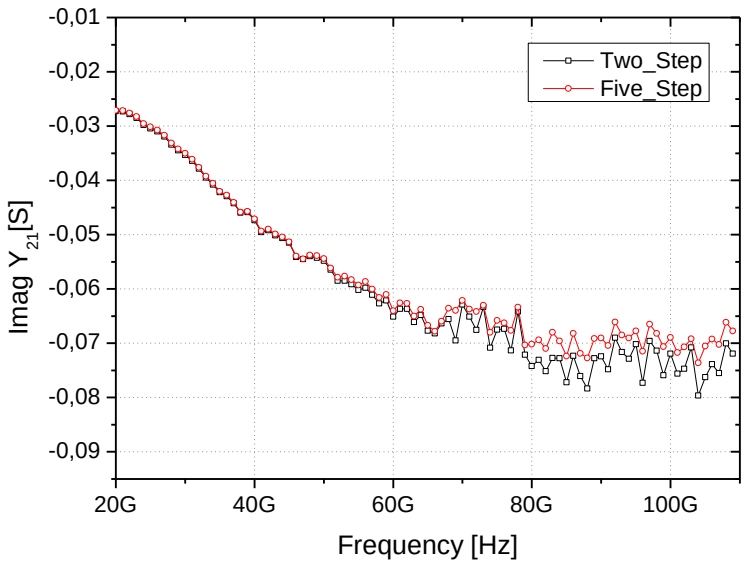


Comparison:

- Validation of the Two-steps method

CBEBC L_E=5µm, V_{BE}=0.9V, V_{CB}=0V





Comparison:

- Validation of the Two-steps method

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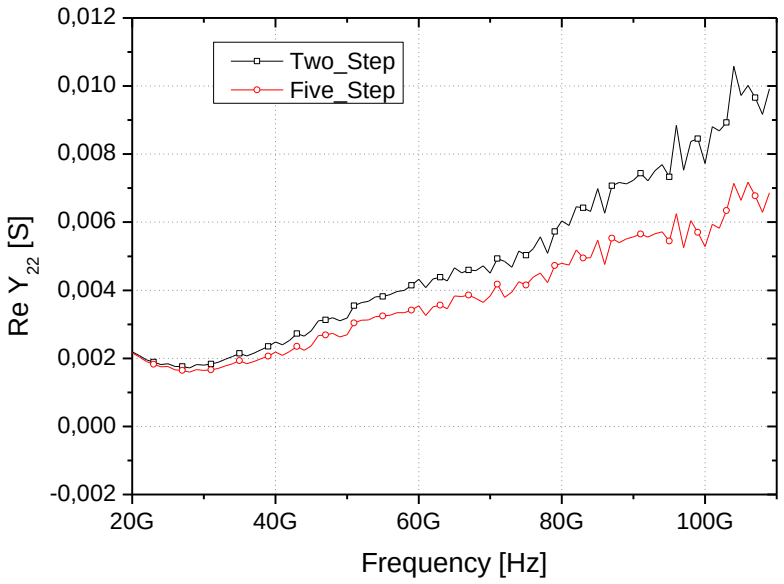

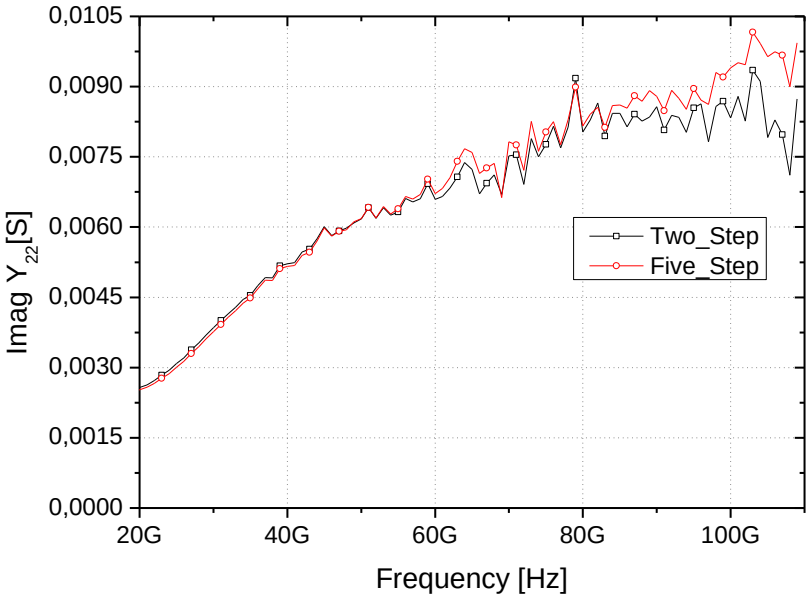

Conclusion

- Different de-embedding methods were presented
- A scalable solution for deembedding is the key
- De-embedding structures use a lot of Si surface
- Pad open and complete short may be sufficient

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Thanks For Your attention