Small Signal Study of Self-heating Effects in SOI FinFETs

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Introduction

FinFET based circuits have been proven quite advantageous over single-gate MOSFET based circuits due to higher gate control. But the SOI implementation is affected by the self-heating effects (SHE). It’s believed that self-heating affects analog circuits more than digital circuits [1]. The small signal study of self-heating (SH) using S-parameters helps us to demarcate between non-isothermal and isothermal regimes – the device is analogous to an electrical RC network [2], and hence a high frequency signal is unable to heat up the channel while a low frequency signal can cause a rise in the lattice temperature. Also it helps us to study the effect of self-heating on the transfer function of the device, which actually is required to study the effect of SH on analog design. Figure below shows a 3D schematic diagram of SOI FinFET.

Fig. 1 – Schematic figure of SOI Trigas FinFET

As apparent from the above figure, the fabricated device sits on a thick insulator which hampers the heat conduction. The reduced conduction results in a significant heating of the channel compared to bulk devices.

Characterization methodology

S-parameter measurements were done on trigate FinFETs with gate lengths ranging from 70 nm to 160 nm, and a fin width of 30 nm. The devices were processed with SOI gate stack and a metal mid-gap TiN gate. The S-Parameter measurements were performed at $V_{ds} = 0.5V, V_{gs} = 1.2V$ in the frequency range of 100kHz-8GHz. S-parameter data was de-embedded and converted to Y-Parameters from which the frequency dependent conductances ($g_{dsf}$, $g_{dsd}$) and capacitances ($C_{dsf}$ and $C_{dsd}$) were extracted.

Non-isothermal parameters

Starting from the definition of the Y-parameter with $y_{ds}$ being the isothermal Y-parameters at the drain-port and $V_j$ denotes the terminal voltages, $j/d$ (drain), $g$ (gate). Eq. (1) indicates that if the current is insensitive to the variation of the temperature, the non-isothermal admittances would approach to their isothermal counterparts even in the presence of self-heating. Fig. 2 shows the DC thermal measurements we did to determine $\partial y_{ds} / \partial T$.

Eq. (1)

$$y_{ds} = y_{dsf} \frac{\partial y_{dsf}}{\partial T}$$

From the frequency dependent conductances it is straightforward to derive an expression for the intrinsic gain ($g_m$). To calculate the intrinsic gain, we note that $g_m = g_{dsf}(V_j)$ and $g_{dsd}(V_j)$ assuming a first-order thermal network. Taking the real part of eq. (1), we get a simplified expression for intrinsic gain:

$$G_i(f) = \frac{1}{\partial y_{dsf}/\partial T} \frac{R_{th}}{1+4\pi^2f^2R_{th}^2C_{th}^2}$$

where $G_m(f)$ denotes the non-isothermal intrinsic gain, $g_{dsf} / g_{dsT}$ is the isothermal intrinsic gain, $\partial y_{dsf} / \partial T$ represents the thermal sensitivity of the bias-current ($I_{ds}$ at $V_{ds} = 0.5V, V_{gs} = 1.2V$ in the present case), $R_{th}$ is the thermal resistance and $C_{th}$ is the thermal capacitance. As apparent from the above equation, the pole frequency strongly depends, among other factors, on the bias current and isothermal output conductance ($g_{dsd}$). Lower values of the bias current and higher values of $g_{dsf}$ push the pole frequency to lower values, and the non-isothermal intrinsic gain towards its isothermal value.

Fig. 2 – Bias current variation with the ambient temperature

Self-Heating Characterization Results

Fig. 3 compares the conductances of N- and PFET. From the figure it’s apparent that the NFET is more strongly affected by self-heating than the PFET (NFET experiences a significant $g_{ds}$ reduction at low frequencies due to self-heating). This is attributed to both lower on-current in the PFET and a lower sensitivity of the on-current on the lattice temperature – as discussed above.

Fig. 3 – Comparison between extracted conductances $g_{dsf}$ and $g_{dsd}$ of NFET and PFET at S-Parameter data. Higher self-heating in the NMOS device degrades the $g_{dsd}$ substantially at lower frequencies.

For NFETs, we observe that the intrinsic gain deviates significantly from its isothermal limit, and even goes negative for long channels, whereas the PFET intrinsic gain deviates only slightly from its high frequency limit. It’s also interesting to note that we don’t observe negative intrinsic gain for the 70nm PFET even with the higher bias current. This follows from the fact that the observed output conductance of the short-channel device is significantly higher than that of the long-channel devices. For PFET devices, no negative intrinsic gain is observed – even for long channels. This can be attributed to significantly lower self-heating in PFETs.

Fig. 4 – Comparison of intrinsic gain ($g_m / g_{dsi}$) for short-channel NFET and PFET. In the high frequency regime NFET and PFET gain is comparable. However at low frequencies the NFET gain is strongly enhanced by approx. a factor of 4-5.

References