Introduction to

Accelicon’s Modeling Tools And Services
Accelicon Technologies, Inc.

- Founded by Xisheng Zhang in July, 2002
- Head office in Cupertino, CA, US
- Full time employees 27, contractor 5.
- Well-known technical adviser board
  - SPICE Modeling expert (BSIM4, PSP and Mextram)
  - Analog/RF designer
  - EDA experts in placement/routing
Expertise from Many Years Experience

Key Team Members

- Dr. Xisheng Zhang
  - President, was VP of R&D, Celestry
- Tim Smith
  - CEO, was VP of Sales, Cadences
- Dr. Xiaolan Wu
  - VP of Marketing, was Director of Marketing, Cadence
- Yanfeng Li
  - Manager of SPICE modeling, was Principle Engineer of PDF
- Yuping Wu
  - Manager of Analog layout group, was Technical Leader of Synopsys
- 22 R&D engineers, many from top universities of China

15 years

Expertise

- CMOS Modeling
- Statistical/Mismatch Modeling
- Test Chip Design
- Analog Layout
- EDA Tool Integration
Selected Customer List

- IBM
- Chartered Semiconductor Manufacturing
- SONY
- ELPIDA
- NEC
- TSMC
- Macronix International Co., Ltd.
- Winbond
- SMIC
- ALTERA
- XILINX
- QUALCOMM
- RF Micro Devices
- National Semiconductor
- HEJIAN
- 1st Silicon
- SinoMOS
- Infineon Technologies
- ATI
- Silian
- RICOH
- ProMOS Technologies
- EMLSI
- AMD
- TOSHIBA
- UMC
- DongbuAnam Semiconductor
- CSMC
- 华虹-NEC
- AMI
- Grace Semiconductor Manufacturing Corporation
- SAMSUNG
Accelicon’s MQA

- Turn-key, fully automated model validation solution for IC designer and modeling engineers.
- Market leader.
- IBM, AMD, Infineon, Sony, Qualcomm, AMIS, Xilinx, Altera and many others use it very heavily in their daily work.
- It provides a great platform to accommodate all user’s model QA and validation routines.
Accelicon’s MQA

- Turn-key, fully automated SPICE model validation solution for IC designer

- User customizable rule file (setup)
- MQA (Model Quality Assurance)
- HSPICE
- SPICE Simulator
- Model library
- Iv/CV/S/PCS
Why MQA (I)

- **Accuracy**
  - Validate Foundry’s generic SPICE model (digital model) vs. customer’s special design application
  - Process variations (corner), temperature, yield analysis

- **Comparison**
  - Foundry’s revision of model
  - Different foundries, technology nodes

- **Documentation**
  - Design documentation for new technology
Why MQA (II)

- Flexibility is the key!
- Open environment allows user to build and automate QA routines for new models and new methodologies.
- Unique data structure eases model data sharing.
- Provide a flexible platform for user to develop QA and documentation procedures for various models (SPICE models, backend models, and DFM models).

![Vtsat vs. L Chart](image)

**Vtsat vs. L Chart**

<table>
<thead>
<tr>
<th>Model Type</th>
<th>Site</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1_SS</td>
<td>site1</td>
</tr>
<tr>
<td>M1_FF</td>
<td>site1</td>
</tr>
<tr>
<td>M2_SS</td>
<td>site2</td>
</tr>
<tr>
<td>M2_FF</td>
<td>site2</td>
</tr>
<tr>
<td>M1_FF</td>
<td>site3</td>
</tr>
<tr>
<td>M2_FF</td>
<td>site3</td>
</tr>
</tbody>
</table>
Modeling in Foundry/Fabless

- Model generator (foundry) and model user becomes more insolated to each other
- Foundry’s generic model vs. different design applications
Example of Problematic Model Card

- Rout vs W is not right for long and narrow device
Example of Problematic Model Card (II)

Spectre calculation result = $-1.19 \times 10^{-13}$.
Report a warning
MQA’s Basic Facts

- Written using Java, run in every platform
- Support all compact models supported by commercial simulators.
  - MOS: Bsim3/4, PSP, HiSIM, BsimSOI and sub-circuit models.
  - BJT: GP, Mextram, others (Black box testing)
  - Resistor, Capacitor, Inductor, and other passive elements
  - Support any circuit block validations
- Support all popular simulators.
- Support different measurement formats
  - IV, CV, S, Noise, ET
  - Different file formats from different tools
MQA’s Main Features

- Rule driven model validation
  - Knowledge based rule, and check functions
- Flexible Interface
- Run time comparison
- Model report function
- Data management and data sharing
- Model Advisor
Rule File for Model Validation

- Contain many rules, knowledge based
- One rule check one specific characterization of model. The structure of one rule

IF (condition satisfied) Then

Do something (get model parameter, or, calculate current, or vth etc.)

Check result (in a range, or, no kink, etc.) and report error/warning if any

Enable/Disable, based on design or user input
Let MQA generate some results
Use MQA’s math function to do inspection

Users can write their own rules
Knowledge Based Rule Driven QA
Flexible Interface

- Rule driven and fully customizable.
- Support batch mode.
- User customizable targets and check functions.
- Easy to support new models.
- Easy to adjust to any QA flow.
Run Time Comparison

MQA’s Result

NMOS Typical Model Result

NMOS Fast Model Result

PMOS Typical Model Result

New Graphic

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Automatic Report Generation Example
Summary of MQA Features

- **SPICE model qualification tool**
  - Knowledge based rule
  - Can handle huge amount of data

- **Design documentation tool**
  - Overlay with measurement data
  - Dynamic graphic to zoom/change scale

- **Design interface (foundry interface) tool**
  - Comparison
  - Sharing the new technology characterization

- **Flexible environment**

- **Model Advisor**
MBP’s Basic Facts

- SPICE Model Extraction Tool
  - Engine: Modified SPICE3f5
    - Support BSIM3v3, BSIM4, GP, PSP, HiSIM, Diode
    - DC, AC (s parameter), Noise
- Optimizer
  - Working with world best known experts in math optimization field
  - State of the art optimizer combines speed, accuracy and robustness
- Development tool: Java
Model Building Program (MBP)

Automatic

Flexible

MBP

TaskTree

BSIM3

BSIM4

PSP

GP

Diode

High Voltage Model

Auto Bin

Auto Retargeting

Equation Viewer

Auto Lib parser

Easy Sub-Circuit

Error Monitor

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MBP Feature Highlight

- **User customizable TaskTree**
  - Allow user to customize and automate extraction/optimization process
  - Better task definition and arrangement
  - A complete model extraction methods based on optimization methodology
  - Automatic extraction of global model, temperature and corner model.

- **Powerful Equation Viewer**
  - Enable user to easily view the model equations and the related variable values, it provides a great tool for model issue debugging.
  - Model tweaking linked with equation viewer
  - Output OP, intermediate variables and equivalent circuits

- **Optimization on Intermediate Variables**
  - Provide optimization with more physical meaning

- **Powerful error monitor to ensure accurate global fitting**

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State of the Art TaskTree

- Combines flexibility and automation
- Offers different levels of extraction
- User can develop their own modeling methodology
State of the Art TaskTree

- Everything is based on TaskTree

Diagram:
- Auto Bin
- Auto Corner
- Auto Bsim3/4
- Auto Subckt
- Auto PSP
- Auto Hisim
- Mismatch
- Auto Stac
Other Applications

- Taskstree can be also used for running many other modeling applications:
  - Measurement QA, Data screening, Golden Die Selection.
  - Automatic corner model generation.
  - Automatic model re-targeting.
  - Automatic extraction routines for other device models.
MBP’s Task Tree

- Benefits to customers
  - Auto extraction/Optimization
  - Productivity increase
  - Easier to get good quality model
  - Open for customer’s customization
Model Equation Viewer

[Graph showing model equations and optimization settings]
Vth’s Equation of BSIM3v3

\[ V_{th} = V_{th0x} + K_{10x} \sqrt{\Phi_s - V_{bseff}} - K_{20x} V_{bseff} + K_{10x} \left( 1 + \frac{Nlx}{L_{eff}} - 1 \right) \sqrt{\Phi_s} + \frac{T_{ox}}{W'_{eff} + W_0} \Phi_s \]

\[ - D_{VT0} \left( \exp \left( - D_{VT1} \frac{W'_{eff} + L_{eff}}{2l_{bw}} \right) + 2 \exp \left( - D_{VT1} \frac{W'_{eff} L_{eff}}{l_{bw}} \right) \right) (V_{bi} - \Phi_s) \]

\[ - D_{VT0} \left( \exp \left( - D_{VT1} \frac{L_{eff}}{2l_{t}} \right) + 2 \exp \left( - D_{VT1} \frac{L_{eff}}{l_{t}} \right) \right) (V_{bi} - \Phi_s) \]

Vth0=0.295, Nlx=2.94e-7, Dvt0=1.106 Dvt1=0.493 Dvt2=-0.092 K1=0.47
W=10um L=0.13um T=25C

How big is Lt? How big is the Dvt1 term? Why adjust Dvt2, curve does not change?
MBP Shows the Full Equation with Parameter Turner

Adjust Parameter, and see the real time change of equation
Hybrid Global Model

No limitation on the local of second model
Smooth Boundary
Compare of Hybrid and global model

- One or several devices not fit well by global model

- Use of hybrid model to get better fitting result
## Compare the three formats of model

<table>
<thead>
<tr>
<th></th>
<th>Global Model</th>
<th>Binning Model</th>
<th>Hybrid-Model</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Model format</strong></td>
<td>All parameters are same for different special caution)</td>
<td>Region model, each region’s 0/l/w/p parameters are calculated from point models</td>
<td>Global model with some selected parameters become function of device size in a user defined region (w/l’s region)</td>
</tr>
<tr>
<td><strong>Advantage</strong></td>
<td>Physical meaning, easy to maintain, easy to generate corner model</td>
<td>Accuracy is better, if the bin region is small</td>
<td>Combine the advantage of both binning model and global model</td>
</tr>
<tr>
<td><strong>Disadvantage</strong></td>
<td>May have problems to fitting some device’s behavior</td>
<td>Extraction is tedious, time consuming, and special caution must be taken when generate the point model. Difficult to maintain. Difficult to generate corner model</td>
<td>Remove the limitation of global model</td>
</tr>
<tr>
<td><strong>Continuity</strong></td>
<td>Characterization vs L(or W) is continual</td>
<td>Characterization vs L (or W) is first-order continual cross the bin boundary, the trend may not right inside bin boundary if extraction is not carefully done</td>
<td>Same as global model</td>
</tr>
<tr>
<td><strong>Extraction tool</strong></td>
<td>Public domain methodology, supported by all modeling tool</td>
<td>Public domain methodology, supported by all modeling tool</td>
<td>Accelicon’s patent-pending methodology, available only in MBP</td>
</tr>
</tbody>
</table>
Check All the Modeling Criteria

<table>
<thead>
<tr>
<th>L (um)</th>
<th>W (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.46</td>
<td>1.55</td>
</tr>
<tr>
<td>2.68</td>
<td>2.61</td>
</tr>
<tr>
<td>2.94</td>
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<td>1.52</td>
</tr>
<tr>
<td>3.62</td>
<td>29.99</td>
</tr>
</tbody>
</table>

All the fitting targets

One particular device fitting results
Easy Sub-circuit Modeling - HV

- Accelicon uses macro model approach that accurately models:
  - Quasi-saturation effect
  - Vbs dependency of Rd and Rs
  - Severe impact ionization
- Our methodology is very flexible and can model many unexpected effects (such as the one highlighted below)
  - Sufficient to address all kinds of parasitic elements
A common circuit used for HV modeling is shown below, impact ionization is not modeled with this circuit.
Easy Sub-circuit Modeling – Layout effect

- MBP allows user to define and optimize on new measurements
  - Device performance vs. layout parameters, such as I_{dsat} vs. SCA
- User can define equations in sub-circuit model format to address layout effects and utilize MBP to easily adjust these parameters.
Statistical, Mismatch Functions
Auto Resistor Model Extraction

- Automatically process resistor data and model simulation.
- Plot resistor performance.
- Automatically extract model parameters.
The modeling experts have years of modeling experiences with various technologies. Currently several world-leading foundries are using Accelicon’s modeling services. We can provide service on both front end and back end modeling. Accelicon’s SPICE modeling services include:

- BSIM3/4/PSP model extraction services (temperature model with corners)
- Bipolar models
- RF modeling
- HV and FG devices subcircuit modeling
- Interconnect modeling
- Physical verification deck generation including DRC, LVS and RCX.
MOS SPICE Modeling

- Supported Compact Model
  - BSIM3v3.2
  - BSIM4
  - PSP: in development
  - Supported Simulators
  - HSPICE
  - Spectre
- Chose of Global or Binning According to
  - Applications
  - Client Preference
- High Quality Model with Rigorous QA Procedure
  - DC
  - AC
  - Temperature
  - Corner models
    - Best case (Fast)
    - Worst case (Slow)

Preliminaries
- Establish temp. range
- Establish Model Specs.
- Determine Process Parameters

DC Model Extraction

Error Criteria Satisfied?
- No
- Yes

AC Model Extraction

Error Criteria Satisfied?
- No
- Yes
RF SPICE Modeling

- Device Type
  - MOS
  - On-chip inductors
  - MIM-Caps
  - Varactors

- Lumped Circuit Model
  - Scalable
  - Valid up to 6Ghz

- Rigorous QA Procedure
  - Ensure model quality
Macro Modeling

- Device Type
  - HV devices, typically LDMOS

- Macro Circuit Model
  - BSIM3V3 core model
  - Optimized the macro circuit elements to obtain the best fit

- Rigorous QA Procedure
  - Ensure model quality
TEG Design

- Digital Block
  - SPICE
  - Interconnect
- Analog & RF
  - Mismatch
  - BJT
  - RF structures
  - Substrate coupling
  - ESD
Interconnect Modeling

- Accelicon has industry’s first complete interconnect parasitic extraction solution
- This methodology has been exercised many times with excellent success
- Accelicon expertise covers structures design, characterization, interconnect modeling and layout parasitic extraction
- In Accelicon, interconnect modeling is referred as RCX
Summary

- Accelicon has the best SPICE modeling tools
  - MQA: validation, documentation, comparison, sharing
  - MBP: equation viewer, Hybrid-model, HV solution

- Accelicon’s tools have been used by worldwide foundry, IDM, design companies