1/f Noise Corner Modeling

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MOS AK 07, Unterpremstaetten 2007-04-20
Agenda

- “Appetizer” – Why to model LF noise?
- LF noise critical design areas
- Some basic theory
- Methodology for corner generation & implementation
- Design example
- Status quo – software, models, equipment …
- Summary
Future technologies

--> increased noise mainly due to new process generations and additional defects!

- **Digital**: \( W \times L = 3 \times 1 \) \( L_{\text{min}}^2 \), p-p Noise
  \( f_{\text{max}}/f_{\text{min}} = 1 \), error rate = \( 10^{12} \), \( t \times \sigma = 12 \text{dB} \)

- **RF**: \( W \times L = 1000 \times 1 \) \( L_{\text{min}}^2 \), RMS Noise
  \( f_{\text{max}}/f_{\text{min}} = 1 \text{MHz}/1\text{Hz} \), \( t \times \sigma = 10 \text{dB} \)

- **Analog**: \( W \times L = 500 \times 20 \) \( L_{\text{min}}^2 \), RMS Noise
  \( f_{\text{max}}/f_{\text{min}} = 100 \text{kHz}/1\text{Hz} \), \( t \times \sigma = 6 \text{dB} \)

LF Noise Critical Design Areas I

- Audio (0-20kHz)
- RF Systems (phase noise, ...)
- Low Power (medical applications like pacemaker, ... or watches)
- High precision analog circuits for sensors, >=24bit AD/DA converters

In principle: Noise is the main limitation for high resolution analog design and all RF systems are affected by noise (!)
RF System - phase noise:

• **Q-factor of the resonator and varactor (tradeoff to bandwidth)**
• **1/f noise of active device (transistor)**
• **DC bias and external tuning voltage noise**
Some Basic Theory I

Typical LF drain-current noise of a MOS device:
Some Basic Theory II

Typical LF drain current noise of a real MOS device:

In case for robust design it is sufficient to know the maximum noise level!

In case for LF noise design optimization it is necessary to know the spread also!
MOS SPICE Formulas:

\[ S_{in} = \frac{1}{C_{OX} \cdot L^2} \frac{K F \cdot I_{DS}^{AF}}{f^{EF}} + \frac{8}{3} \cdot k \cdot T (g_m + g_{mb} + g_{ds}) \]

\[ S_{in} = \frac{1}{C_{OX} \cdot W \cdot L} \frac{K F \cdot I_{DS}^{AF}}{f^{EF}} + \frac{8}{3} \cdot k \cdot T (g_m + g_{mb} + g_{ds}) \]
Some Basic Theory III

BSIM3V3 Formulas (valid for both NMOS and PMOS):
(derived from oxide-trap induced carrier and surface mobility fluctuation mechanism)

\[ V_{gs} \geq V_{th} + 0.1 \]

\[ S_i(f) = \frac{q^2 \cdot V_i \cdot \mu_{eff} \cdot I_{ds}}{1 \times 10^{18} \cdot C_{ox} \cdot I_{eff}^2 \cdot f} \left[ NOIA \cdot \log \left( \frac{N_0 + NSTAR}{N_i + NSTAR} \right) + NOIB \cdot (N_0 - N_i) + NOIC \cdot \frac{N_0^2 - N_i^2}{2} \right] + \]

\[ \frac{V_i \cdot \Delta I_{clm} \cdot I_{ds}^2}{W_{eff} \cdot I_{eff}^2 \cdot f} \cdot \frac{NOIA + NOIB \cdot N_i + NOIC \cdot N_i^2}{(N + NSTAR)^2} \]

\[ N_0 = \frac{C_{ox}}{q} \cdot (V_{gs} - V_{th}) \]

\[ N_i = \frac{C_{ox}}{q} \cdot (V_{gs} - V_{th} - \text{Min}(V_{ds}, V_{ds\text{sat}})) \]

\[ V_{gs} < V_{th} + 0.1 \]

\[ S_{km,\mu}(f) = S_i(V_{gs} = V_{th} + 0.1) \]

\[ S_{Wi}(f) = \frac{NOIA \cdot V_i \cdot I_{ds}^2}{1 \times 10^{8} \cdot W_{eff} \cdot I_{eff} \cdot f \cdot (NSTAR)^2} \]

\[ S_i = \frac{\Delta I_{clm}}{\Delta f} = \frac{S_{Wi} \cdot S_{km,\mu}}{S_{Wi} + S_{km,\mu}} \]

flicker term + thermal noise term = LF noise characterisation

[http://www-device.eecs.berkeley.edu/~bsim3/latenews.html]
LF noise as a sum of Lorentzians:

\[ S_N(f) \approx \frac{\tau}{1 + \tau^2 f^2} \]

\[ S_N(f) \approx \sqrt{\sum_{\tau=\tau_0}^{\tau_1} \left( \frac{\tau}{1 + \tau^2 f^2} \right)^2} \approx \frac{1}{f} \]

A large enough sample of devices will exhibit on the average 1/f behaviour in case of equally distributed Lorentzians!
Methodology For Corner Generation & Implementation

1.) Measurement of several geometries @ different bias settings per wafer per lot

2.) Calculation of the average and 3 sigma deviation for each geometry/bias
   → typical mean data base (tm) and worst case data base (wc)

3.) Parameter extraction for tm and wc

4.) Simulator implementation → → →

5.) check: simulation versus measurement

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Methodology for Corner Generation & Implementation

Simulation versus Measurement

- **NMOS** \( W/L = 10/1.2 \)
- \( V_{DS} = 2V \)
- \( I_D = 1 \) and 100\( \mu \)A

- \( I_D = 2 \) and 200\( \mu \)A
Low noise audio amplifier

Specification: 7µV @ 0.5pF load for LF BW 1.5-14kHz

Simulated: tm=2.7µV; wc=3.5µV

Measurement: 3.06µV for several circuits

→ good agreement with the LF noise WC models
Status Quo - Software, Models, Equipment ...

Supported models : BSIM3v3, (SPICE)
Supported Simulators : SPECTRE, ELDO, ...
Extraction environment: MATLAB, ICCAP
Measurement Software: LABVIEW (HP4155, HP89410A), (ICCAP)
Processes : 0.35µm CMOS and High Voltage CMOS (>=50V) BiCMOS
Summary

- For LF noise critical designs → sample spread for design optimization
- Methodology for WC generation and simulator implementation
- Benchmark with a design example

Thank you very much for your attention!
Biasing Concept: SMU and battery driven buffer amplifier (in house development)

totally screened in a metal box for packaged devices

Electrical specifications: $V_{GS} = \pm 0$ to 8V; $V_{DS} = \pm 0$ to 8V; $V_{BS}$ additionally (also $\pm 0$ to 8V)

$IDS = 1\mu A$ to 200$\mu A$

Freq. = 100Hz to 30kHz (with some restrictions to 100kHz; 2.5 to 3 decades)
APPENDIX – On wafer equipment

Biasing Concept: SMU with 1Hz filters

Electrical specifications:
VGS = 0 to ±10V, VDS = 0 to ±3V
IDS = 1μA to 100μA, GSG probes only
Freq. = 1Hz to 1kHz (with some restrictions to 100kHz)