MODELLING OF CARBON NANOTUBE FIELD EFFECT TRANSISTORS ORIENTED TO SPICE SOFTWARE FOR A/D CIRCUIT DESIGN

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BACKGROUND AND AIMS

WE PRESENT A MODEL OF CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNTFETS) DIRECTLY AND EASILY IMPLEMENTABLE IN SIMULATION SOFTWARE. THE MODEL IS BASED ON THE HYPOTHESES OF FLAT VoltAge TRANSPORT IN A MESOSCOPIC SYSTEM BETWEEN TWO NON-REFLECTIVE CONTACTS. TO AVOID THE PROBLEMS ASSOCIATED WITH THE DIFFERENT PARAMETERS EXTRACTED FROM QUANTUM MECHANICAL SIMULATIONS OF THE DEVICE AND DEPENDANT ON THE NANO DIMENSION AND THE CNT DIAMETER. MOREOVER TWO COEFFICIENTS, DEPENDING ON THE SUB-BAND INDEX, ARE INTRODUCED TO EVALUATE THE HYSTERESIS IN THE TRANSPORT. IN ORDER TO DETERMINE THE QUANTUM CAPACITANCES. IN THIS WAY THE PROPOSED MODEL ALLOWS AN EASY IMPLEMENTATION OF THE MODEL IN SIMULATORS WITHOUT LOSING IN ACCURACY WITH A RELATIVE ERROR LESS THAN 5% IN COMPARISON WITH EXPERIMENTAL DATA.

INTRODUCTION

CNTFETS are field effect transistors using a carbon nanotube as channel. As it is known, the carbon nanotubes consist in a hexagonal mesh of carbon atoms wrapped in cylinder shapes, some time with closing hemispherical meshes on the tips. An important characteristic of CNT is mesh tension, denoted as chirality, which has a strong influence on the CNT behaviour, changing electronic band structure. Among carbon nanotube FETs, C-CNTFETs or conventional CNTFETs, with heavily doped source and drain contacts, show the best performances in terms of “on-off” ratio current and subthreshold swing. Most of the models available in literature are numerical and make use of self-consistency and therefore they cannot be directly implemented in simulation software for electronic circuits, such as SPICE.

MODELLING I-V Model

The proposed model is based on a work of A. Raychowdhury et al. and on the following improvements introduced by F. Prégaldiny et al. The model, developed for a n-type C-CNTFET with semiconductor single wall CNT having diameters ranging from 1 nm to 4 nm, is based on the hypothesis of ballistic transport. In this hypothesis, when a positive voltage is applied between gate-source, the conduction band at the channel beginning decreases by $\Delta V_g$ (where $\Delta V_g$ is the surface potential), while $e$ is the electron charge. With the hypothesis that each sub-band decreases by the same quantity along the whole channel length, the total drain current is:

$$I_{D} = \frac{eL}{h} \int \left[ \left\{ \epsilon_{max}(x_1) \right\} - \left\{ \epsilon_{min}(x_1) \right\} \right] \mu(x_1) dx_1$$

The surface potential $\Delta V_g$ is expressed through the following equation:

$$\Delta V_g = \frac{qN_D}{\varepsilon_s} \left[ n(x) - n_0 \right] + e \frac{q}{\varepsilon_s} \frac{D_{nn}}{D_{np}} \left[ \left\{ \epsilon_{max}(x_1) \right\} - \left\{ \epsilon_{min}(x_1) \right\} \right]$$

We have considered the first five sub-bands, but verifying that only three sub-bands are required to describe the C-CNTFET behaviour having diameters ranging from 1 nm to 4 nm. Moreover we have verified that the sub-band effect is hidden when the quantum resistance $R_q$ of the dopant source region in series with the parasitic ones of the electrodes is considered.

To evaluate $V_{GS}$, the following approximation has been proposed:

$$V_{GS} = V_{DD} - V_{DS} - \left( \frac{qN_D}{\varepsilon_s} \right) \left[ n(x) - n_0 \right] - e \frac{q}{\varepsilon_s} \left( \frac{D_{nn}}{D_{np}} \right) \left[ \left\{ \epsilon_{max}(x_1) \right\} - \left\{ \epsilon_{min}(x_1) \right\} \right]$$

In the proposed algorithm we have not used the previous approximation of $V_{DS}$ to calculate $\Delta V_g$ and $\Delta V_g$, because some convergence issues occur during the SPICE simulation. Therefore $\Delta V_g$ has been evaluated as:

$$\Delta V_g = \frac{qN_D}{\varepsilon_s} \left[ n(x) - n_0 \right] + e \frac{q}{\varepsilon_s} \left( \frac{D_{nn}}{D_{np}} \right) \left[ \left\{ \epsilon_{max}(x_1) \right\} - \left\{ \epsilon_{min}(x_1) \right\} \right]$$

The CNTFET equivalent circuit, is similar to a common MOSFET one. We have extracted $V_{TH}$ and $\alpha$ by best-fit procedure between the measured and simulated values of $I-V$ characteristics of the device, while the quantum capacitances have been computed from the charge in the channel.

As analog test circuit a phase-shift oscillator has been used, it includes 3 identical RC networks, each stage provides a $\pi$-type phase shift, resulting in the required $\pm 180^\circ$ total phase shift. From the output of SPICE simulation, the oscillation frequency ($\approx$580 GHz) can be easily evaluated. At this frequency the CNT quantum inductance is negligible since the magnitude of the inductive reactance is much smaller than the resistance values of the doped drain and source regions ($\approx$25 k$\Omega$); only at about 10 THz these magnitudes are comparable and cannot be neglected in the circuit.

As digital application we have studied NOT logic gates in a four stage architecture. Each NOT is designed using 3 identical CNTFET, while resistors represent parasitic elements. The further fourth NOT gate has been used only to load the third stage. We have simulated the circuit driven by a 10ps clock, also in this case the CNT quantum inductance is negligible since the magnitude of the inductive reactance is much smaller than the resistances of the doped source region ($\approx$25 k$\Omega$) only at about 10 THz these magnitudes are comparable and cannot be neglected in the circuit.

CONCLUSIONS

WE HAVE PRESENTED A COMPACT, SEMI-EMPirical MODEL OF CNTFET IN WHICH WE HAVE PROPOSED SEVERAL ISSUES TO ALLOW AN EASY IMPLEMENTATION IN CIRCUIT SIMULATIONS, SUCH AS SPICE. IN ORDER TO OBTAIN THE ACCURACY OF THE PROPOSED MODEL, THE RESULTS HAVE BEEN COMPARED WITH THOSE OF THE NUMERICAL MODEL ONLINE AVAILABLE AND OF EXPERIMENTAL DATA, WITH A NEGLIGIBLE RELATIVE ERROR IN BOTH CASES. MOREOVER THE GOOD AGREEMENT BETWEEN SIMULATION AND EXPERIMENTAL RESULTS FOR A n-TYPE CNTFET DEMONSTRATES THE VALIDITY OF THE PROPOSED MODEL, BORN FOR n-TYPE CNTFET ALSO FOR THIS KIND OF DEVICES.

ACKNOWLEDGMENTS

WE HAVE APPLIED THE MODEL IN THE SPICE SIMULATOR TO DESIGN BOTH ANALOG AND DIGITAL CIRCUITS, DEMONSTRATING THE IMPORTANCE OF THE QUANTUM CAPACITANCE DEPENDENCE ON POLARIZATION VOLTAGE AND BEING TO INVESTIGATE ABOUT THE EFFECTS OF THE CNT QUANTUM INDUCTANCE.

REFERENCES


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