Modeling and optimization of SiP/SoP and packaging for signal integrity
Outline

- Introduction
- Embedded passives
- CST solutions for SiP/SoP, chips(SoC), MCM and packaging
- Examples and validation
- Conclusions
Overview examples

- **System-on-Chip (SoC)**
  - Partial system (two or more functions) on a single IC

- **Multichip Module (MCM)**
  - 2D integration of two or more ICs

- **Stacked ICs (SiP)**
  - 3D stacking of two or more thinned ICs

- **System-in-Package (SiP) / System-on-Package (SoP)**
  - Total system integration - Integration of active and passive components.
  - Multiple technologies are combined in a package.
System-on-Package (SoP) - Complete System Integration (active and passive parts)
Inductor

2 turns inductor on LTCC substrate (120x120mils)
VIC capacitor

On-Package Vertical Interdigitated Capacitor

n. of electrodes
Resonator

Surface Current $\text{max}(S21)$ at $2.81$ GHz
Filter

MIM

Inductor

VIC

S-Parameter Magnitude in dB

Frequency / GHz
Design flow

- **System design / Partitioning**
  - To define Circuit topology and values
    - Circuit diagram
  - To specify physical Layout

- **RF circuit design & simulation**

- **EM Simulation & RF circuit optimization**

- **System verification and multiple designs**
  - To verify & adjust layout for overall system performance
  - To check design rules and layout for system design issues (e.g. coupling).

- **DRC and overall layout check**

- **Fabricate and test / Verify results**
  - To test & to meet specification: Measure test circuits and module performance. Iterate best design to meet all specifications
Step 1

Ideal L and C; parasitics not considered.

Coupling is not considered.

C = 5 pF
C = 10 pF
C = 15 pF
Step 2

Parasitics of L and C are considered.
Coupling is not considered.

C = 5 pF
C = 10 pF
C = 15 pF
Step 3

Parasitics of $L$ and $C$ are considered.

Coupling is considered.
EDA imports

* .brd, * .mcm and * .SiP

bond wires and BGAs not available
SiP

Wirebonds and die stacks automatically imported
example
FEM - Tet
Model validation

FIT (time domain) simulation extended up to 100GHz with almost same time ($\approx 4h$) for each port
results

Type = Surface Current (peak)
Monitor = h-field (f=0.001) [1]
Component = Abs
Maximum-3d = 6461.87 A/m at 1452.9 / 1819.8 / 477.3
Frequency = 0.001
SiP with bond wires

Power noise coupling

Insertion loss

Port1 Power supply pin

Port2

Port3

Port4

Port5
Model validation
Currents

$f = 0.01 \text{ GHz}$

$f = 8.9 \text{ GHz}$
Currents

Type = H-Field (peak)
Monitor = h-field (f=0.01) [1]
Component = Abs
Plane at z = -0.6334
Frequency = 0.01
Phase = 0 degrees
Maximum=2d = 1.20592 A/m at -0.4 / -2 / -0.6334

Type = H-Field (peak)
Monitor = h-field (f=0.9) [1]
Component = Abs
Plane at z = -0.6334
Frequency = 0.9
Phase = 0 degrees
Maximum=2d = 130.183 A/m at 0.4 / -2 / -0.6334
TDR

Port 2 excited

Automatic extraction

$Z(t) / \text{Ohm}$
Full package - example 1
Results

Time Signals

S-Parameter Magnitude in dB

NEXT

NEXT
Eye diagram

Excitation Signal

Type
Select type: PAB5
Select file for ASCII import type: ...

Settings:
N: 7
Vpulse: 1.0
Trise: 0.05
Tfall: 0.05
Total: 0.05×2
Wrap: 2
Preset: 0

Source
Voltage Current Signal

OK Cancel Help

P2 Real Part

TD Voltage

Voltage / V

Time / ns
Timing analysis

Excitation Signal

- Type: PRRS
- N: 7
- Pulse: 1.0
- Rise: 0.05
- Fall: 0.05
- Total: 0.05
- Total: 0.05
- Wrap: 0
- Prebias: 0

Result Real Part

- Voltage / V
- Time / ns

input
output
Conclusions

- CST STUDIO SUITE™ can be successfully used to simulate and optimize embedded passives, SiP/SoP and real world packages

- The complete technology (FIT and FEM) can be used to achieve fast solutions and to validate the results

- Multiple examples prove the effectiveness of the solution offered by CST