

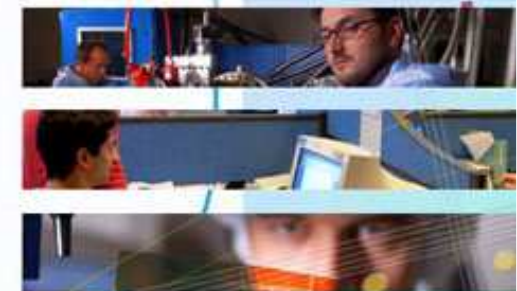
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MOSFET Modeling for Design of Mixed Analog/Digital Circuits at Cryogenic Temperature

Patrick MARTIN

CEA, LETI, MINATEC - Grenoble (France)



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Outline

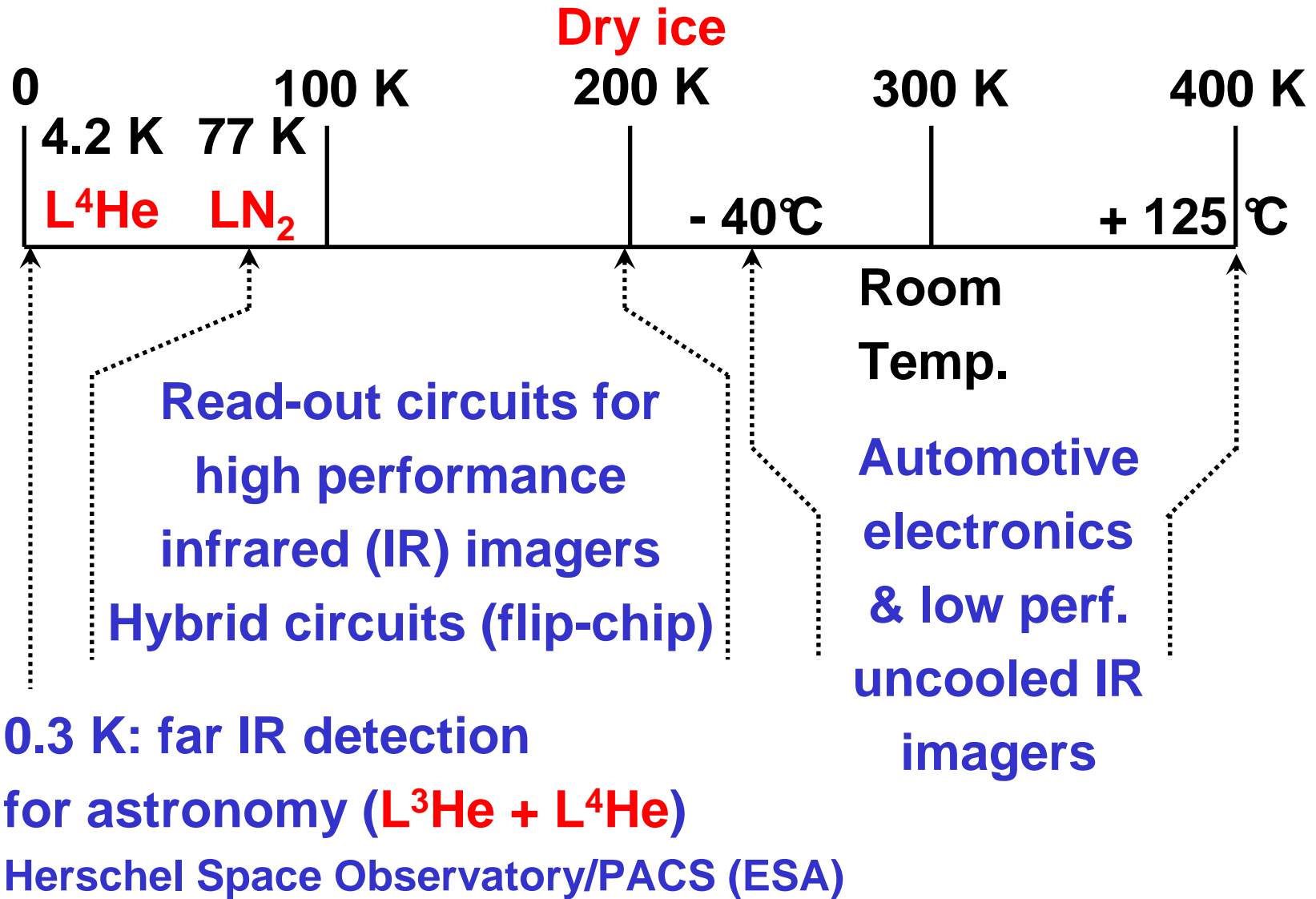
- **Introduction**
- **Studied CMOS process**
- **Specific & non specific physical effects at LT:**
 - **Freeze-out effect in LDD**
 - **Subbands quantization effect**
- **Compact modeling with EKV3**
- **Benchmarking of models at LT: PSP vs. EKV3**
- **1/f noise**
- **Transistor matching**
- **Conclusion**

Synthesis of work done in LETI during last 2 years on MOSFET at Low Temperature (LT)

- **WOLTE-8, Jena/Gabelbach 2008**
- **WCM-Nanotech, Boston 2008**
- **MOS-AK, Edinburgh 2008**
- **MOS-AK, Frankfurt am Oder 2009**
- **WCM-Nanotech, Houston 2009**
- **Int. Conf. on Noise & Fluctuations, Pisa 2009**
- **Article in Cryogenics, vol. 49 (11), 2009**
- **R. Fascio, DRT diploma, Grenoble INP, 2009**
- **WOLTE-9, Guarujá (Brazil), June 2010**



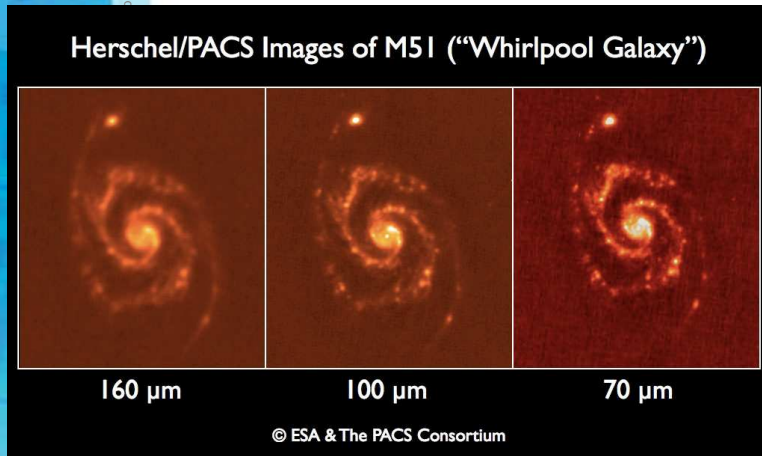
Why cryogenically cooled CMOS?



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Cooled CMOS at Ultra Low Temperature: 1st example

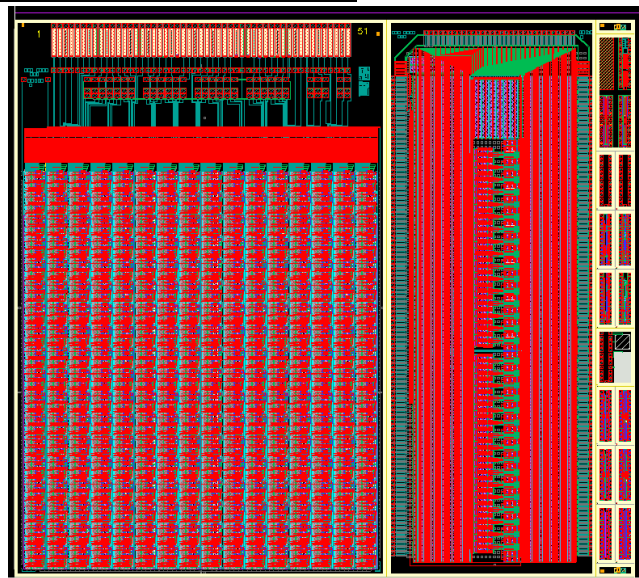
Ariane 5 launch, 14 may 2009
First test image



LT ASIC: 2 K stage



ULT ASIC: 0.3 K stage (from Si bolometer arrays 2560 px)

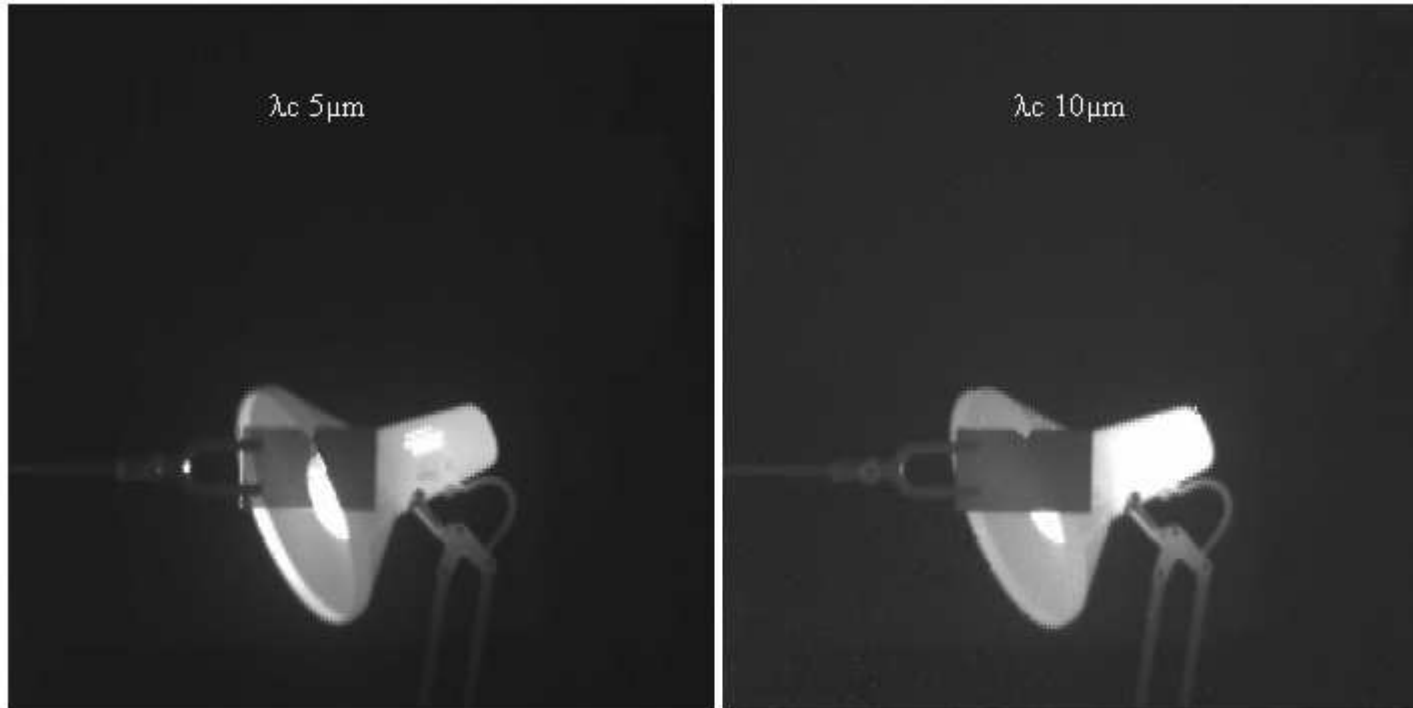


- Electrical characterization at 0.3 K and 4.2 K
- LF noise meas. at 4.2 K
- CMOS ≡ PD-SOI severe floating effects (kink)
- Lack of MOSFET model
- No complete parameter extraction
- “Simple” but robust read-out circuit: mainly PMOS source-followers and switches
- 0.5 μm CMOS process

← *Test module*

Cooled CMOS at Low Temperature: 2nd example

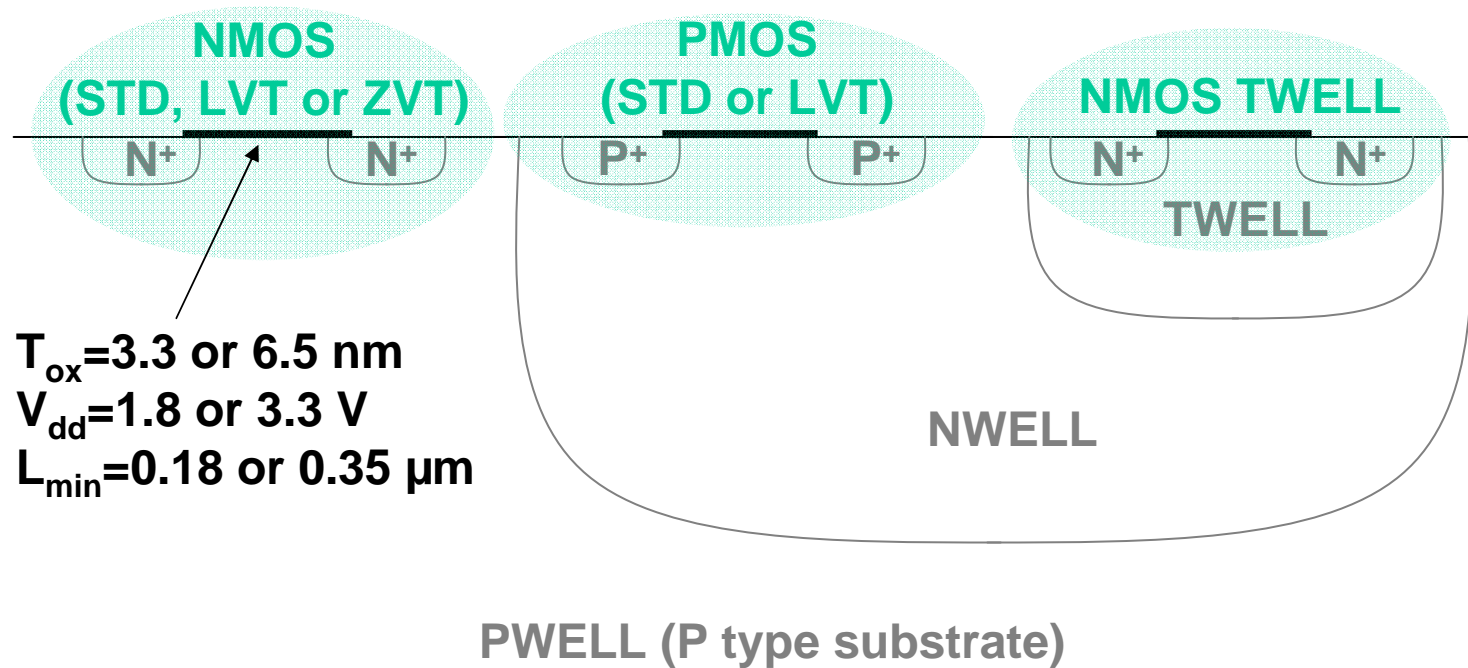
Bispectral IR imager from CEA/Leti



- **Format=256 x 256, pitch=30 μm**
- **Complex CMOS circuit, approx. number of transistors: 530,000**
- **0.35 μm / 3.3 V CMOS process**
- **Full parameter extraction at intermediate temperature (77 - 300 K)**

Results on a 0.18 μm CMOS process

Analog/Digital/RF transistors



12 kinds of MOS transistors

Standard and specific effects at LT

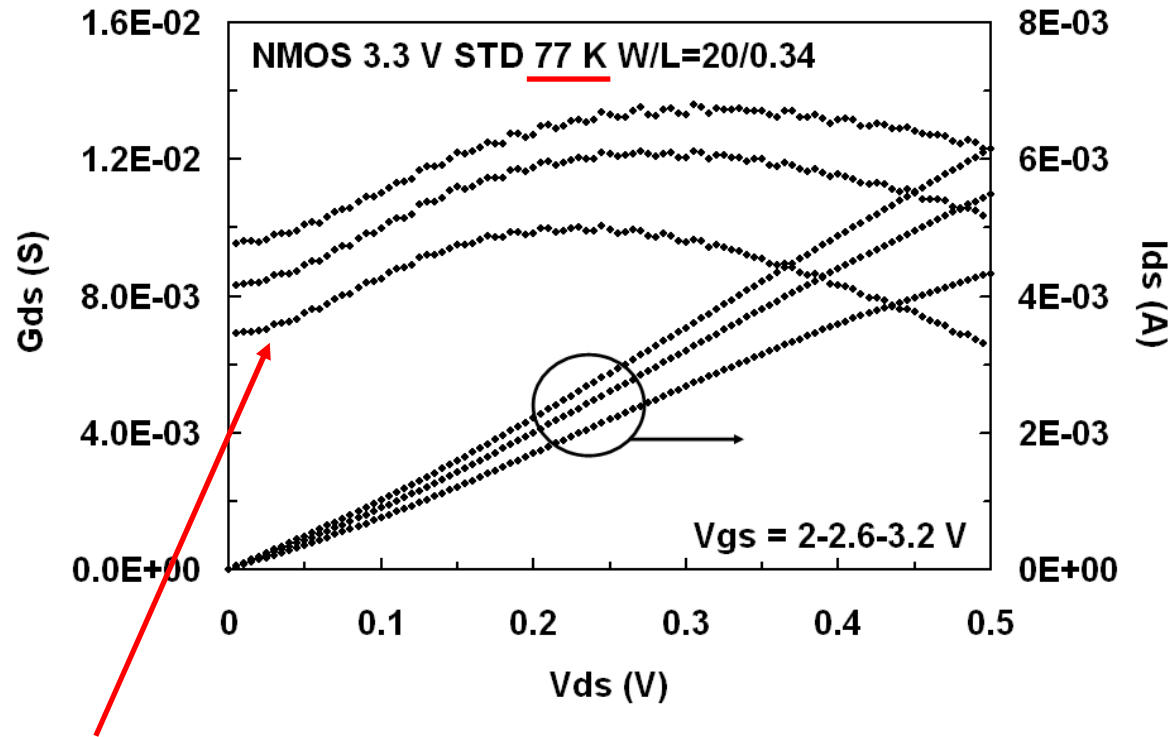
Many standard effects:

- e.g. standard INW (Inverse Narrow Width) effect in PMOS
- Temperature scaling to be improved for precise analog modeling in a wide range: 77 - 300 K

Some specific effects:

- Anomalous INW effect in NMOS
- Negative gate transconductance G_m at high V_{gs}
- Degradation of weak inversion slope
- Freeze-out effect in LDD regions
- Energy subbands quantization effect

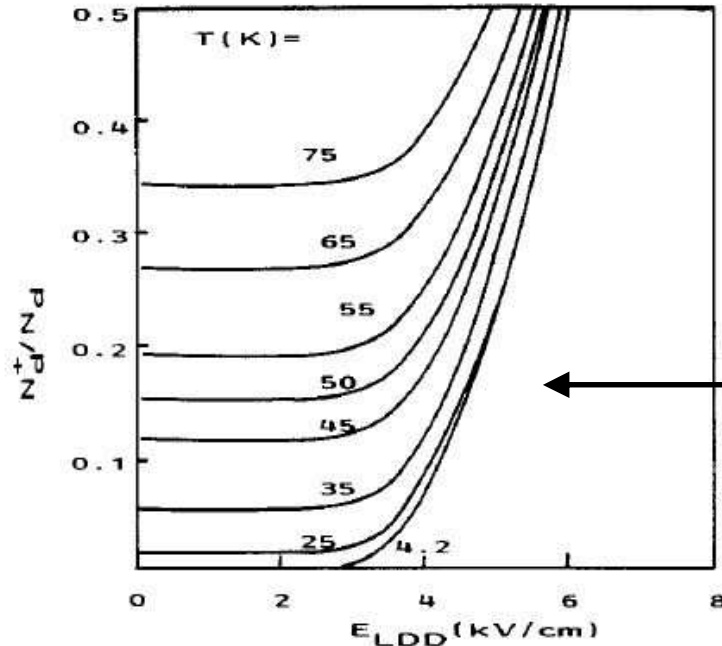
Freeze-out effect in LDD regions



- Drain conductance G_{ds} decreases at low V_{ds} due to impurity freeze-out in LDD regions at LT (only when $T < 130$ K, depending on N_{LDD})
- De-freezing at high V_{ds} due to impurity ionization assisted by lateral electrical field (shallow level impact ioniz. effects)

Modeling of freeze-out effect in LDD

I.M. Hafez *et al.*, SSE, 38(2), 419-424 (1995)



Increase of source-drain series resistance due to freeze-out:

$$R_{SD}(E_{LDD}) = R_{min} \frac{1}{Nd^+/Nd}$$

$$Nd^+/Nd = 1 + (Nd_0^+/Nd - 1) / (1 + \gamma)$$

$$\gamma = \gamma_0 \exp(-B / E_{LDD})$$

Nd^+/Nd : fraction of ionized impurities

R_{min} : min. R_{SD} when all impurities are ionized

// `ekv3_parameters.va` - New parameters for modeling freeze-out effects in LDD zones:

parameter real F_LDD	= 0	from [0:1]; ---> Flag pour simuler sans ou avec gel dans LDD
parameter real L_LDD	= 1.0E-7	from [1.0E-8:1.0E-7]; ---> Longueur des zones LDD, en mètre
parameter real B_LDD	= 6.0E6	from [1.0E6:1.0E7]; ---> Paramètre B dans eq (8), en Volt/mètre
parameter real G_LDD	= 100	from [1:1000]; ---> Pré-facteur gamma0 dans eq (8), pas d'unité
parameter real ND_LDD	= 0.5	from [0.1:1.0]; ---> Fraction de donneurs ionisés à une température donnée, en l'absence de champ électrique latéral notée Nd_0^+/Nd dans eq (7b)

Modeling of freeze-out: modifications in ekv3.va

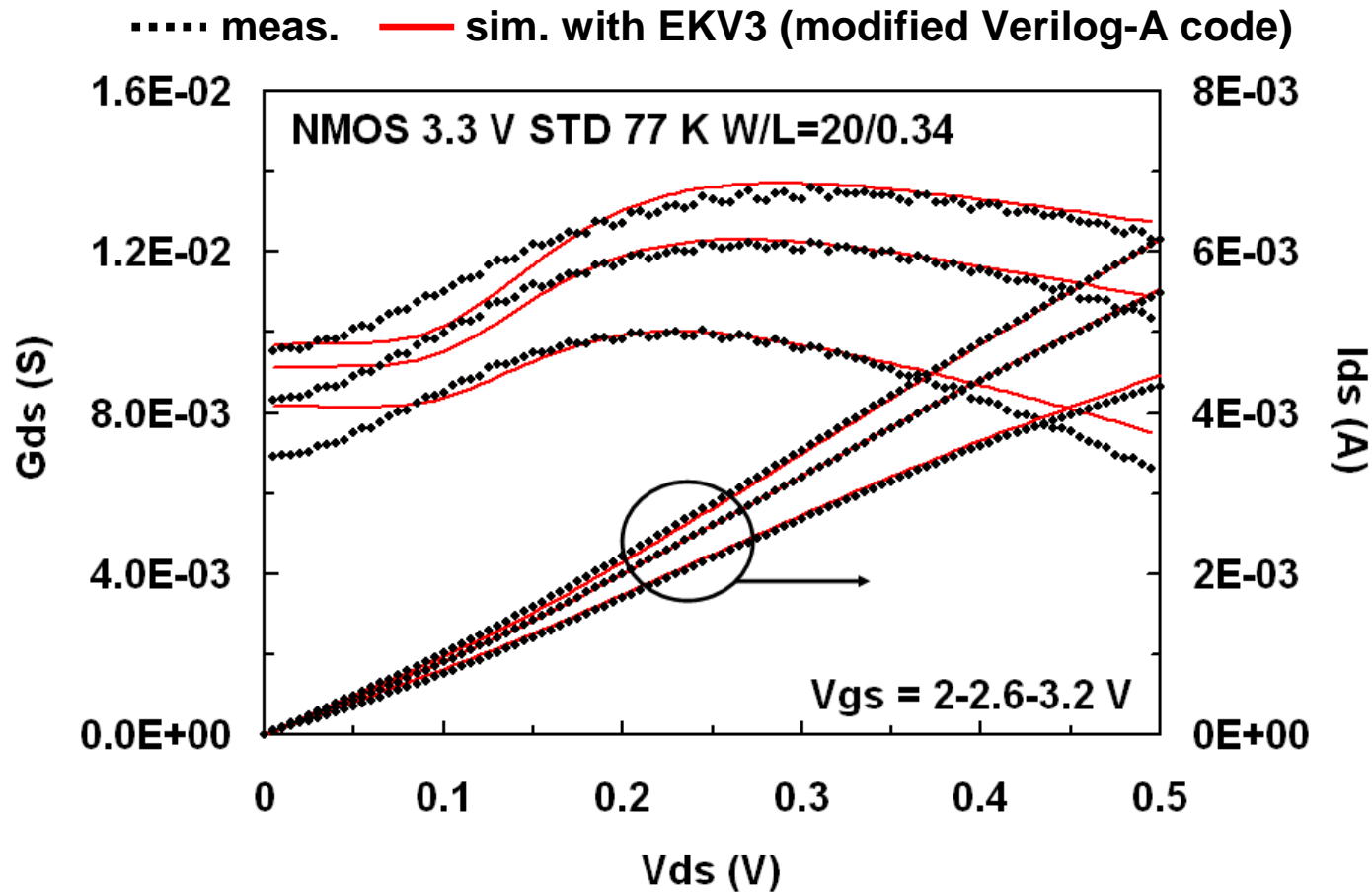
```

`ifdef DC_S
// SERIES RESISTANCE
  tmp = abs((VD-VS)) / (L_LDD + 1.0e-9); ---> electric field ELDD, Hafez eq. (3)
  if (tmp == 0.0)
  begin
    Gamma = 0.0;
  end
  else
  begin
    Gamma = 1.0E-9 + G_LDD*exp(-B_LDD/tmp); ---> Hafez eq. (8)
  end
  Nd = 1.0 + (ND_LDD - 1.0)/(1.0 + Gamma); ---> Hafez eq. (7b)
  rs_new = rs; ---> unmodified RS
  if (F_LDD == 0.0)
  begin
    rd_new = rd;
  end
  else
  begin
    rd_new = rd / abs(Nd); ---> Hafez eq. (9)
  end
  IDS = IDS / (1.0 + (rs_new * Ispec / UT) * qs + (rd_new * Ispec / UT) * qdp);
// IDS
---> ekv3 code continuation

```

Non linear field-dependent
drain resistance

Freeze-out effect in LDD regions



- Fair agreement obtained with the Hafez model with impact ioniz.
- Strong impact of these regions during characterization traditionally made in the linear regime ($V_{ds} \leq 50$ mV) \Rightarrow artifacts in $V_{th}(L)$ extractions

Subbands quantization effect

Peak in G_m for moderate inversion, only on lightly doped and long NMOSFET ($< 8 \cdot 10^{16} \text{ cm}^{-3}$)

⇒ Subbands quantization effect

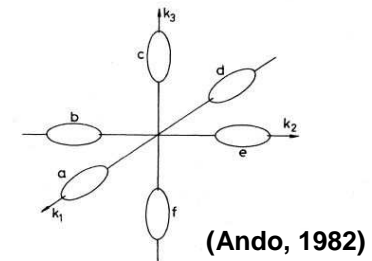
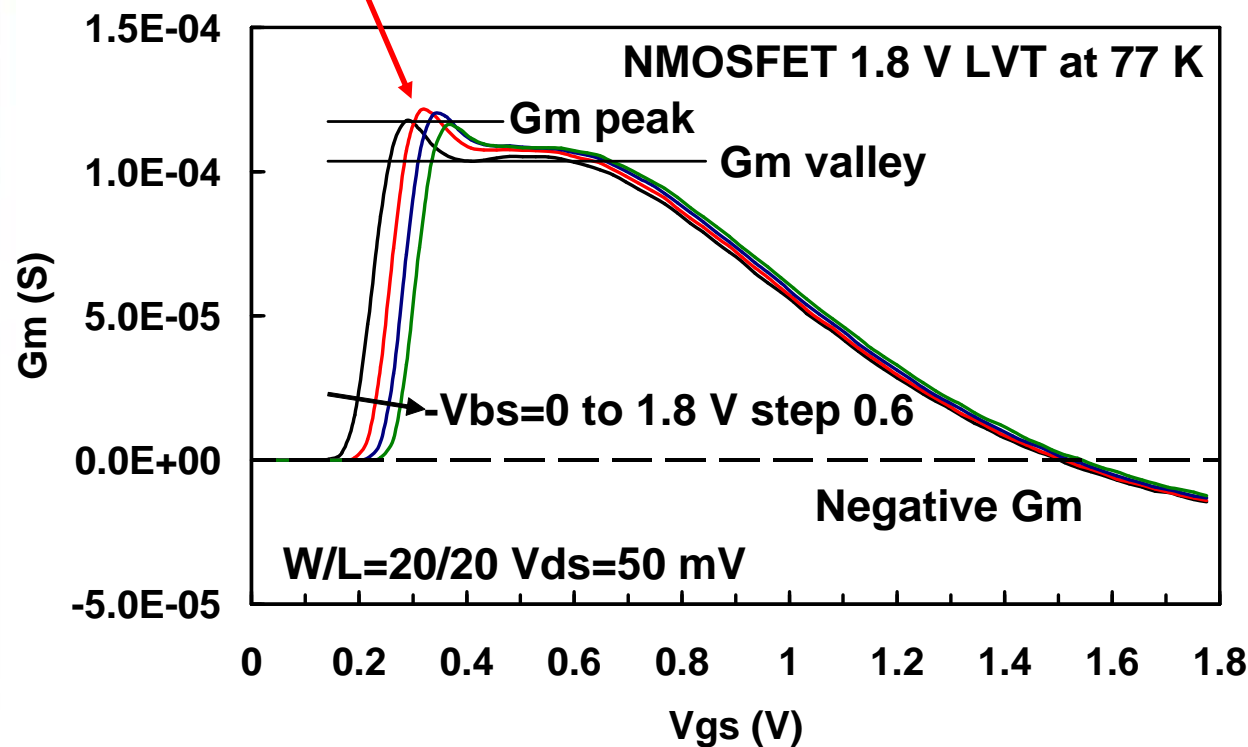
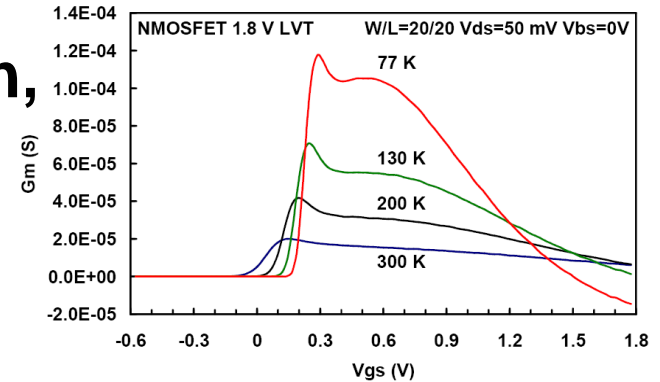
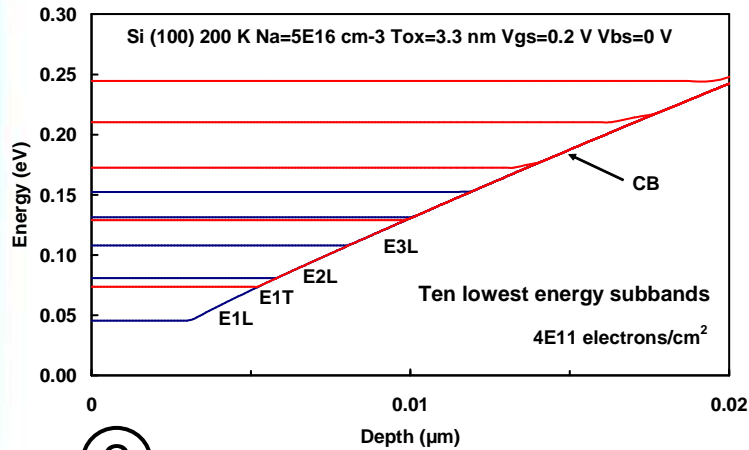


FIG. 5. Schematic constant-energy surfaces for the conduction band of silicon, showing six conduction-band valleys in the $\langle 100 \rangle$ direction of momentum space. The band minima, corresponding to the centers of the ellipsoids, are 85% of the way to the Brillouin-zone boundaries. The long axis of an ellipsoid corresponds to the longitudinal effective mass of electrons in silicon, $m_l=0.916m_0$, while the short axes correspond to the transverse effective mass, $m_t=0.190m_0$.

Subbands quantization effect: Numerical 2D simulations with Atlas (Silvaco)

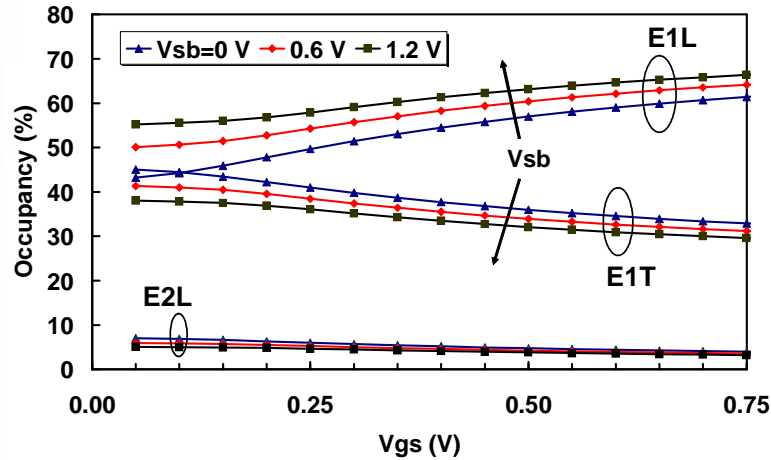
①



Poisson-Schrödinger simulations:

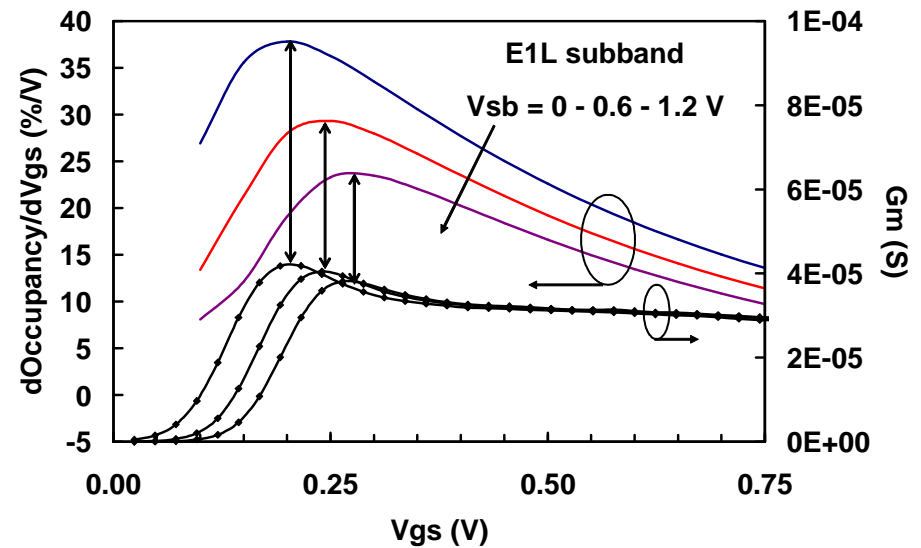
- Si (100) ; $m_L=0.916 m_0$; $m_T=0.19 m_0$
- degeneracy: $g_L=2$; $g_T=4$
- $N_A=5 \times 10^{16} \text{ at/cm}^3$; $T=200 \text{ K}$; $T_{ox}=3.3 \text{ nm}$

②



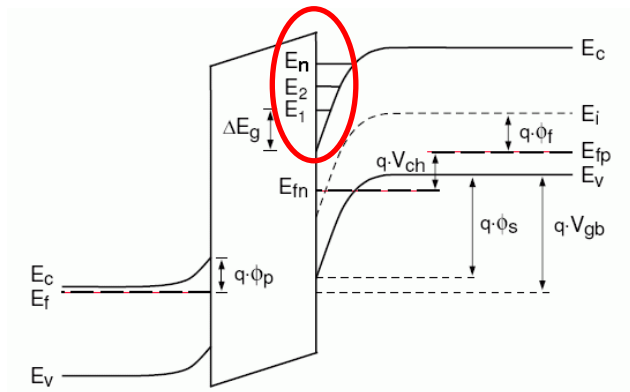
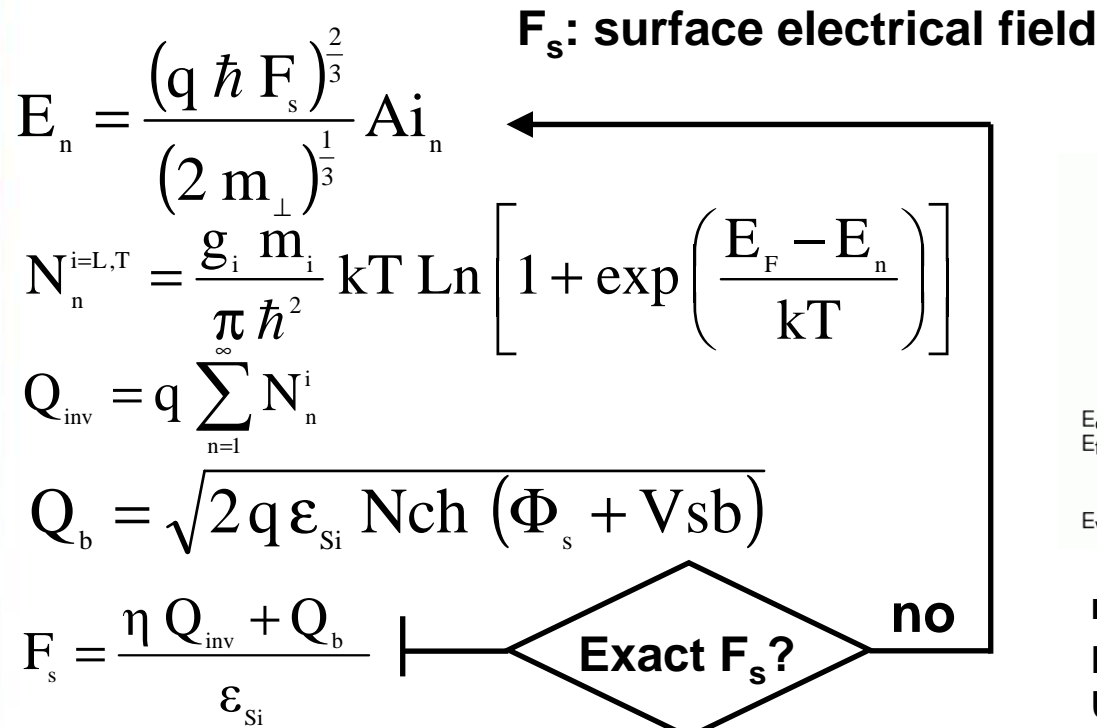
Occupancy \Leftrightarrow Drain current

③



dOccupancy/dVgs \Leftrightarrow Gm

Toward compact modeling of subbands quantization effect?



n-MOSFET energy band diagram
From F. Prégaldiny, PhD
U. Strasbourg (2003)

$$\mu = \mu_0 / \left[\left(\frac{Q_{inv}}{Q_c} \right) + \left(\frac{Q_c}{Q_{inv}} \right)^{\alpha-2} \right]$$

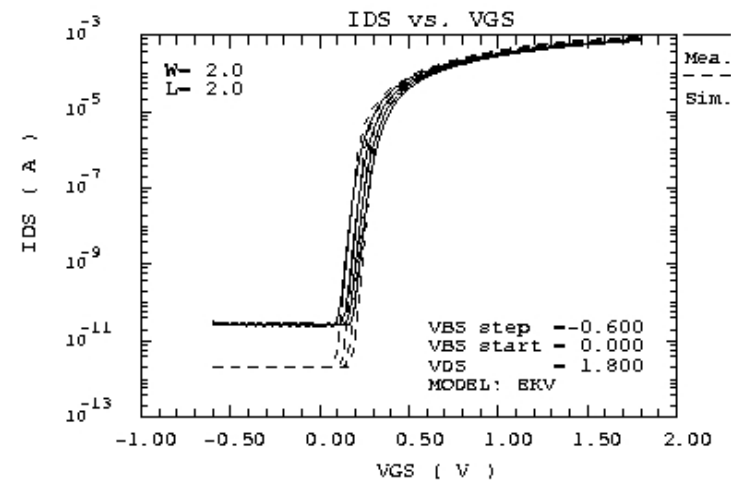
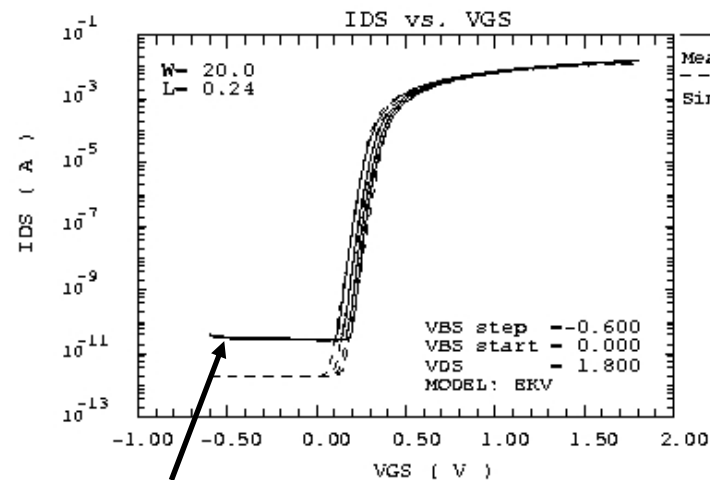
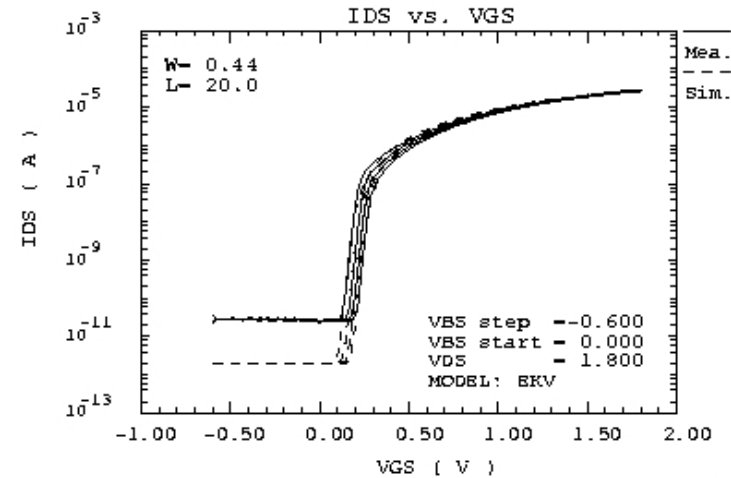
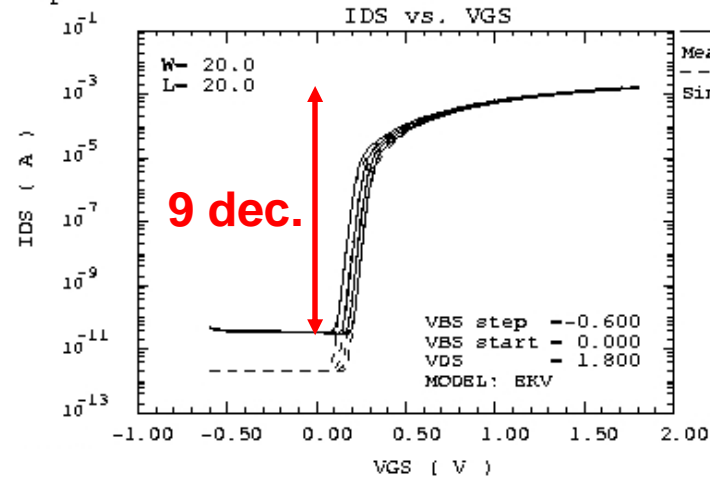
A. Emrani, PhD INP Grenoble (1992)

$$I_{ds_Lin} = \frac{W}{L} V_{ds} (\mu_{1L} Q_{inv}^{1L} + \mu_{1T} Q_{inv}^{1T} + \mu_{2L} Q_{inv}^{2L} + \dots)$$

EKV3 + 1.8 V NMOS LVT at 77 K

Ids-Vgs in Log scale, Vds=1.8 V, after parameter optimization

Run by : SCME
Process : CMOS
Temp. : -196



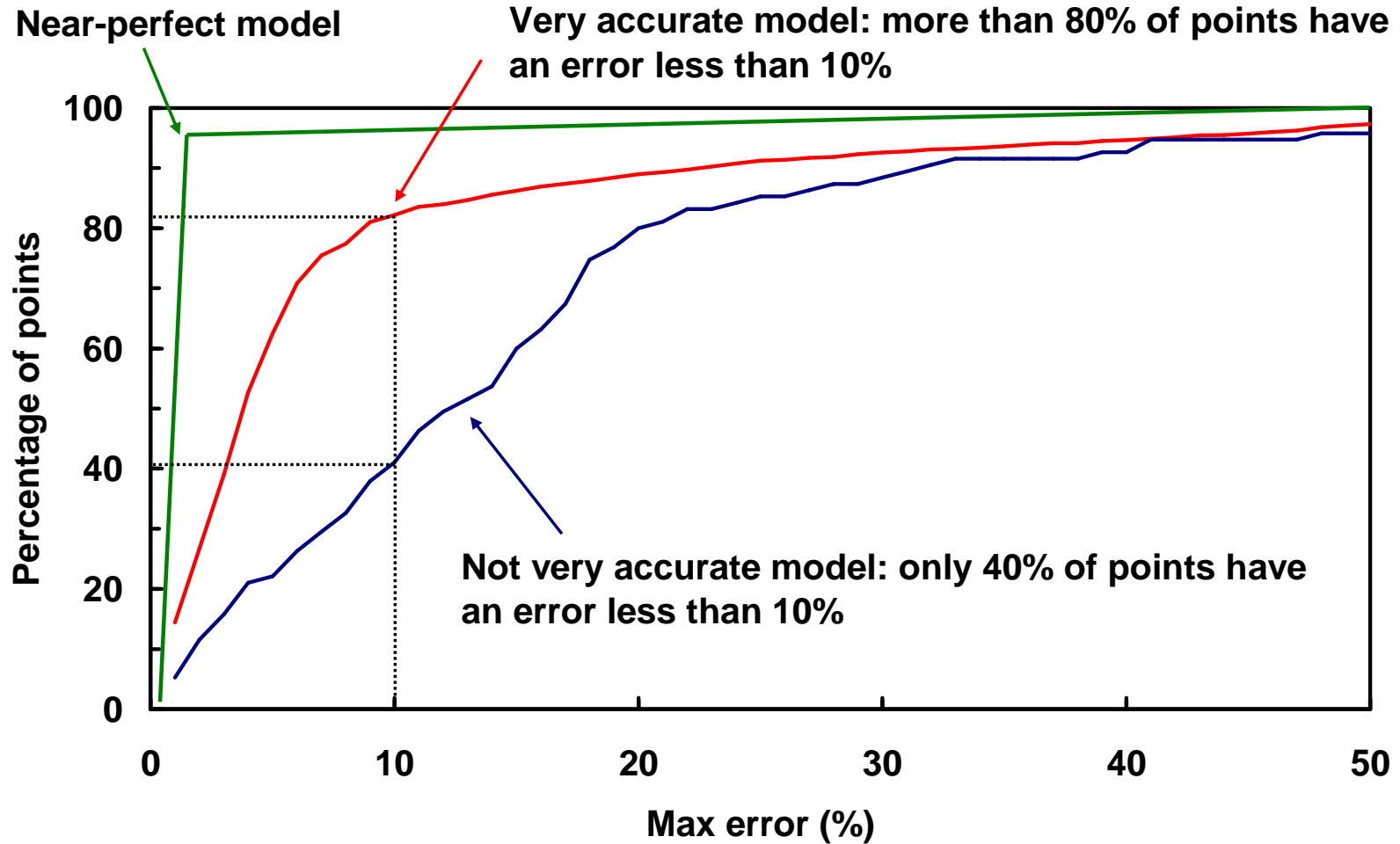
Leakage current due to measurements in cryostat

How to compare two compact models for analog/digital applications?

- Choose one family of MOSFETs: NMOS 1.8 V LVT
- Choose one temperature: 300 K, 77 K
- Choose one model: EKV3, PSP (HiSIM2 not evaluated)
- Choose MOSFET with different W/L (20/20, ... Wmin/Lmin) representative of the design (transistors in the pixel for imagers)
- Perform a complete DC parameter extraction
- Evaluate errors between simulations and measurements on I_{ds} , G_m [from $I_{ds}(V_{gs})$] and G_{ds} [from $I_{ds}(V_{ds})$] in saturation (at $V_{ds}=1.8$ V) for each measurement point (in weak, moderate and strong inversion, I_{ds} from nA to mA) and each geometry
- Calculate the cumulative number of experimental points whose error is less than a fixed amount (2, 4, 6 ... 100 %)
- Normalize this figure to the total number of measurements
- Repeat the procedure (other temperature, other model)

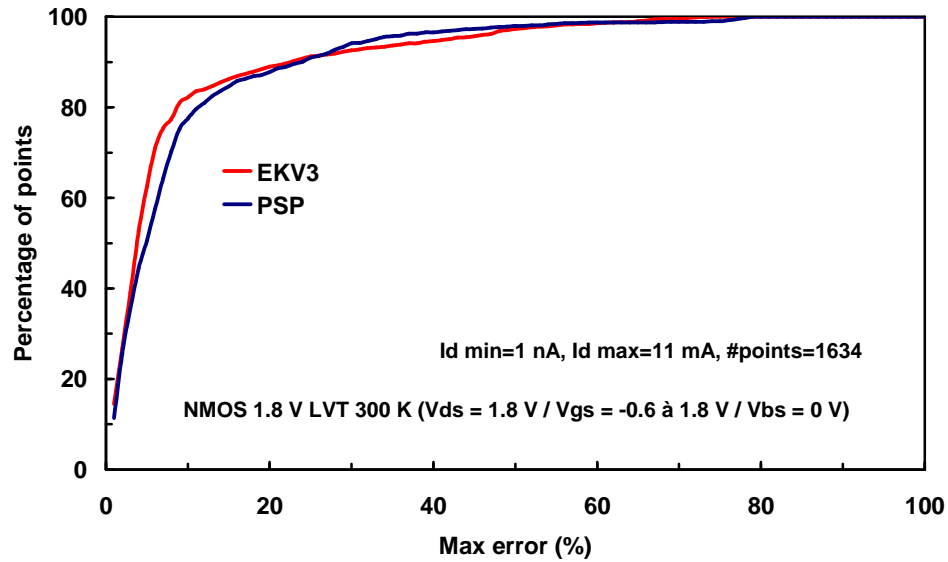
How to compare two compact models for analog/digital applications?

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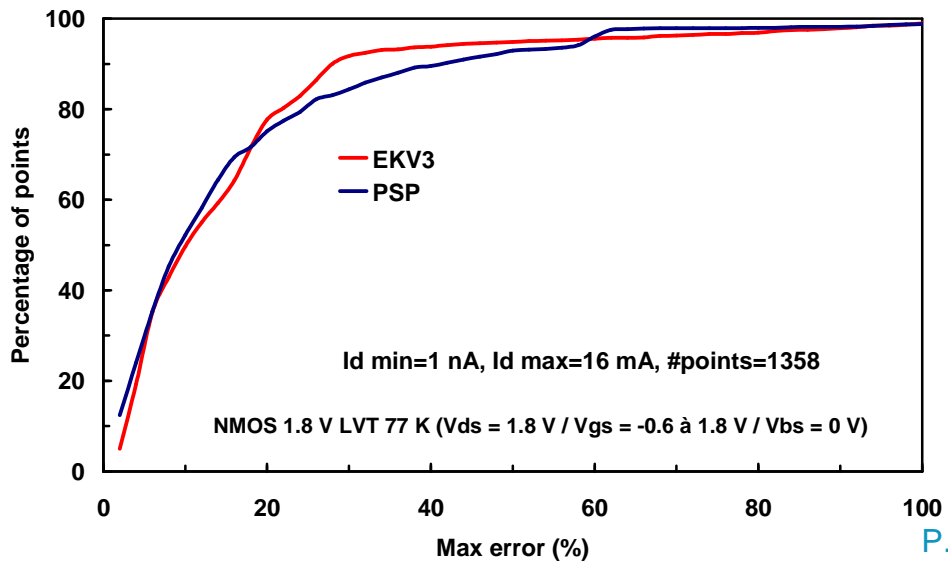


PSP vs. EKV3 at 300 K and 77 K

A - Error on drain current in saturation ($V_{ds}=1.8\text{ V}$)



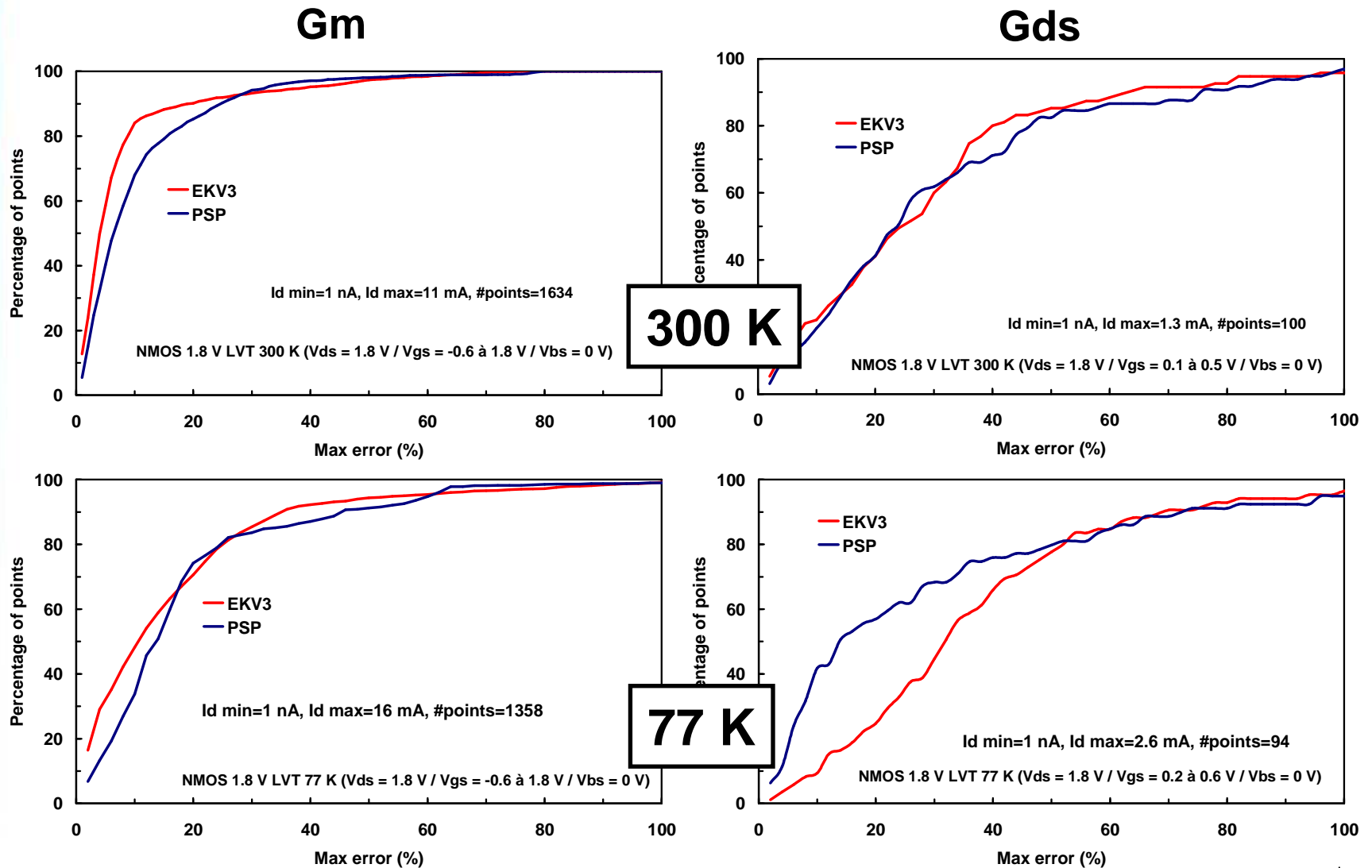
← 300 K



← 77 K

PSP vs. EKV3 at 300 K and 77 K

B - Error on drain current derivatives, G_m and G_{ds} , at $V_{ds}=1.8$ V



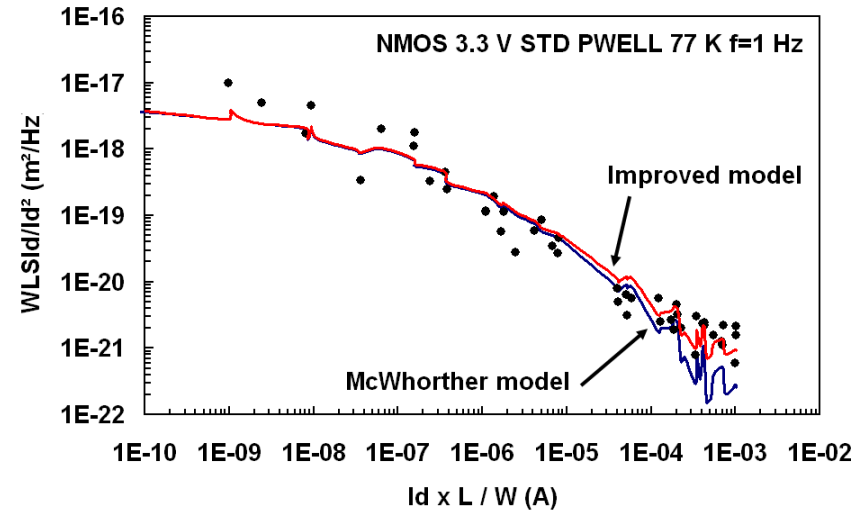
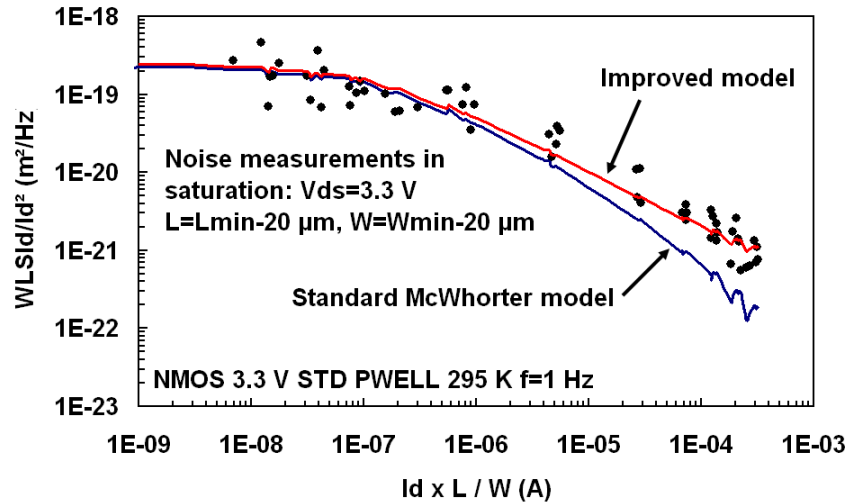
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Comparison between PSP and EKV3 for analog/digital applications

- **Both PSP and EKV3 are less accurate at LT**
- **Near the same accuracy for I_{ds} and G_m at LT**
- **EKV3 less accurate for G_{ds} at 77 K: due to parameter extraction?**

LF noise: physical mechanisms

Normalized drain current power spectral density W_{LSId}/I_d^2



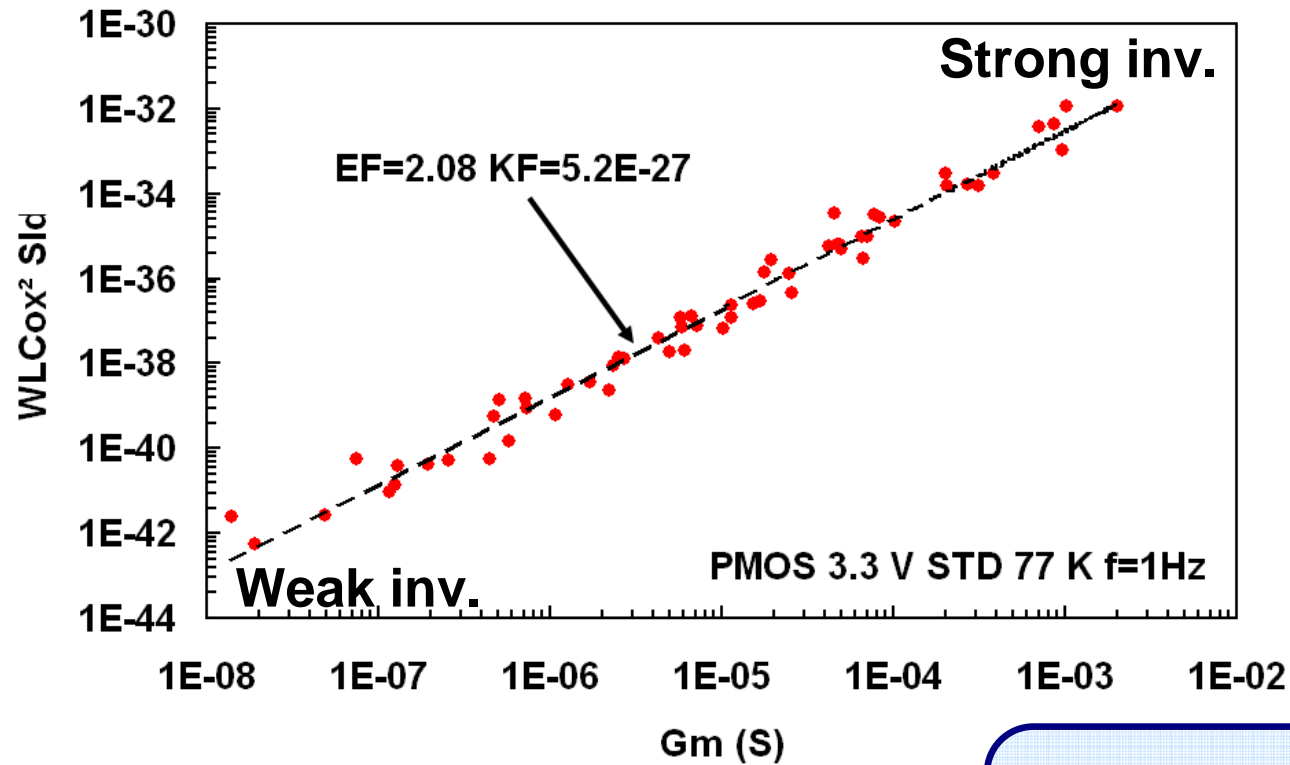
1 - Standard McWhorter carrier number fluctuations (ΔN)

Ghibaudo model:

$$S_{I_d} = \left[1 + \alpha \mu C_{ox} \frac{I_d}{G_m} \right]^2 G_m^2 S_{V_{fb}}(f) \quad [A^2/Hz]$$

2 - Correlated mobility fluctuations ($\Delta\mu$) at high current

LF noise: compact modeling



- Three parameters: KF, AF, EF ≠ 2
- Only Gm, the gate transconductance
- Simple but efficient model
- Valid in weak, moderate and strong inversion
- This is the model introduced in EKV3

$$S_{Id} = \frac{KF G_m^{EF}}{C_{ox} W_{eff} L_{eff} f^{AF}}$$

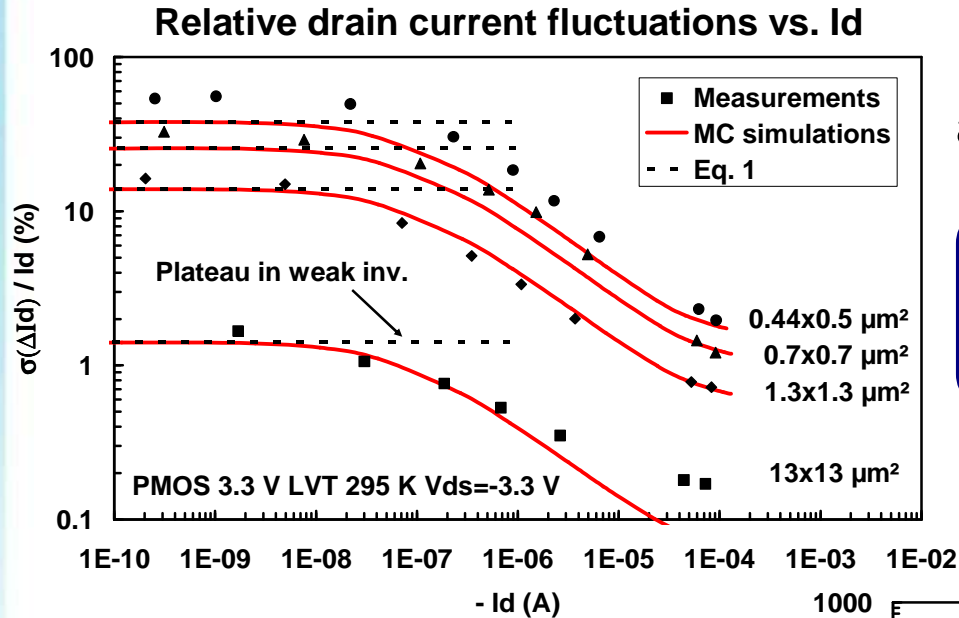
Matching of MOS transistors

Pelgrom model

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2$$

- Area (A_P) and spacing (S_P) matching parameters
- Electrical parameter $P = VT_0, \beta, \gamma$

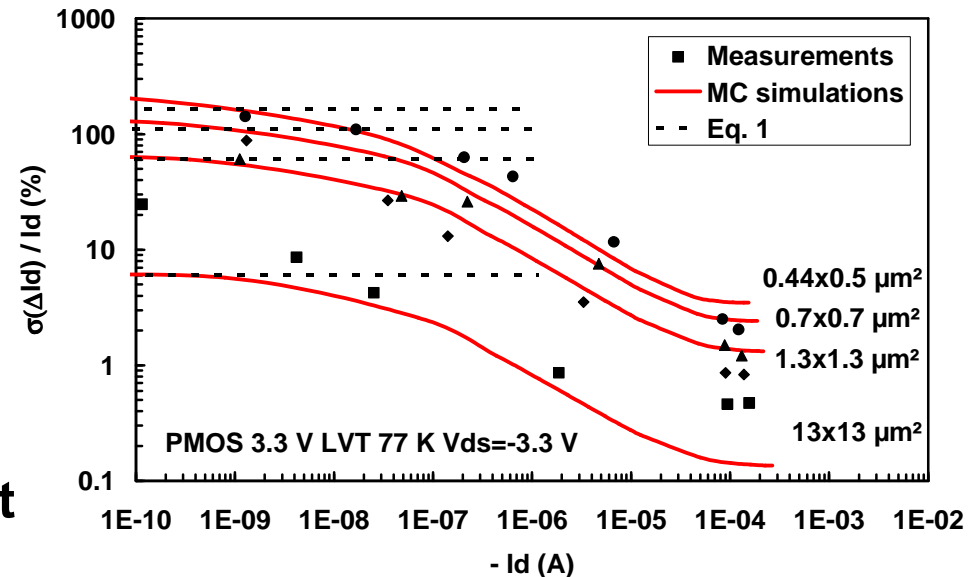
Matching of MOS transistors



MC analysis with ELDO
after EKV parameter extraction

$$\frac{\sigma(\Delta I_d)}{I_d} = \frac{1}{n U_t} \sigma(\Delta V_{T0}) \quad \text{Eq. 1}$$

- Fair agreement between measurements and MC simulations (for relative mismatch higher than ~ 0.5%)
- Higher current mismatch at low temperature



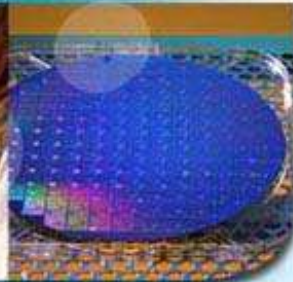
Conclusion

- **Specific & non specific physical effects observed at low temperature**
- **Analog compact modeling at ultra-low temperature is still a challenge**
- **Standard versions of EKV3 and PSP models are relatively accurate for LT modeling in weak & moderate inversion**
- **These advanced models are very interesting, even for not very aggressive technologies**
- **Some improvements are needed, e.g. freeze-out & subbands QM effects, as well as temperature modeling of non specific effects such as GIDL**

Acknowledgments

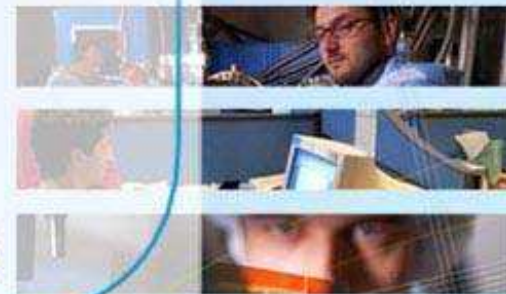
- **Pierre Castelein, Mickaël Cavelier, Raphaël Fascio, Jean-Luc Martin and Anne-Sophie Royet (CEA, Leti, Minatec)**
- **Gérard Ghibaudo (IMEP-LAHC, Minatec, Grenoble)**
- **Matthias Bucher (Tech. Univ. of Crete)**
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