Extraction of a Scalable Electrical Model for a SOI JFET

Simona Cozzi – Lorenzo Labate – Roberto Stella

Technology R&D – Smart Power & High Voltage Competence Center
Device Characterization & Modeling Group

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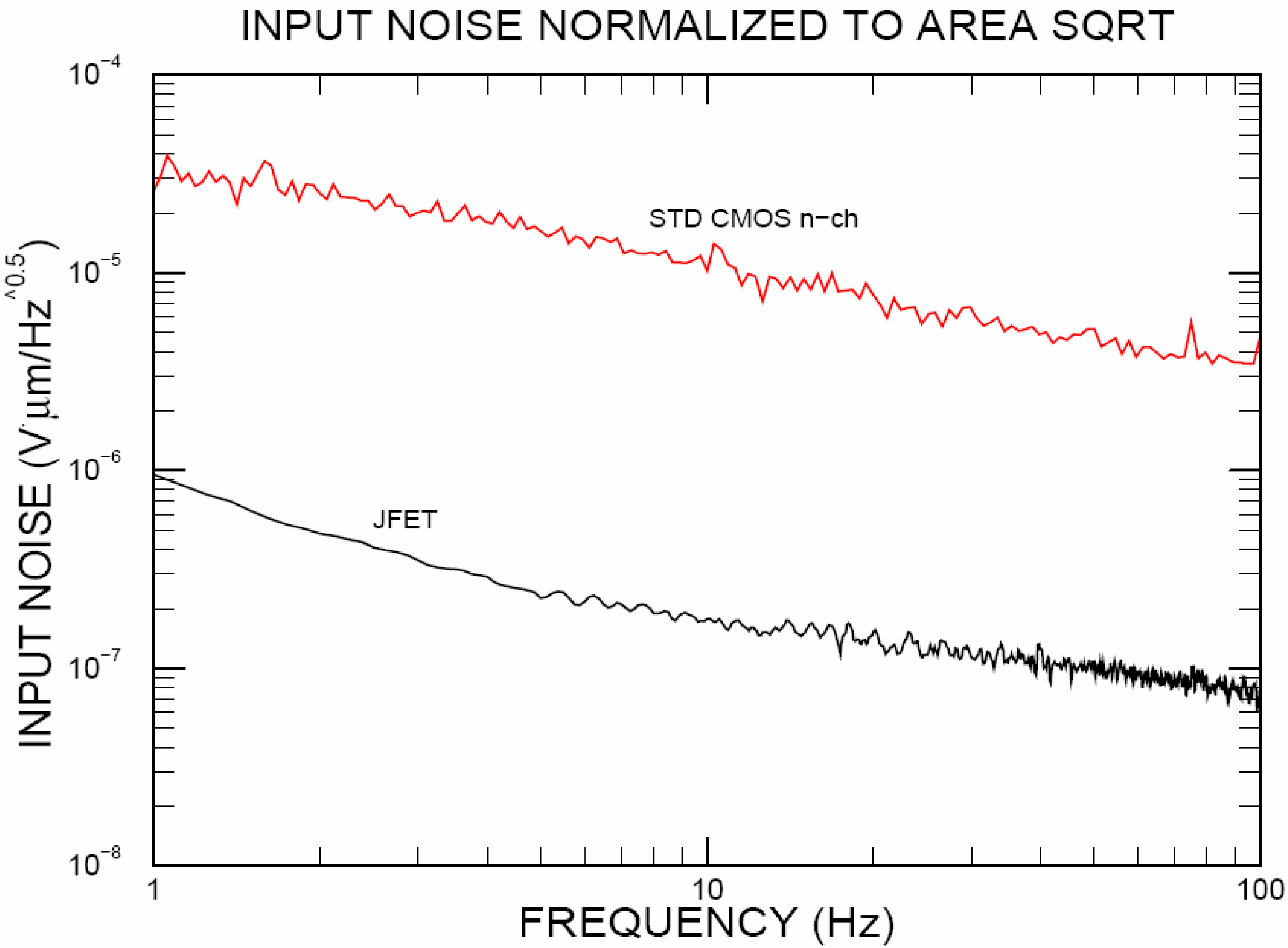
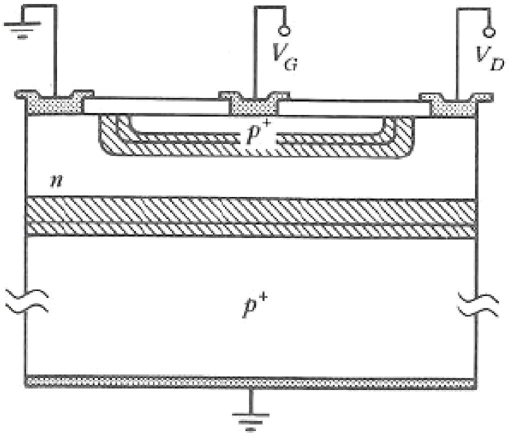
Introduction

- In microelectronic ICs requiring very low 1/f noise , JFET becomes an interesting component alternative to MOS
  - Input stage for audio application, low noise amplifier etc.
- Thanks its negative Vth, can substitute in excellent way start-up circuits, because of reduced power dissipation
  - Std start-up circuits (actives or passives) are normally on
  - JFET switch off when the circuit wakes up

Typical flicker noise comparison



Junction Field Effect Transistor

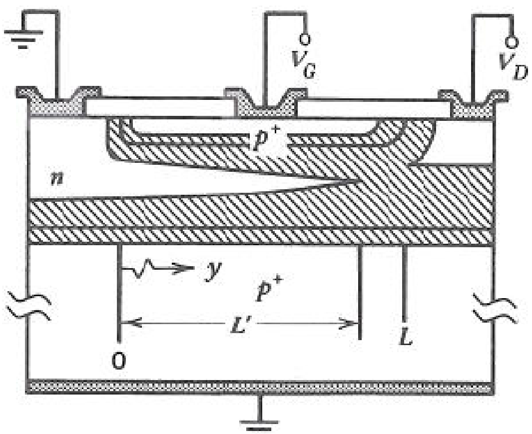


(a)

Linear Region:

$$I_D = G_0\left\{1-\left[\frac{2\varepsilon_S}{qN_d t^2}(\phi_i - V_G)\right]^{1/2}\right\}V_D$$

where $$G_0 = \frac{W}{L} q\mu_n N_d t$$



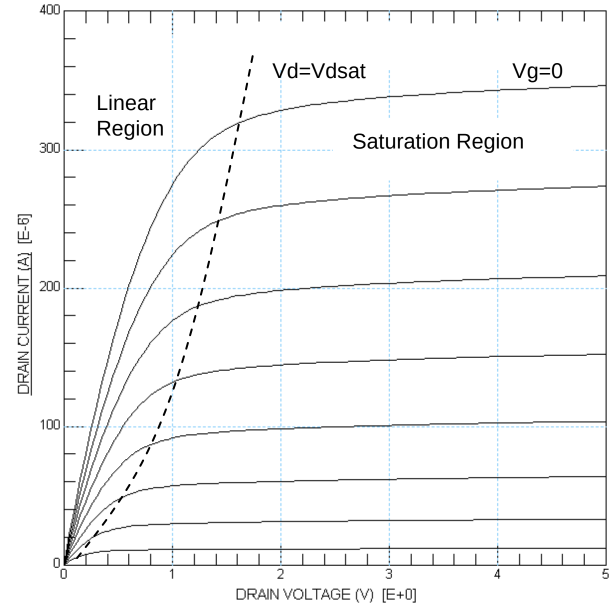
(c)

Saturation Region:

$$I_{Dsat} = G_0\left[\frac{qN_d t^2}{6\varepsilon_S} - (\phi_i - V_G)\left\{1-\frac{2}{3}\left[\frac{2\varepsilon_S(\phi_i - V_G)}{qN_d t^2}\right]^{1/2}\right\}\right]$$

$$V_{Dsat} = \frac{qN_d t^2}{2\varepsilon_s} - (\phi_i - V_G)$$

$$V_P = \phi_i - \frac{qN_d t^2}{2\varepsilon_s}$$ Pinch-off Voltage



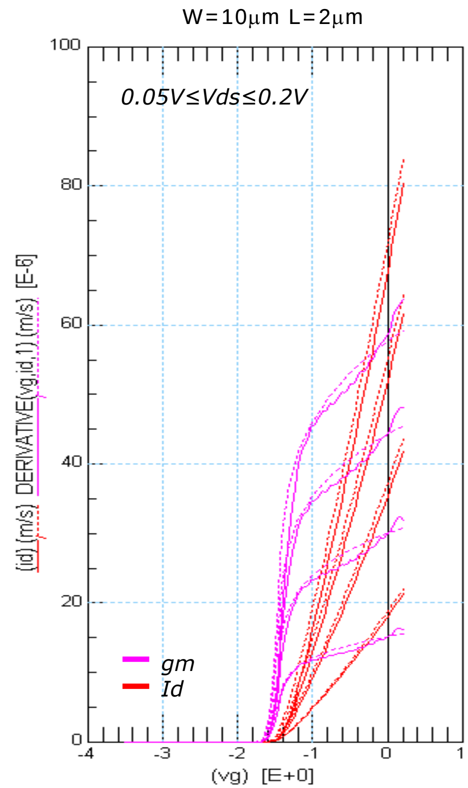
JFET Modeling - Schichman and Hodges

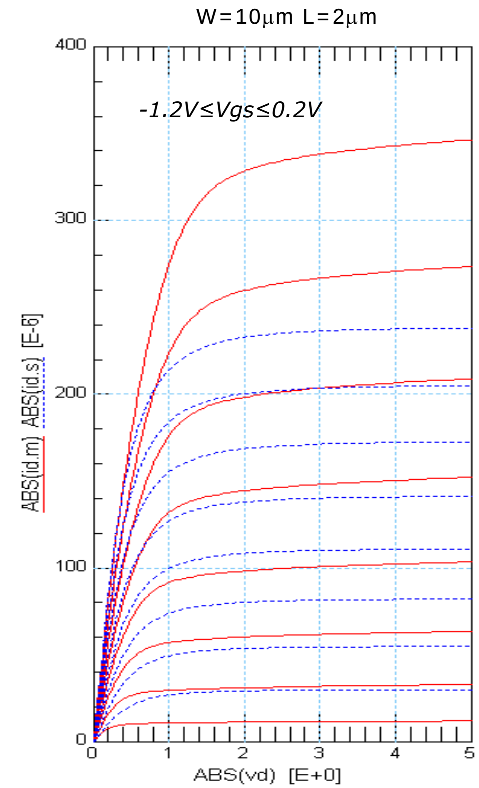
- Using Schichman and Hodges JFET and MESFET Equations:
  - From level 1 to 8 the model does not describe sub threshold region ($V_{gs} < V_t$), stating that $I_{ds}=0$
  - Level 9 describes sub threshold region, but just few parameters are present to describe both linear and saturation region

S&H Level 9 – Model accuracy

DC RELATED PARAMETERS

	Description
VTO	Zero Bias Vth
ALPHA	Parameter influencing Vsat
BETA	Transconductance coeff.
LAMBDA	Channel Length modulation Coeff.
GAMMA	Static feedback param.
DELTA	Output feedback param.
Q	Power-law param.
IS	Gate junction saturation current
N	Gate junction emission coeff.
K	Vds moltiplication factor



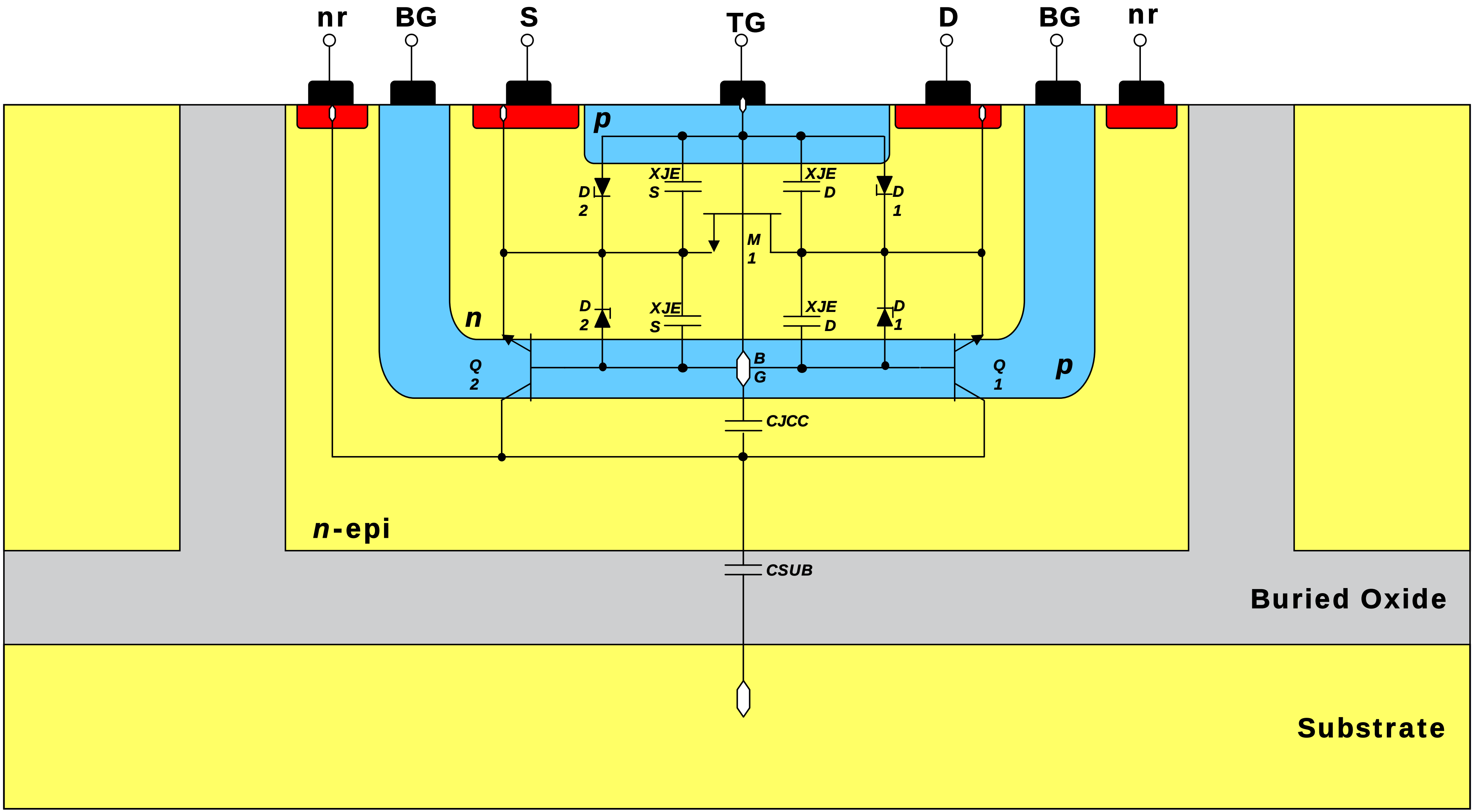


Exp.
Sim.

JFET Modeling – BSIM3

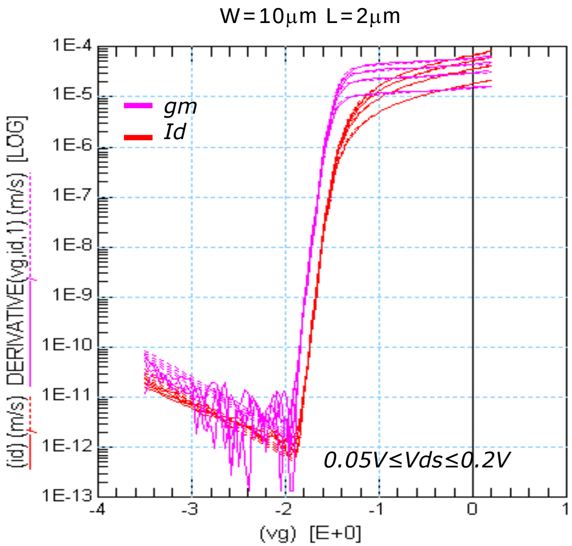
- New approach: BSIM3.
  - BSIM3 is a physics-based, accurate, scalable and predictive MOSFET SPICE widely adopted for circuit simulations.
  - *Strength*:
    - accurate in all regions, scalable, largely tested and easy to be extracted
  - *Drawback*:
    - BSIM 3 describes MOS, but
      - no Gate oxide is present in a JFET
      - JFET has two Gates
  - *Problem solution*:
    - BSIM3 includes a parameter which allows to adjust Gate Oxide thickness for CV model: DTOXCV. That parameter has been appropriately set to null Gate capacitance which is externally added
    - Bottom Gate can be considered as MOS Body terminal

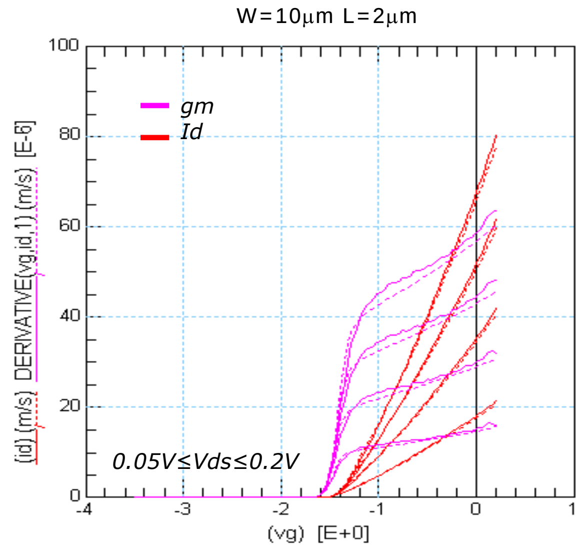
SOI JFET - Modeling strategy



Model accuracy - All regions @T= 25°C

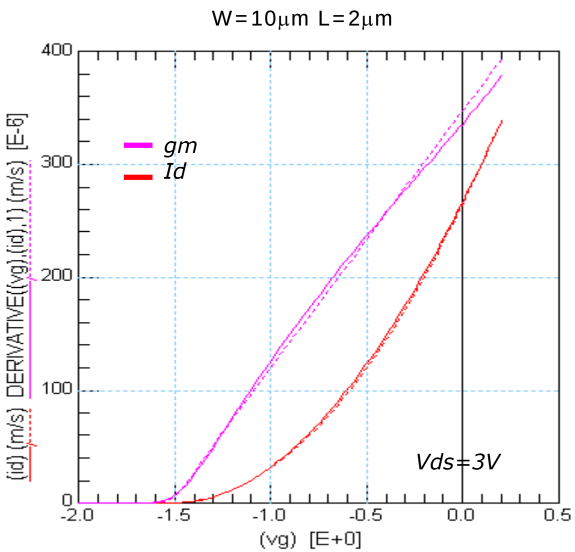
Sub-Threshold linear region

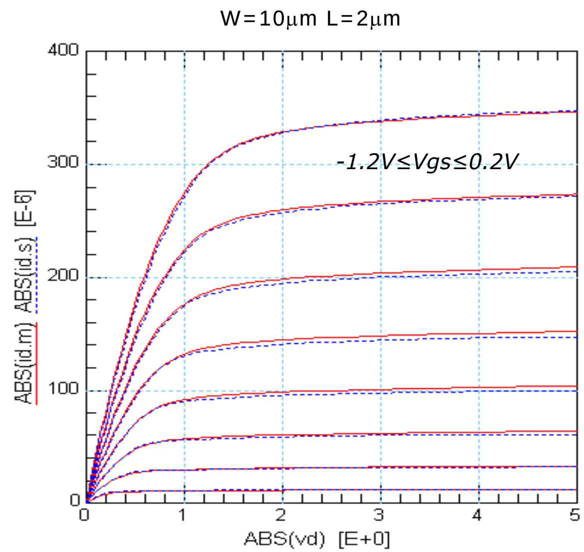




Linear region

Saturation region





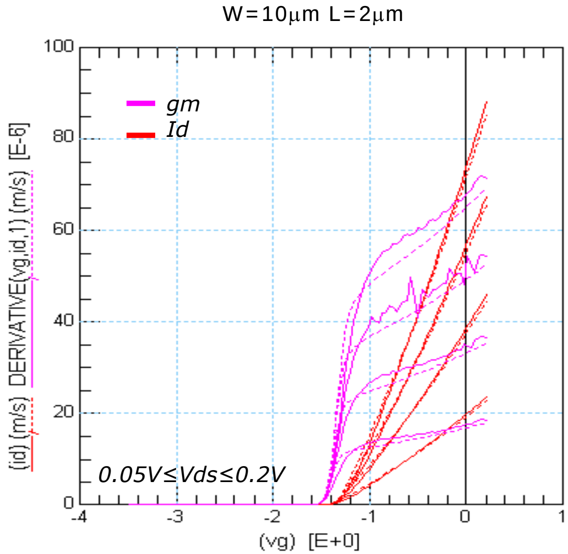
Output Characteristics

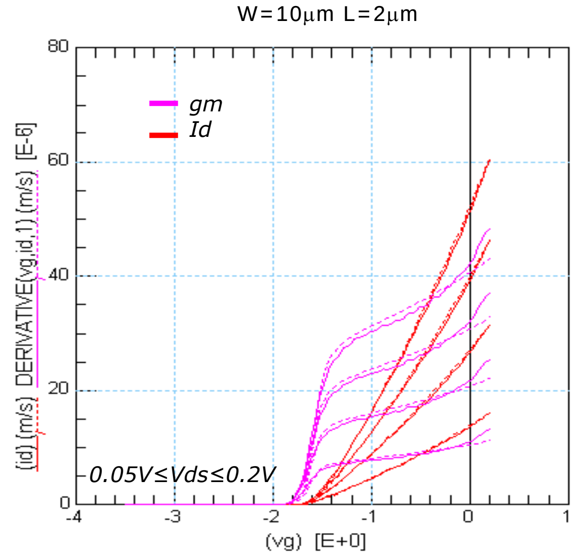
Exp.

Sim.

Model accuracy – Linear and Output Char. vs Temperature

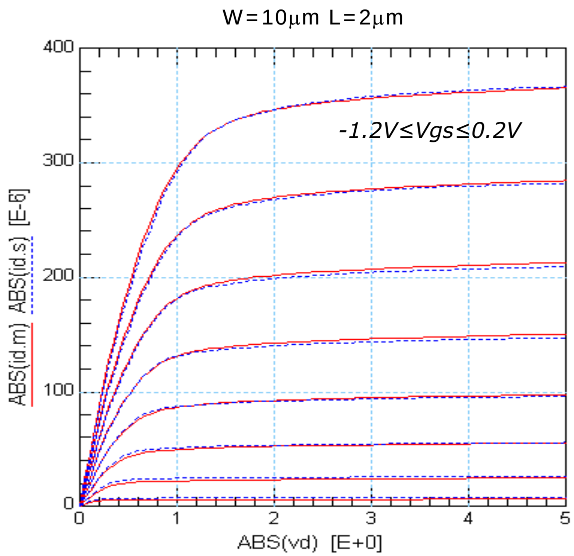
Linear region
T= -40°C

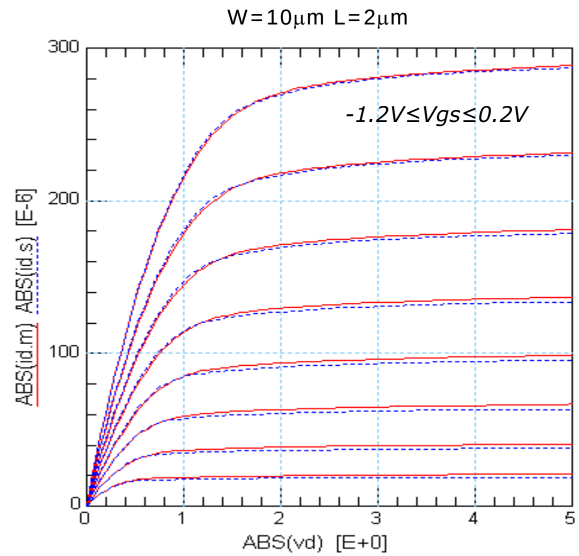




Linear region
T= 150°C

Output Characteristics
T= -40°C



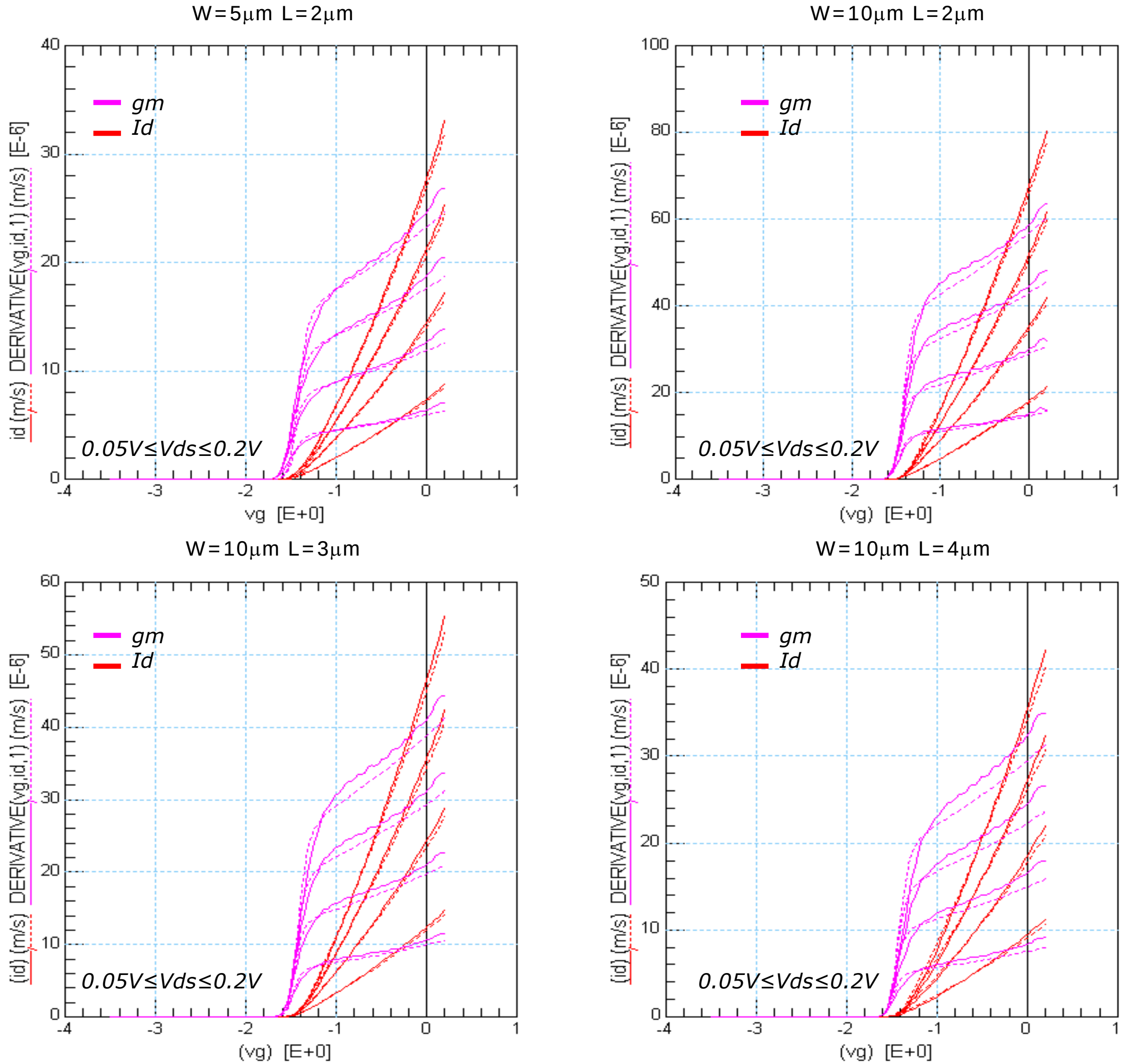


Output Characteristics
T= 150°C

Exp.
Sim.

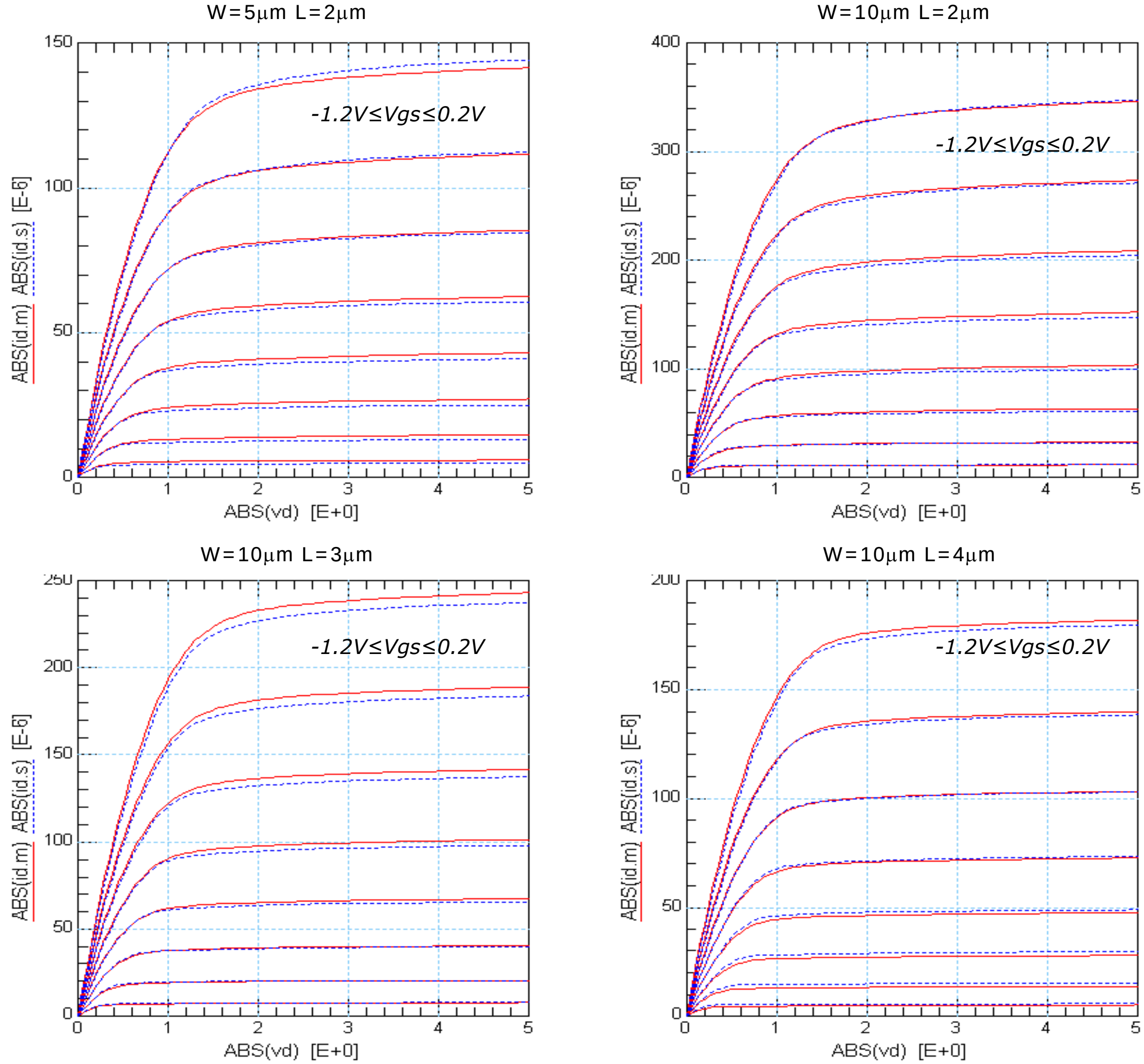
Model accuracy –
Model scalability @T= 25°C /1

Linear region



Exp.
Sim.

Model accuracy –
Model scalability @T= 25°C /2

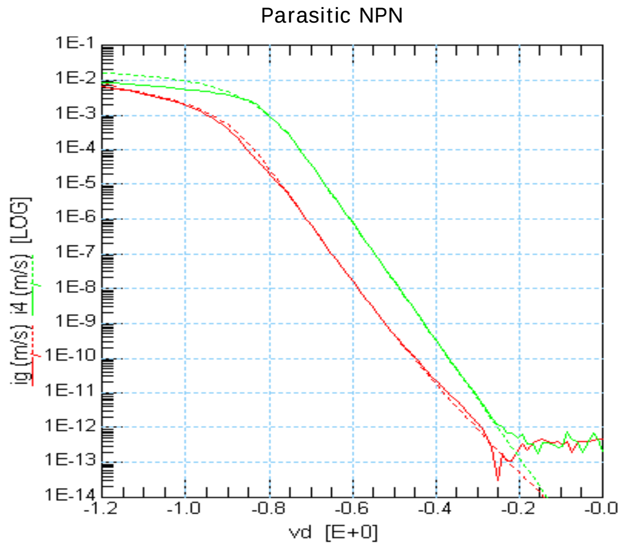


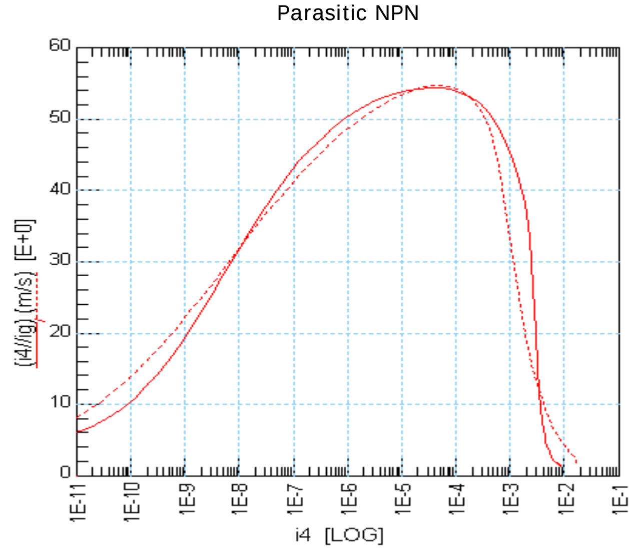
Output Characteristics

Exp.
Sim.

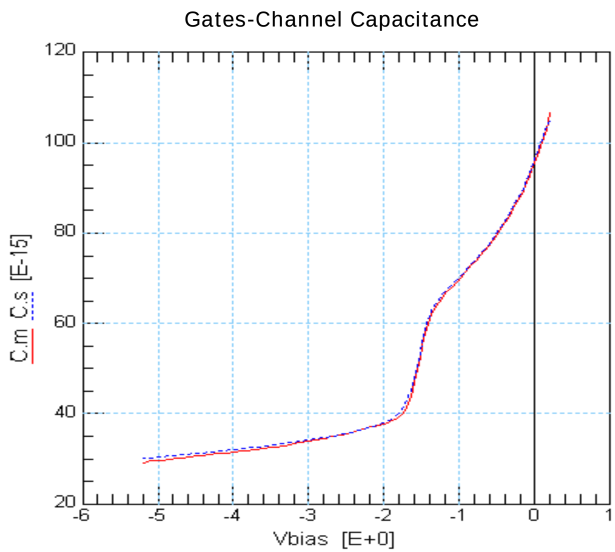
Model Accuracy –
Parasitic elements and Capacitances

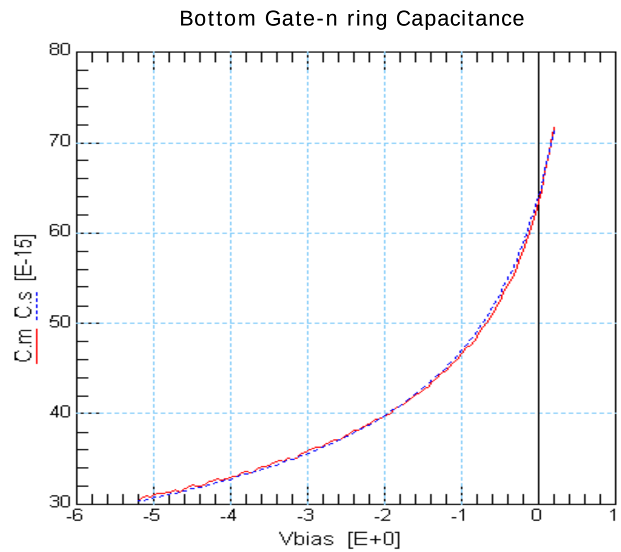
Gummel Plot





Beta



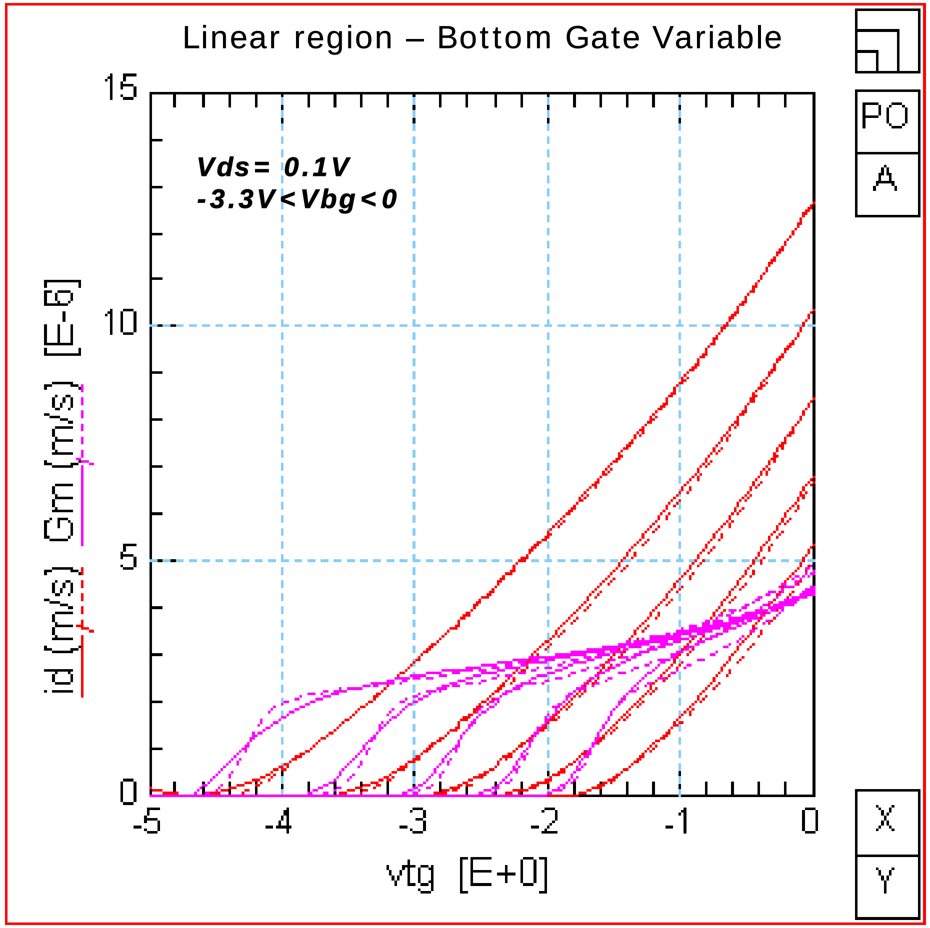


Exp.

Sim.

Model Accuracy – Bottom Gate as Body

- The two Gates can be biased separately .For example signal can be applied just to Top Gate to avoid large parasitic capacitance related to Bottom Gate
- Relationship of Body effect can easily reproduce the Bottom Gate driving
- Good Accuracy reached



Exp.
Sim.

Conclusions

- Accurate electrical models have been done using a sub circuit in which JFET has been described with MOS equation and parasitic elements.

- BSIM3 can accurately describe also Junction Field Effect Transistor electrical behaviors.

Acknowledgments

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End of Presentation

Thank you for your attention