A physics-based model for Charge-Trapping memory simulation

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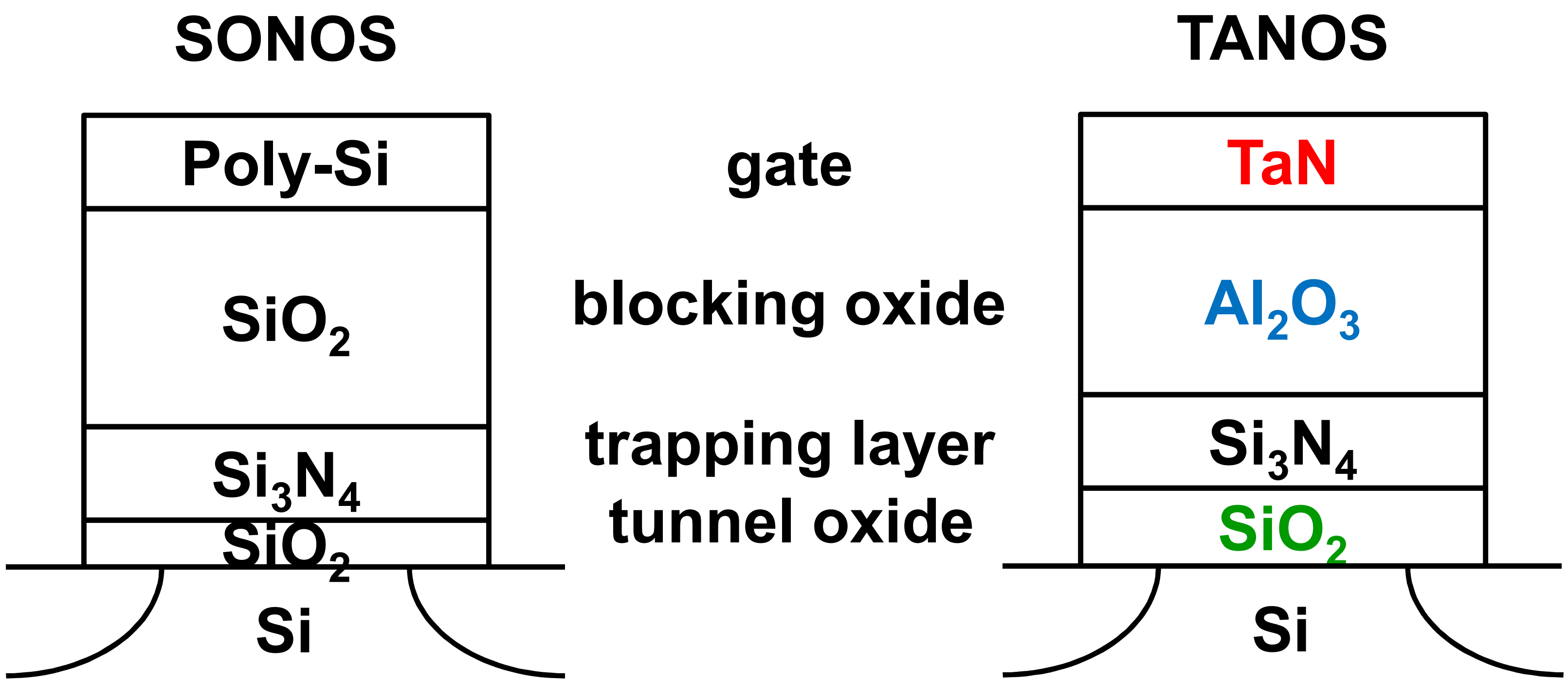
Purpose

- Charge-trapping devices like TANOS are a promising candidates to replace Floating Gate memories
- Understanding the physical mechanisms governing device operation is fundamental for performance and reliability optimization
- This requires accurate simulation models
- We present results obtained with a physical model accounting for both charge trapping in alumina and temperature effects

Outline

- Introduction
- Physical Model
- Model Results
  - Program and Erase operations
  - Charge Separation Experiments
  - Charge Trapping into Alumina
  - Effects of Temperature
- Toward a SPICE-like model of the TANOS cell
- Conclusions

Introduction

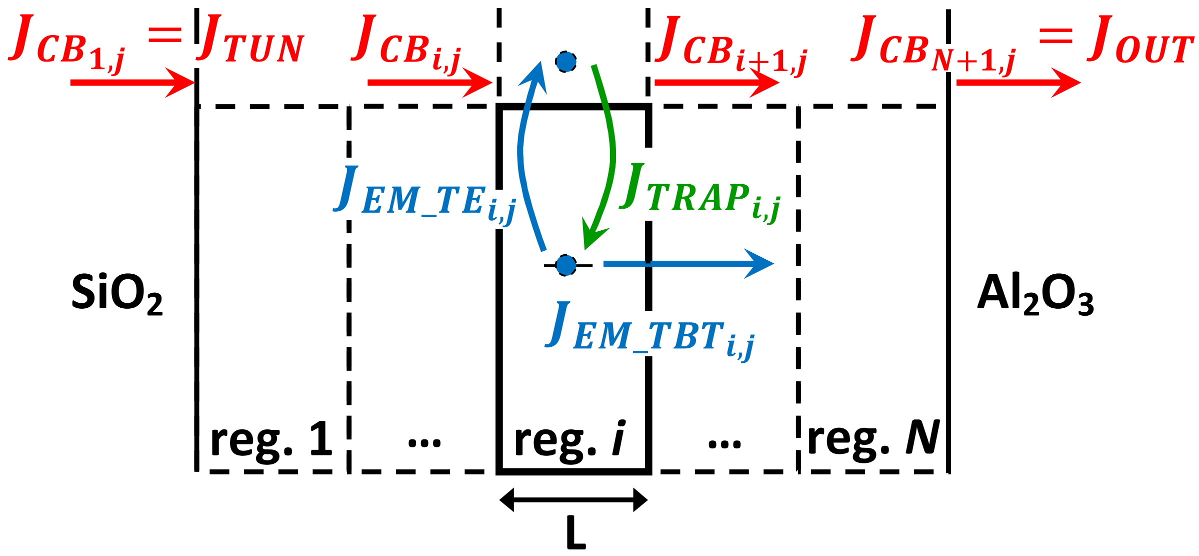


- Better retention (thicker tunnel SiO_2)
- Improved program/erase speed (high-k)
- Improved erase V_T saturation level (metal gate)

C. H. Lee *et al*., IEDM Tech. Dig., 2003, p. 613

Physical Model

- **Charge trapping and transport across the stack is described by a set of differential equations solved by discretizing space and time (indexes *i* and *j*)**

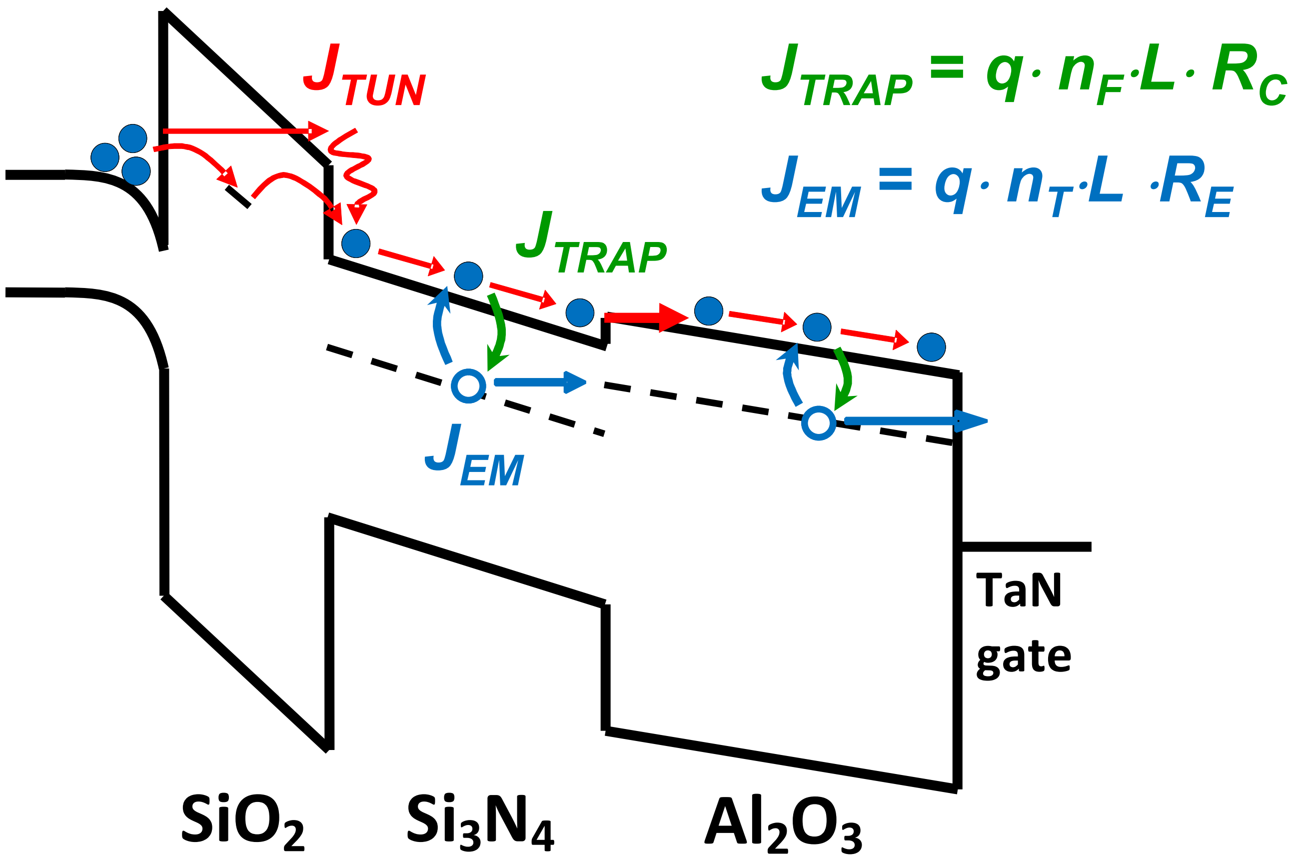


$$J_{CB\,i,j} = q\mu\left[n_{F\,i,j} F_{i,j-1} + \frac{k_B T}{q} \frac{n_{F\,i,j} - n_{F\,i+1,j}}{L} \right]$$

$$\frac{qL\left(n_{F\,i,j} - n_{F\,i,j-1}\right)}{t_j - t_{j-1}} = J_{CB_{i,j}} - J_{CB_{i+1,j}} + J_{EM\,i,j} - J_{TRAP\,i,j}$$

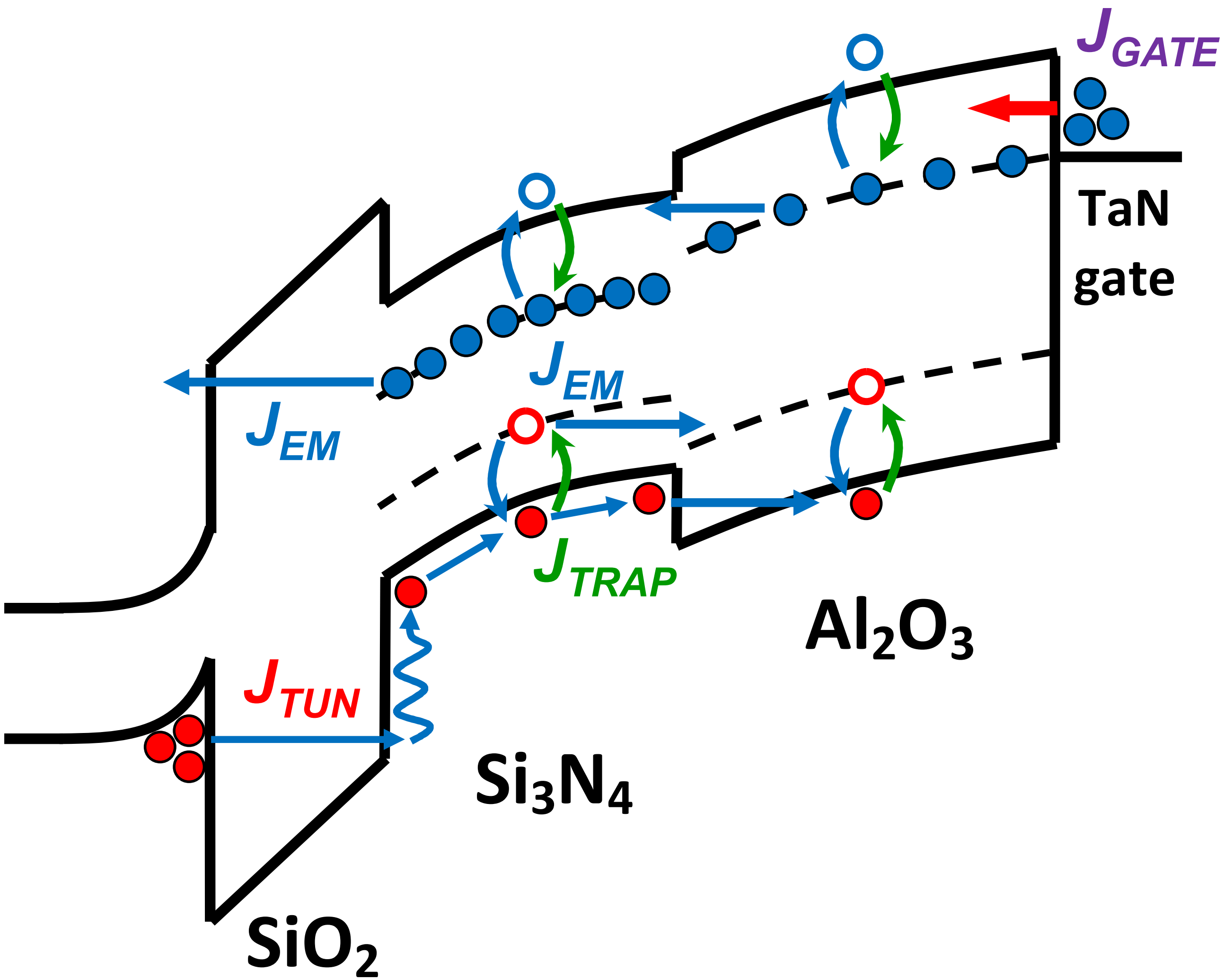
$$\frac{qL\left(n_{T\,i,j} - n_{T\,i,j-1}\right)}{t_j - t_{j-1}} = J_{TRAP\,i,j} - J_{EM\,i,j}$$

Physical Mechanisms: Program



- J_{TUN} includes tunneling and TAT contributions
- J_{TRAP} is calculated using Shockley-Read-Hall theory
- J_{EM} includes thermal and trap-to-band tunneling emission

Physical Mechanisms: Erase



- J_{TUN} is the hole current injected from the substrate
- J_{GATE} is the electron current injected from the gate

Solution Algorithm

- **Iterative methods commonly used to solve the equation system**
- **We developed a novel algorithm allowing deriving a closed form solution of the above system**

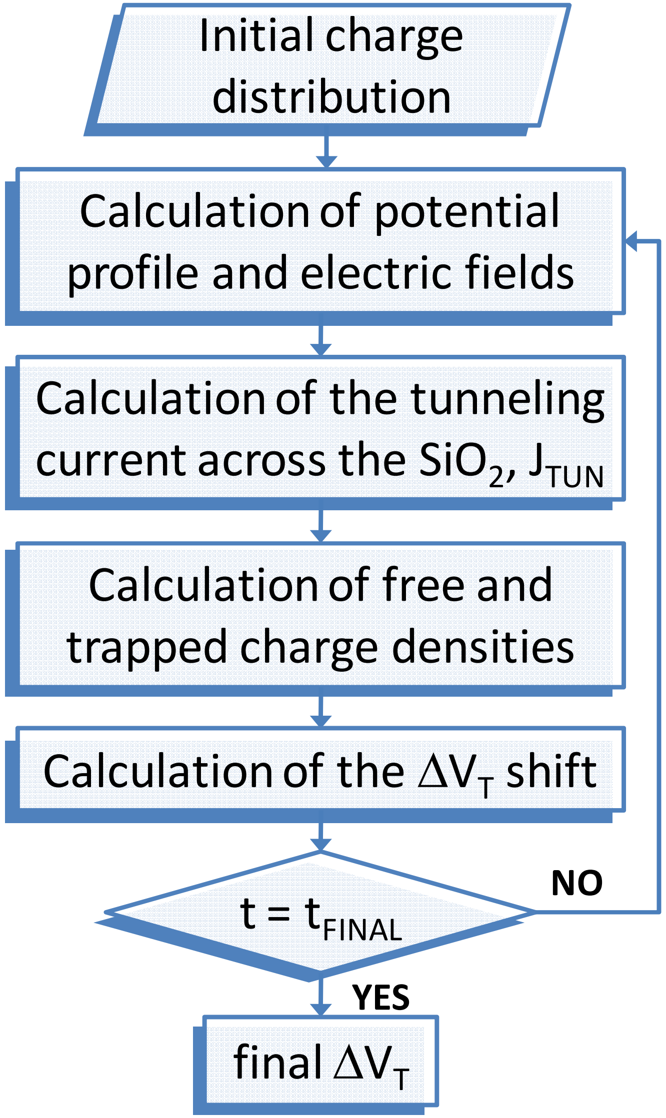
$$n_{F\,i,j} = \left(\beta_{i,j} J_{CB\,i,j} - \gamma_{i,j}\right) / \alpha_{i,j}$$

$$\alpha_{i,j} = \begin{cases} \alpha_{i+1,j} A_{i,j} + \beta_{i+1,j} C_{i,j} & i < N \\ qL\,\mu F_{i,j-1} P_{OUT} + C_{i,j} & i = N \end{cases}$$

$$\beta_{i,j} = \begin{cases} \beta_{i+1,j} + \alpha_{i+1,j} B & i < N \\ 1 & i = N \end{cases}$$

$$\gamma_{i,j} = \begin{cases} \gamma_{i+1,j} + \beta_{i+1,j} Y_{i,j} + \beta_{i+1,j} J_{TUN} & i = 1 \\ \gamma_{i+1,j} + \beta_{i+1,j} Y_{i,j} & 1 < i < N \\ Y_{i,j} & i = N \end{cases}$$

$$J_{CB\,i+1,j} = J_{CB\,i,j} - n_{F\,i,j} C_{i,j} + Y_{i,j}$$



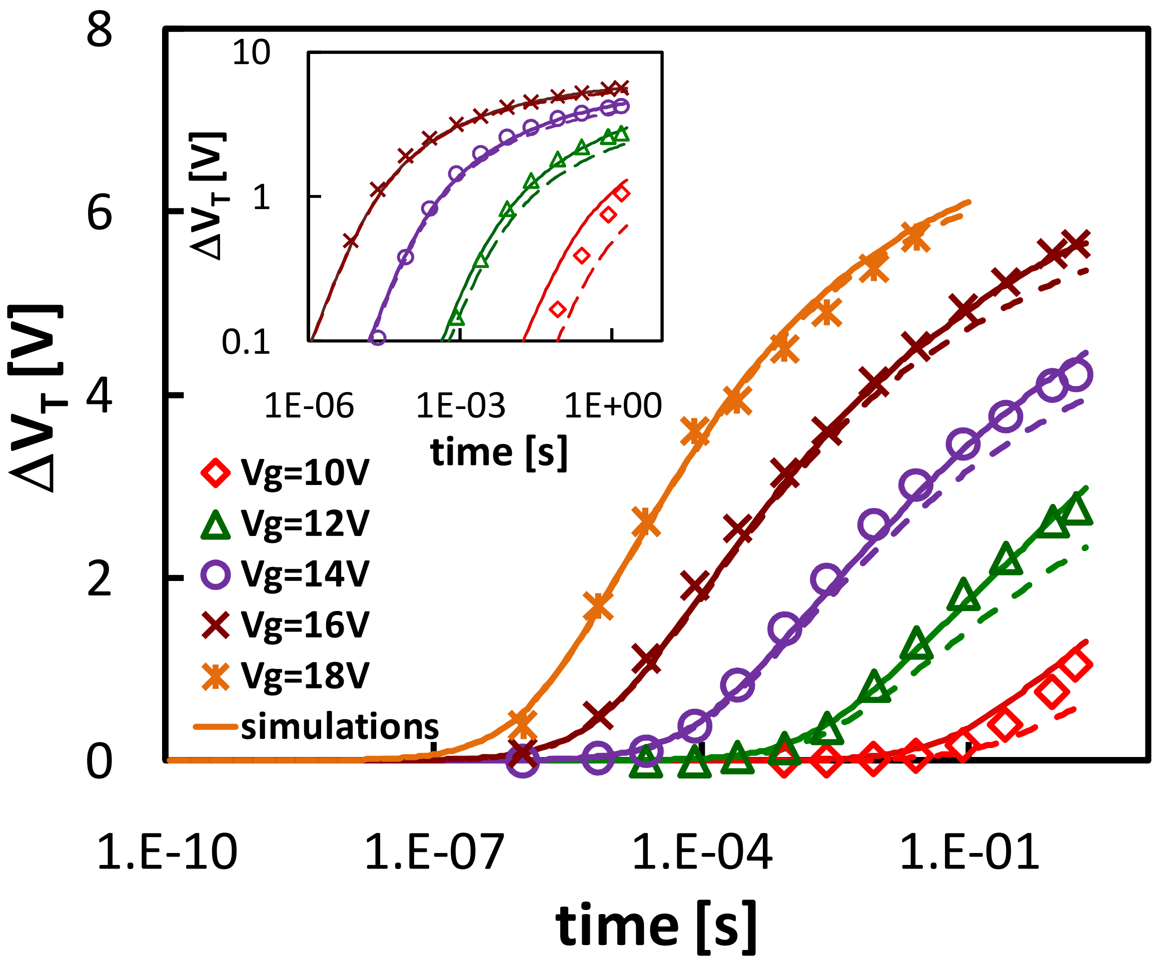
Samples

- **Model used to reproduce program, erase and retention of TANOS devices manufactured by different technologies (A, B, C)**

	Sample	t_{OX} [nm]	t_{NI} [nm]	t_{AL} [nm]	
TANOS	A1	3	5	11.5	
	A2	4	5	11.5	
	A3	4	8.7	11.5	**highest t_N/t_{AL} ratio**
	A4	4.5	7	12	
	B1	4	6	12	
	B2	5	6	12	
	C1	4.5	6	15	
	C2	4.5	4	15	**lowest t_N/t_{AL} ratio**
	C3	4.5	6	10	
TAOS	C4	1	-	5	
	C5	1	-	10	
	C6	1	-	15	

Program

- **TAT through SiO_2 is fundamental to achieve high accuracy at low V_G and high times (low fields)**

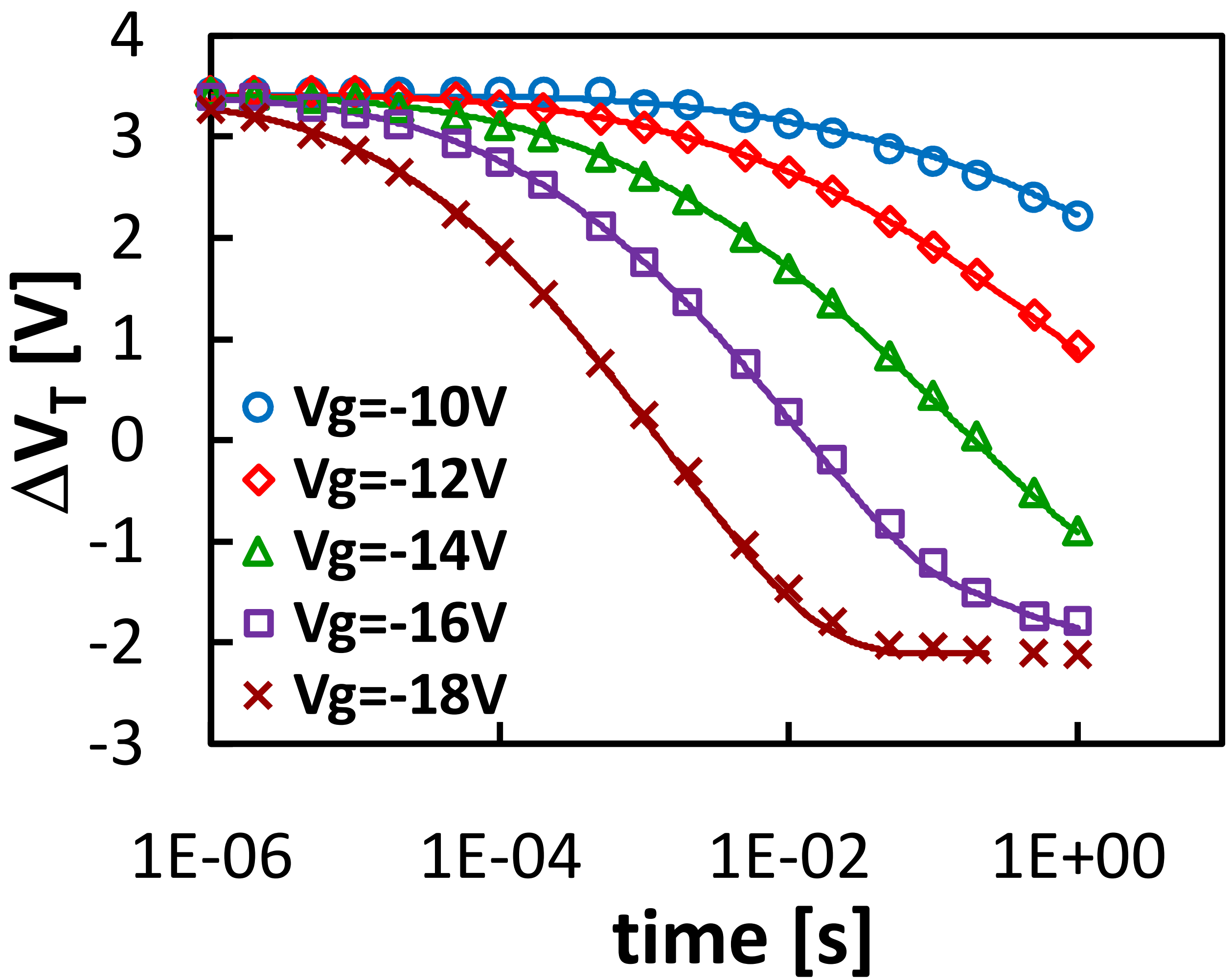


sample C1
$t_{OX}/t_N/t_{AL}$ = 4.5/6/15

A. Padovani *et al.*, IEEE EDL **30**, p.882, Aug. 2009

Erase

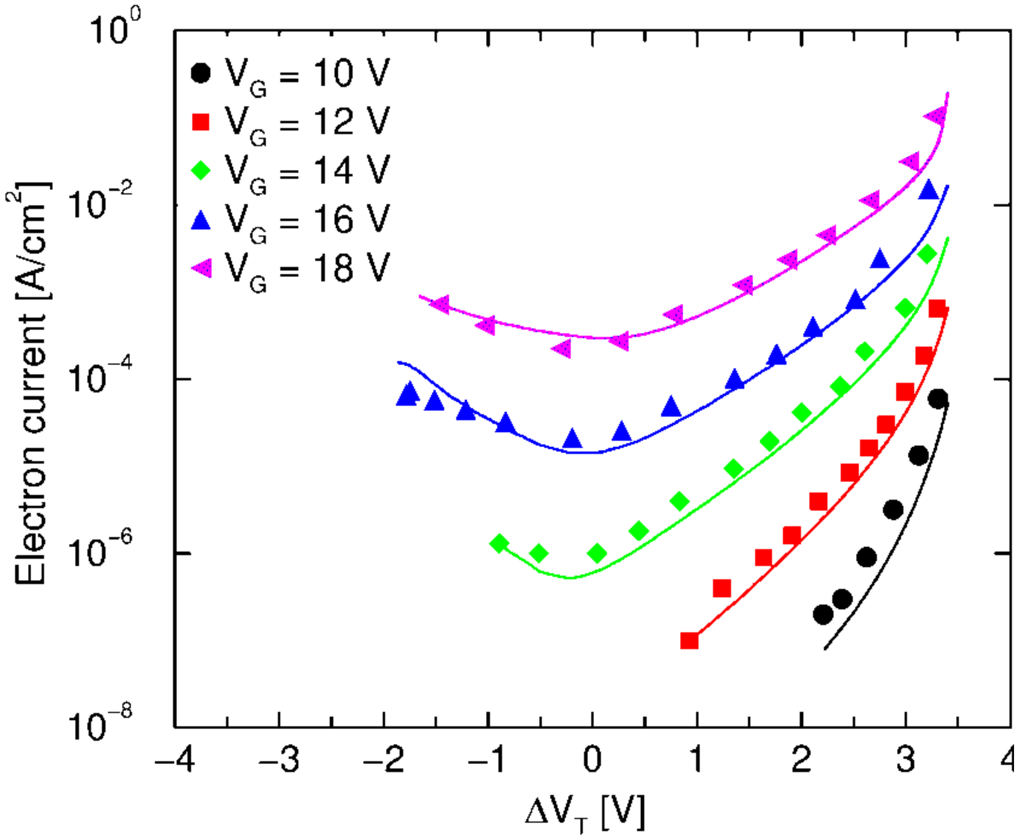
- **Simulations accurately reproduce erase transients**
- **Holes significantly contribute to TANOS erase at high $|V_G|$**

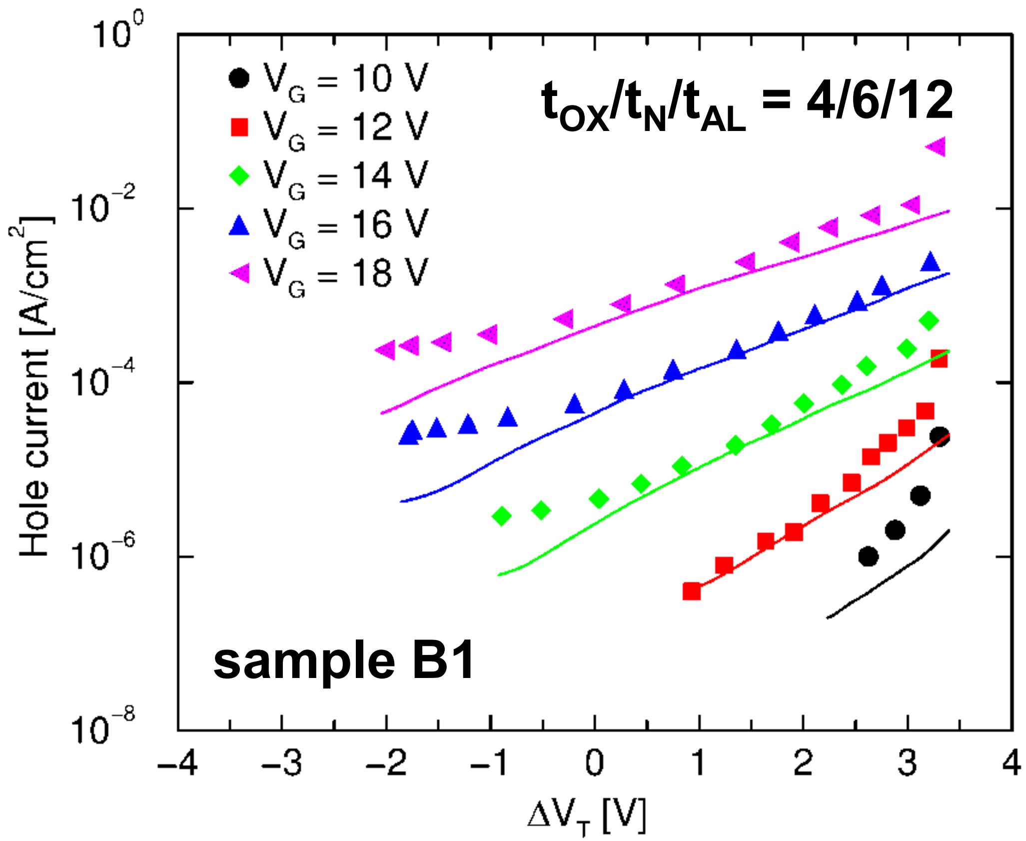


sample B1
$t_{OX}/t_N/t_{AL}$ = 4/6/12

Charge Separation

- **Simulations accurately reproduce both electron and hole currents measured during charge separation experiments**

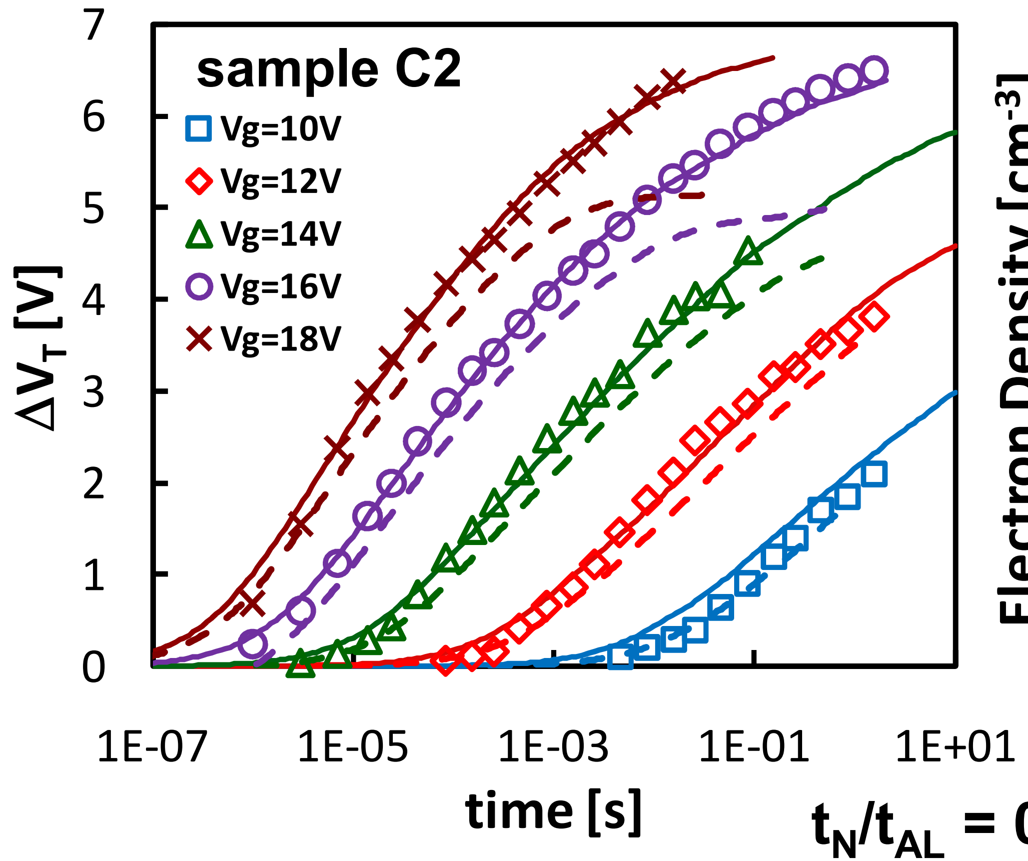




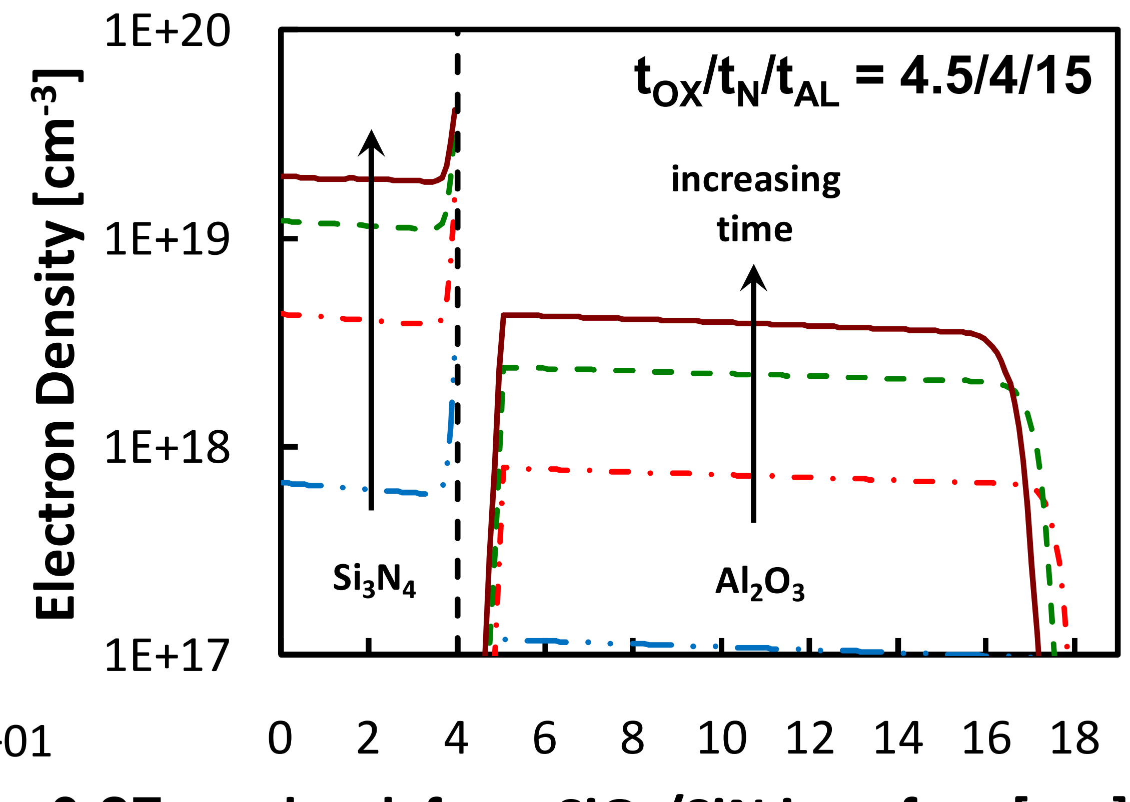
L. Vandelli *et al*., to be presented at IRPS 2010, 2-5 May, Anaheim (CA).

Trapping into Alumina

- Early saturation observed in simulations when trapping in alumina is neglected on the sample having a low t_N/t_{AL} ratio
- Large amount of electron charge trapped into Al_2O_3 defects



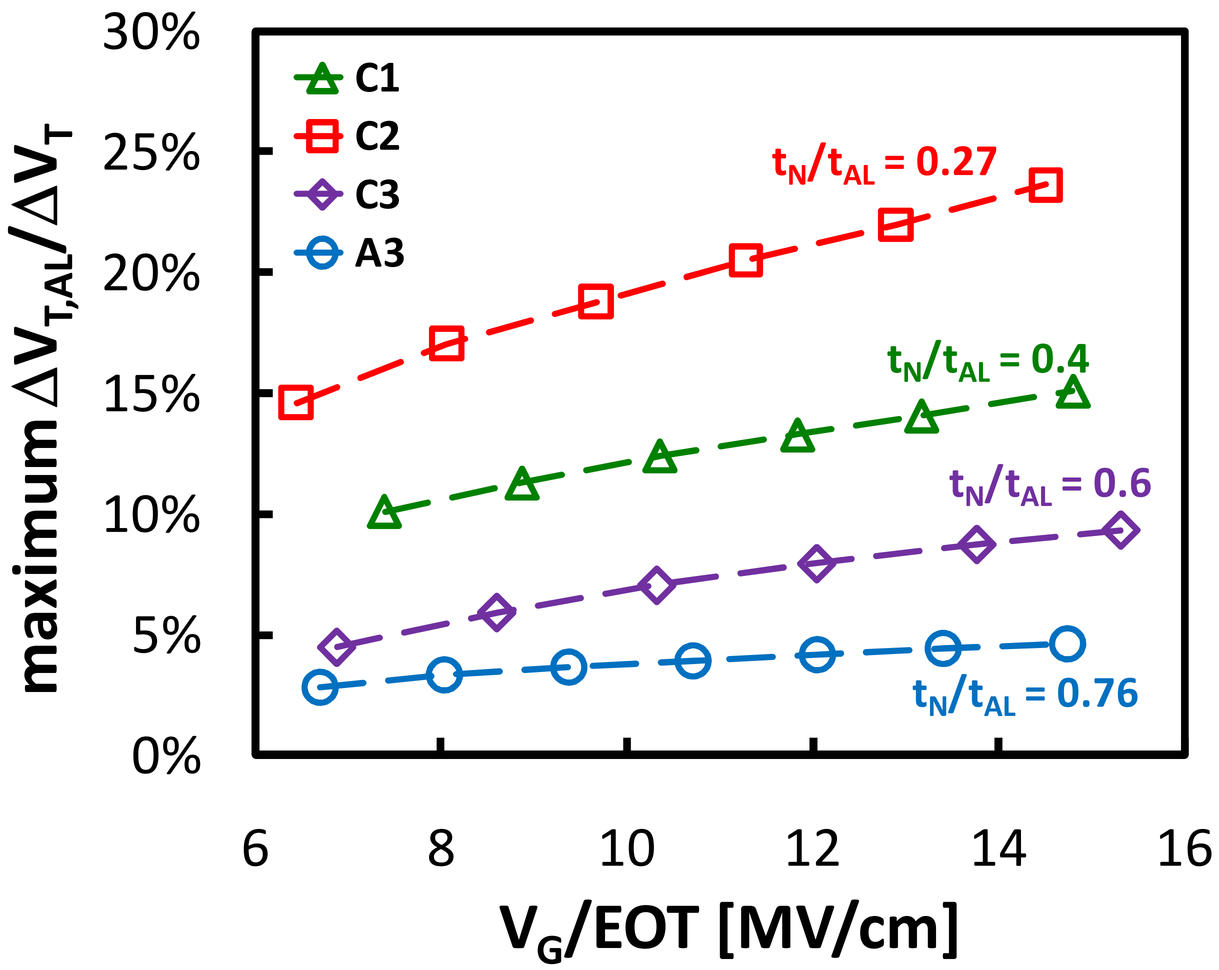
t_N/t_{AL} = 0.27



A. Padovani *et al.*, to be presented at VLSI-TSA 2010, 26-28 April, Taiwan

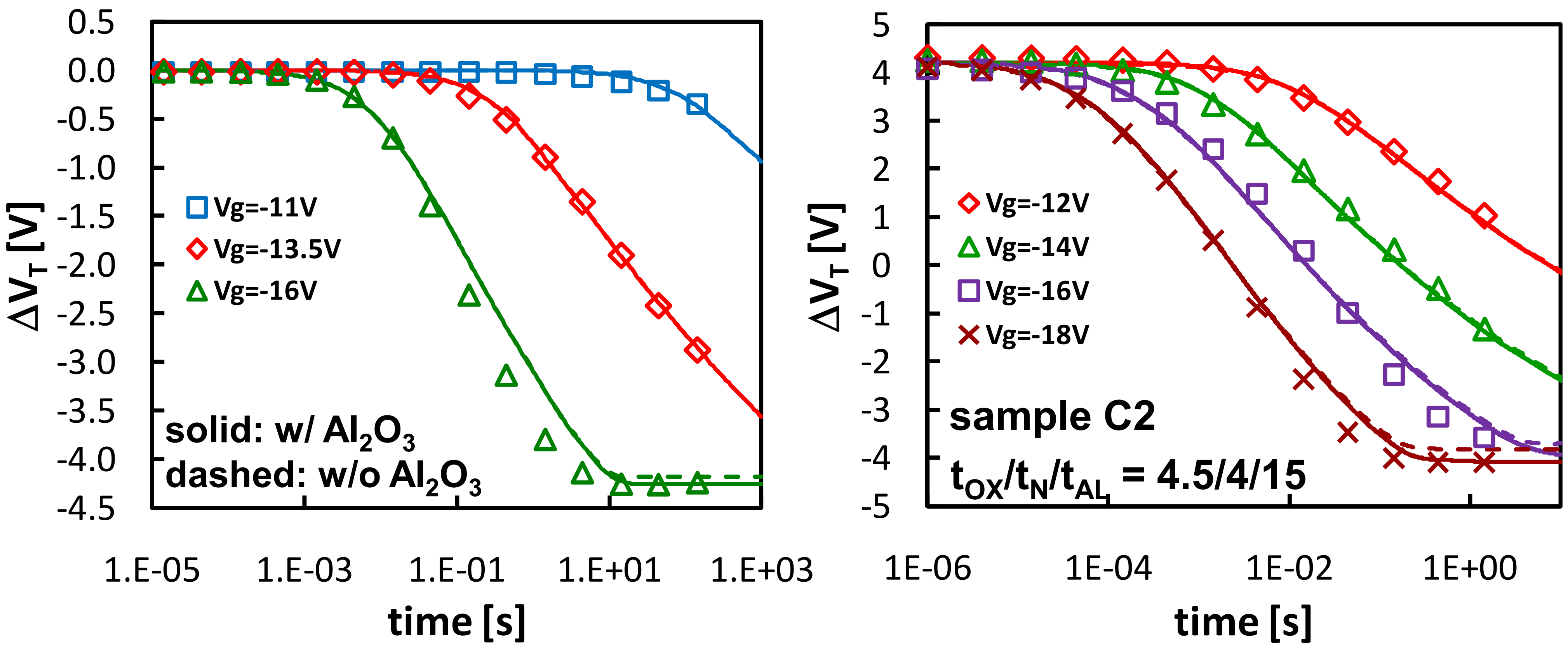
Trapping into Alumina -2

- Electron charge trapped in the alumina layer during program can account for up to 25% of the total ΔV_T shift
- Electron trapping in Al_2O_3 is negligible for a high t_N/t_{AL} ratio



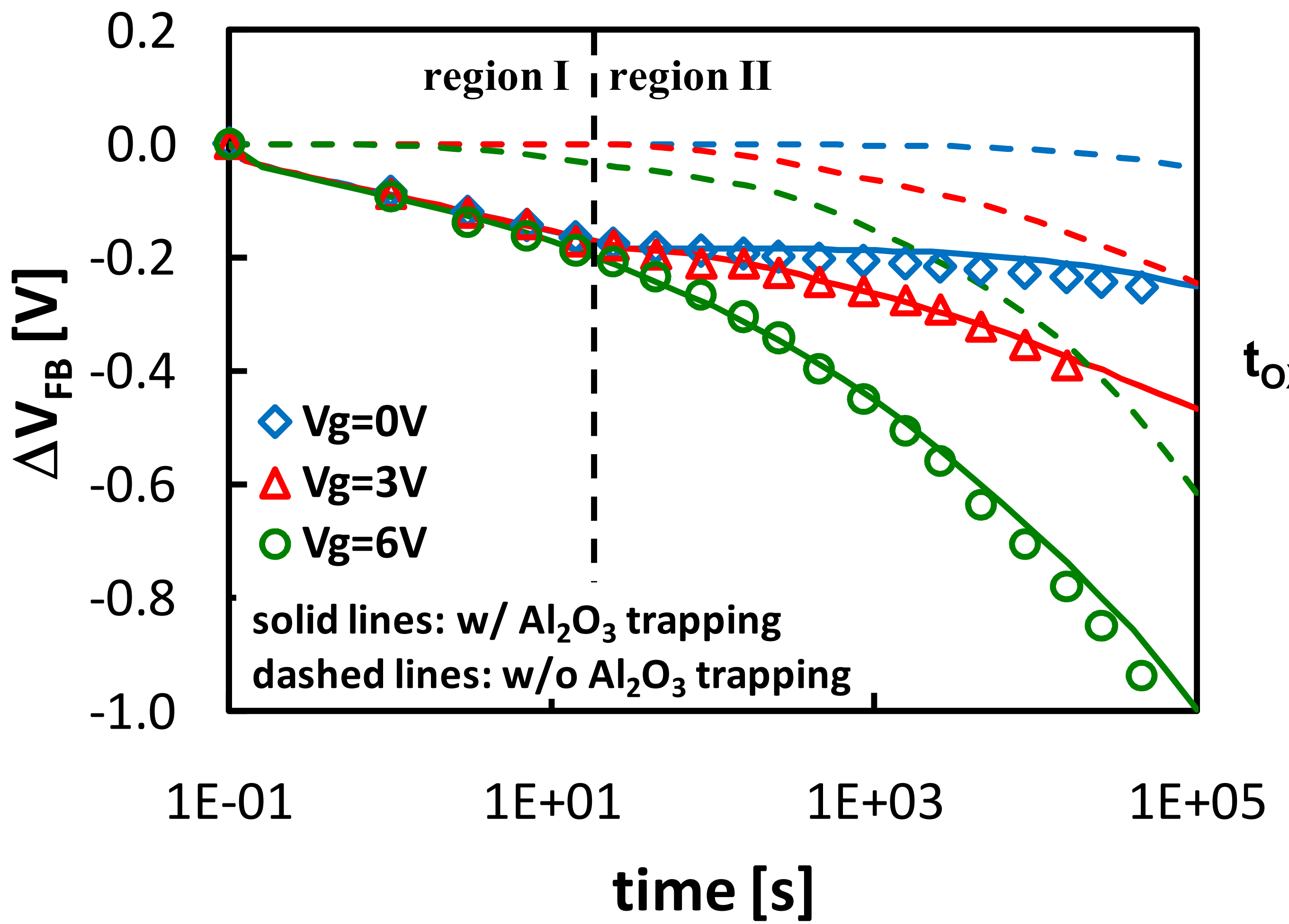
Trapping into Alumina -3

- **Hole trapping in alumina during erase is negligible**
- **30% of the electron trapped into Al_2O_3 during program are still there at the end of the subsequent erase operation**



Trapping into Alumina -4

- **Accelerated retention tests exhibit a double slope: clear signature of charge trapping in alumina**

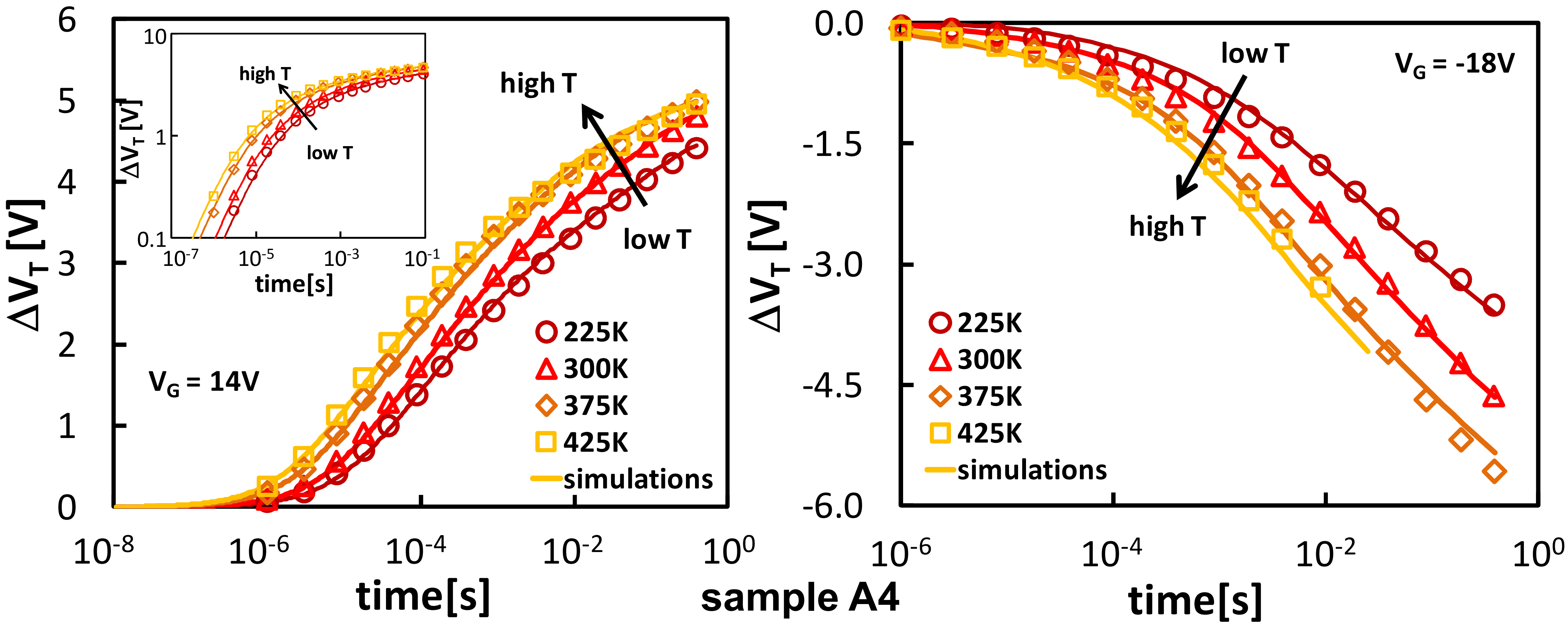


sample C1

$t_{OX}/t_N/t_{AL}$ = 4.5/6/15

Temperature Effects

- **Program and erase operations exhibit a strong temperature dependence, which is not explained by the temperature dependence of charge trapping and emission mechanisms**



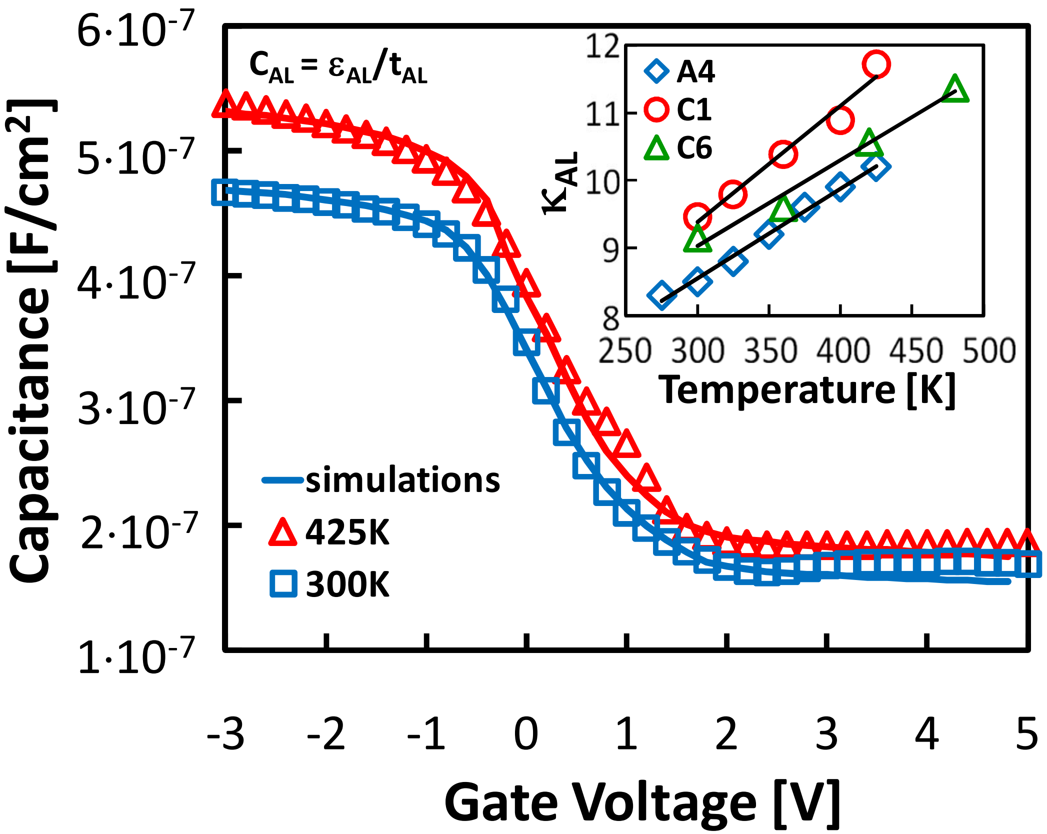
sample A4

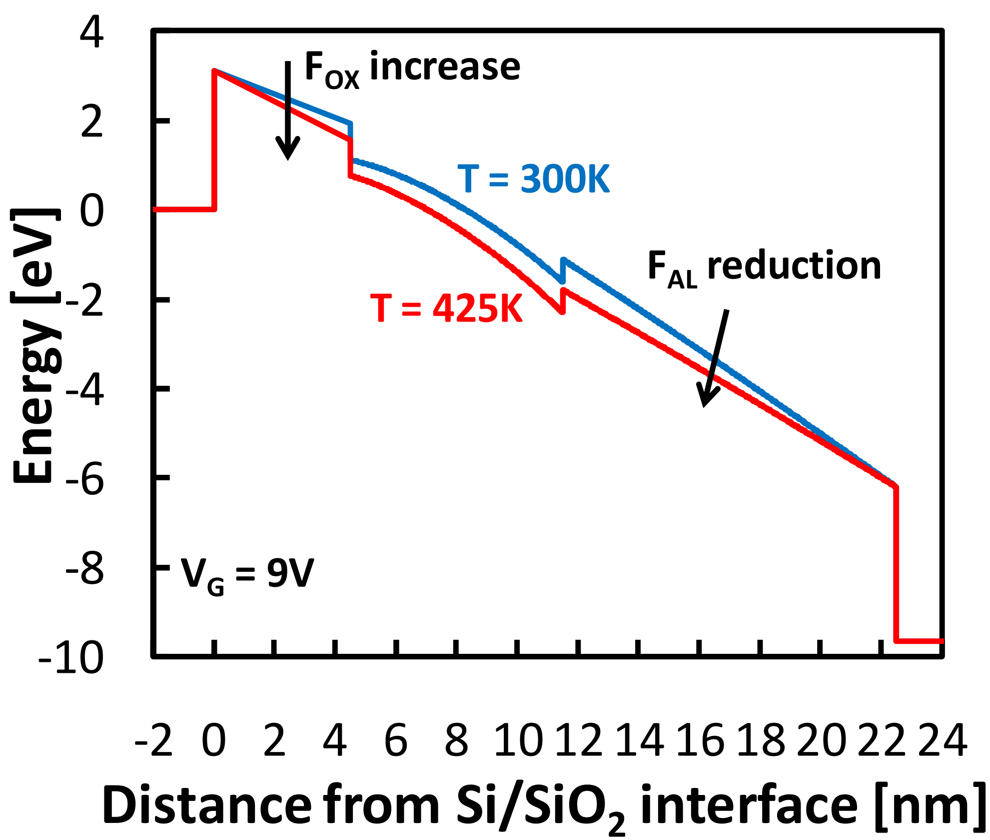
$t_{OX}/t_N/t_{AL}$ = 4.5/7/12

A. Padovani *et al.*, to be published on APL

Temperature Effects -2

- **Explanation: κ_{AL} increases with temperature (~25% over 125K)**
- **Voltage redistribution across the stack ($V_G \approx V_{OX}+V_N+V_{AL}$) leading to an increase of F_{OX}**



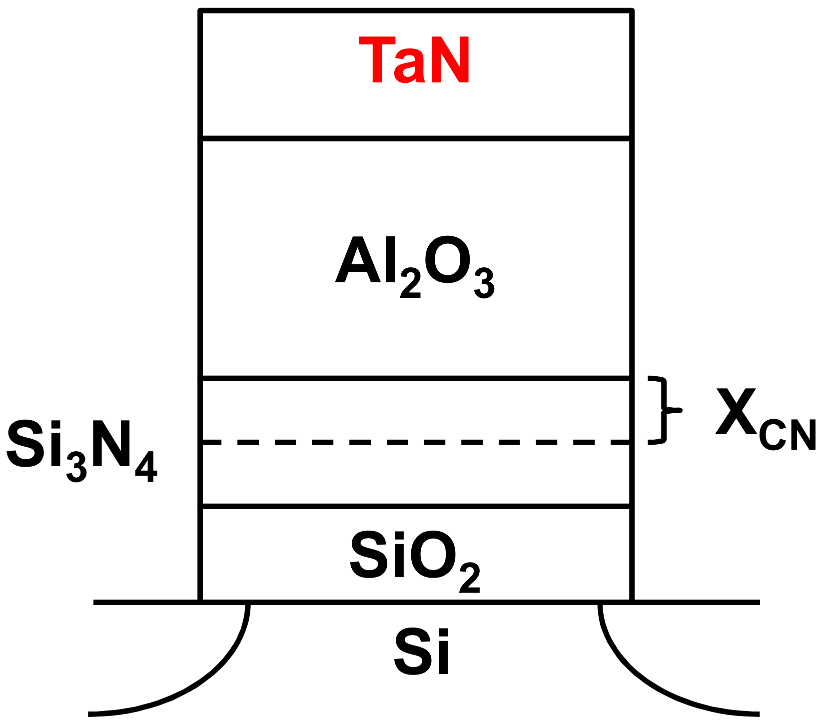


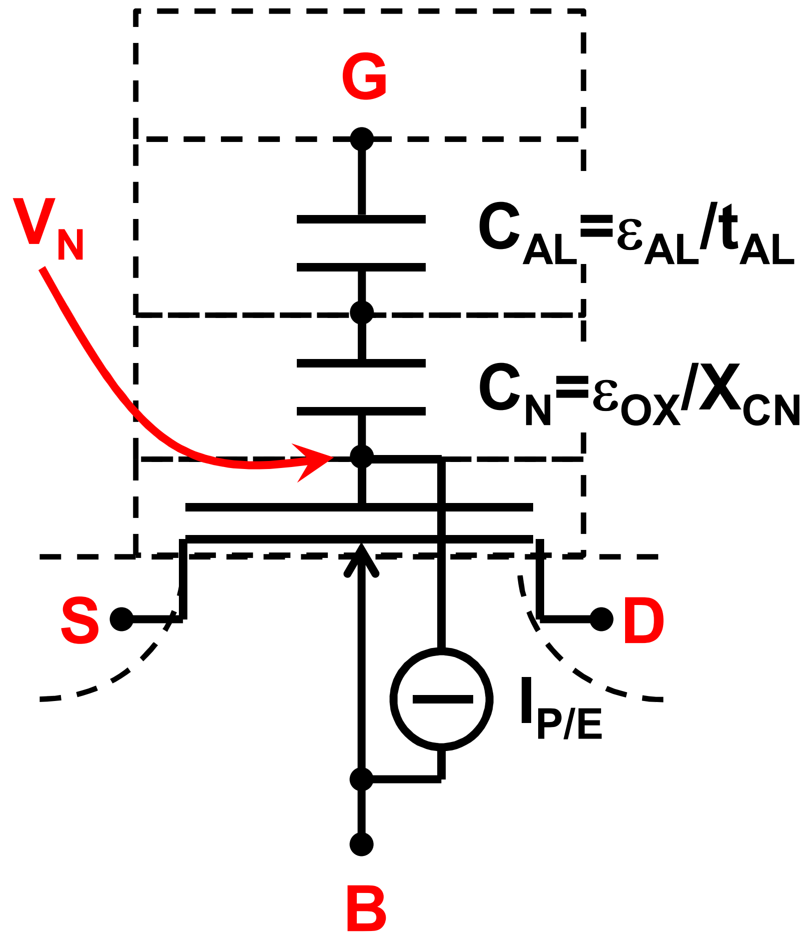
A. Padovani *et al.*, to be published on APL

A. Arreghini *et al.*, ULIS Tech. Dig., p.101, 2010.

Toward a Compact TANOS model

- Charge centroid findings can be used to develop simple TANOS SPICE-like models





Conclusions

- We developed a physical model to simulate P/E operations and reliability of TANOS devices
- The model exploits a new algorithm for the closed form solution of the equation system describing charge trapping and transport across the TANOS stack
- The model has been used to investigate the effects of temperature and charge trapping into alumina on TANOS operations and reliability
- This allows extracting important guidelines for stack optimizations
- The model allows deriving the basic approximations to develop SPICE-like compact models