A physics-based model for Charge-Trapping memory simulation

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Purpose

• Charge-trapping devices like TANOS are a promising candidates to replace Floating Gate memories
• Understanding the physical mechanisms governing device operation is fundamental for performance and reliability optimization
• This requires accurate simulation models
• We present results obtained with a physical model accounting for both charge trapping in alumina and temperature effects
Outline

• Introduction
• Physical Model
• Model Results
  – Program and Erase operations
  – Charge Separation Experiments
  – Charge Trapping into Alumina
  – Effects of Temperature
• Toward a SPICE-like model of the TANOS cell
• Conclusions
**Introduction**

- Better retention (*thicker* tunnel SiO$_2$)
- Improved program/erase speed (*high-k*)
- Improved erase $V_T$ saturation level (*metal gate*)

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Physical Model

• Charge trapping and transport across the stack is described by a set of differential equations solved by discretizing space and time (indexes $i$ and $j$)

$$J_{CB_{1,j}} = J_{TUN} \rightarrow J_{CB_{i,j}} \rightarrow J_{CB_{i+1,j}} \rightarrow J_{CB_{N+1,j}} = J_{OUT}$$

$$J_{EM\_TE_{ij}} \quad J_{TRAP_{ij}}$$

SiO$_2$ \hspace{1cm} Al$_2$O$_3$

reg. 1 \hspace{1cm} ... \hspace{1cm} reg. $i$ \hspace{1cm} ... \hspace{1cm} reg. N

$$J_{CB_{i,j}} = q \mu \left[ n_{F_{i,j},F_{i,j-1}} + \frac{k_B T}{q} \frac{n_{F_{i,j}} - n_{F_{i+1,j}}}{L} \right]$$

$$\frac{qL(n_{F_{i,j}} - n_{F_{i,j-1}})}{t_j - t_{j-1}} = J_{CB_{i,j}} - J_{CB_{i+1,j}} + J_{EM\_i,j} - J_{TRAP\_i,j}$$

$$\frac{qL(n_{T_{i,j}} - n_{T_{i,j-1}})}{t_j - t_{j-1}} = J_{TRAP\_i,j} - J_{EM\_i,j}$$
Physical Mechanisms: Program

- $J_{TUN}$ includes tunneling and TAT contributions
- $J_{TRAP}$ is calculated using Shockley-Read-Hall theory
- $J_{EM}$ includes thermal and trap-to-band tunneling emission

$J_{TRAP} = q \cdot n_F \cdot L \cdot R_C$

$J_{EM} = q \cdot n_T \cdot L \cdot R_E$
Physical Mechanisms: Erase

- $J_{\text{TUN}}$ is the hole current injected from the substrate
- $J_{\text{GATE}}$ is the electron current injected from the gate
Solution Algorithm

- Iterative methods commonly used to solve the equation system
- We developed a novel algorithm allowing deriving a closed form solution of the above system

\[
n_{F,i,j} = \left( \beta_{i,j} J_{CB,i,j} - \gamma_{i,j} \right) / \alpha_{i,j}
\]

\[
\alpha_{i,j} = \begin{cases} 
\alpha_{i+1,j} A_{i,j} + \beta_{i+1,j} C_{i,j} & i < N \\
qL \mu F_{i,j-1} P_{OUT} + C_{i,j} & i = N 
\end{cases}
\]

\[
\beta_{i,j} = \begin{cases} 
\beta_{i+1,j} + \alpha_{i+1,j} B & i < N \\
1 & i = N 
\end{cases}
\]

\[
\gamma_{i,j} = \begin{cases} 
\gamma_{i+1,j} + \beta_{i+1,j} Y_{i,j} + \beta_{i+1,j} J_{TUN} & i = 1 \\
\gamma_{i+1,j} + \beta_{i+1,j} Y_{i,j} & 1 < i < N \\
Y_{i,j} & i = N 
\end{cases}
\]

\[
J_{CB,i+1,j} = J_{CB,i,j} - n_{F,i,j} C_{i,j} + Y_{i,j}
\]
Samples

- Model used to reproduce program, erase and retention of TANOS devices manufactured by different technologies (A, B, C)

<table>
<thead>
<tr>
<th>Sample</th>
<th>(t_{\text{OX}}) [nm]</th>
<th>(t_{\text{NI}}) [nm]</th>
<th>(t_{\text{AL}}) [nm]</th>
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</thead>
<tbody>
<tr>
<td>A1</td>
<td>3</td>
<td>5</td>
<td>11.5</td>
</tr>
<tr>
<td>A2</td>
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</tr>
<tr>
<td>A3</td>
<td>4</td>
<td>8.7</td>
<td>11.5</td>
</tr>
<tr>
<td>A4</td>
<td>4.5</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>B1</td>
<td>4</td>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>B2</td>
<td>5</td>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>C1</td>
<td>4.5</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
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<tr>
<td>C4</td>
<td>1</td>
<td>-</td>
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<td>-</td>
<td>10</td>
</tr>
<tr>
<td>C6</td>
<td>1</td>
<td>-</td>
<td>15</td>
</tr>
</tbody>
</table>

- TANOS
  - Highest \(t_{\text{NI}}/t_{\text{AL}}\) ratio

- TAOS
  - Lowest \(t_{\text{NI}}/t_{\text{AL}}\) ratio
Program

- TAT through SiO$_2$ is fundamental to achieve high accuracy at low $V_G$ and high times (low fields)

\[ \begin{array}{c|cccc}
\text{time [s]} & 1E-06 & 1E-03 & 1E+00 \\
\hline
\text{$\Delta V_T$ [V]} & 0.1 & 1 & 10 \\
\end{array} \]

\[ \begin{array}{cccc}
V_g=10V & V_g=12V & V_g=14V & \text{simulations} \\
\text{sample C1} & t_{OX}/t_N/t_{AL} = 4.5/6/15 \\
\end{array} \]

• Simulations accurately reproduce erase transients
• Holes significantly contribute to TANOS erase at high $|V_G|$
Charge Separation

• Simulations accurately reproduce both electron and hole currents measured during charge separation experiments

L. Vandelli et al., to be presented at IRPS 2010, 2-5 May, Anaheim (CA).
Trapping into Alumina

- Early saturation observed in simulations when trapping in alumina is neglected on the sample having a low $t_N/t_{AL}$ ratio
- Large amount of electron charge trapped into $\text{Al}_2\text{O}_3$ defects

A. Padovani et al., to be presented at VLSI-TSA 2010, 26-28 April, Taiwan
• Electron charge trapped in the alumina layer during program can account for up to 25% of the total $\Delta V_T$ shift
• Electron trapping in Al$_2$O$_3$ is negligible for a high $t_N/t_{AL}$ ratio
Trapping into Alumina -3

- Hole trapping in alumina during erase is negligible
- 30% of the electron trapped into Al₂O₃ during program are still there at the end of the subsequent erase operation
Accelerated retention tests exhibit a double slope: clear signature of charge trapping in alumina.

Sample C1

$t_{\text{OX}}/t_{\text{N}}/t_{\text{AL}} = 4.5/6/15$

Region I
Region II

$\Delta V_{FB}$ [V]

Time [s]
Temperature Effects

- Program and erase operations exhibit a strong temperature dependence, which is not explained by the temperature dependence of charge trapping and emission mechanisms.

A. Padovani et al., to be published on APL
Temperature Effects -2

- Explanation: $\kappa_{AL}$ increases with temperature (~25% over 125K)
- Voltage redistribution across the stack ($V_G \approx V_{OX} + V_N + V_{AL}$) leading to an increase of $F_{OX}$

A. Padovani et al., to be published on APL
Toward a Compact TANOS model

- Charge centroid findings can be used to develop simple TANOS SPICE-like models

\[
\begin{align*}
C_{\text{TaN}} &= \varepsilon_{\text{TaN}} / t_{\text{TaN}} \\
C_{\text{Si}3\text{N}_4} &= \varepsilon_{\text{Si}3\text{N}_4} / \chi_{\text{Si}3\text{N}_4}
\end{align*}
\]
Conclusions

• We developed a physical model to simulate P/E operations and reliability of TANOS devices

• The model exploits a new algorithm for the closed form solution of the equation system describing charge trapping and transport across the TANOS stack

• The model has been used to investigate the effects of temperature and charge trapping into alumina on TANOS operations and reliability

• This allows extracting important guidelines for stack optimizations

• The model allows deriving the basic approximations to develop SPICE-like compact models