Development of an Enhanced ADS® Electrothermal Simulation Tool for RF Circuits

Salvatore Russo, Vincenzo d’Alessandro, Niccolò Rinaldi

Department of Biomedical, Electronics and Telecommunications Engineering
University of Naples Federico II, via Claudio 21, 81025 Naples, Italy
Outline

- Introduction to electrothermal effects
  - Relevance of ET effects in RF device/circuits
  - ADS based simulation software
- Thermal modeling
  - Approaches to thermal modeling
  - Thermal models for ET simulation
- Electrothermal simulation
  - Software structure
  - Simulation examples
Thermal issues: reliability

- **$T_{\text{max}}$ boundary**: caused by failure mechanisms activated at high temperatures (increased leakage currents, oxide breakdown, electromigration, metal contact degradation, increased stresses due to differing coefficient of thermal expansion among materials…). Determines SOA limitation at high power levels, which shrinks in the downscaling process due to $R_{\text{TH}}$ increase in small area devices.

- **2nd breakdown boundary**: related to self-heating and/or impact ionization. Occurs at lower power levels and shrinks with device downscaling due to increased $R_{\text{TH}}$, reduced breakdown voltage, reduced ballasting effect of parasitic resistances.

- **1st breakdown boundary**: decreases with device downscaling due to vertical doping optimization.

![Thermal Issues Diagram]
Thermal issues in GaAs-based PA’s

- In GaAs-based HBT’s used in wireless applications thermal issues are even more critical due to the combination of the poor GaAs thermal conductivity (about one third of that of Si) and high current densities usually handled.
- Poor thermal design may cause long term reliability problems, hot spot formation, thermal runaway, current hogging effects eventually leading to performance degradation (current gain collapse [Liu, T-ED 1993, 1994, 1995, 1996]).
- Thermal memory effects also degrade linearity performance.

![Graph showing power density vs. power dissipation for different devices.](image_url)

T. Nozu, 21st IEEE SEMI-THERM Symposium, 2005
Thermal Issues: Device Isolation

- Isolation schemes have evolved over time (STI-DTI/SOI/Silicon-On-Glass) in the attempt to reduce parasitics, improve noise immunity, reduce leakage currents, etc.
- Electrical insulating materials also provide an (unwanted) thermal isolation.

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<tr>
<th>Material</th>
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<td>148</td>
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<td>Si (10 nm)</td>
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\[ R_{TH\text{-}trench\text{-}SOI} \approx 5900 \text{ K/W} \]

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SOG, Nanver T-ED 2003
Electrothermal Analysis

PROBLEM:
In solid state devices the current (and hence the dissipated power) is a function of device temperature, which, in turn, is determined by the dissipated power. Therefore the determination of device current and temperature represents a **coupled problem**.

- To solve the circuit equations the device temperature must be known \([i_i = f(T_i)]\).
- To calculate the temperature the power dissipated by the devices should be known \([T_i = f(P_i)]\).

SOLUTION:
Develop circuit simulation tools where the electrical and thermal problems are solved simultaneously.
Electrothermal simulation approaches

- **Direct Approach:**
  - Direct coupling between electrical and thermal solvers
  - Solution of the heat diffusion equation at each iteration point (huge computational effort)

- **Reduced Thermal Models Approach:**
  - Use reduced thermal models (e.g., $R_{TH}$ matrix or equivalent thermal networks). Parameters can be extracted in advance through measurements, numerical simulations, or analytical models.
Electrothermal Analysis:
Limitations of present circuit simulation tools/models

Commercial circuit simulators (PSPICE) without thermal models:
• The temperature is a constant parameter and does not change during the simulation process.

Most simulators (like ADS® and Spectre) include advanced electrothermal models for devices; if enabled, the electrothermal feedback can be accounted for through a simple single-pole equivalent network; however:
• Only self-heating effect is included, that is, thermal coupling between devices is not taken into account. However, this might lead to markedly inaccurate results when the temperature of a transistor is affected by other (close enough) devices
• Thermal parameters ($R_{TH}$, $C_{TH}$) have to be set manually in the thermal circuit
• Single-pole thermal circuits have insufficient accuracy when describing transient evolution.
Electrothermal Analysis: ADS®

Routine for generating a thermal model imports all required information from the layout.

Thermal model parameters

The thermal compact model is automatically linked to the circuit.
Self-heating & coupling effects.
DC, AC, transient analysis.
Transient analysis can be done with selected accuracy.

ADS® (circuit simulation)

ADS® device models in which the temperature changes during the simulation process.
Thermal modeling
Thermal Resistance Matrix

- The temperature of each device is due to the power dissipated by the device itself (self-heating) and to the power due to the neighboring devices (thermal coupling).
- This leads to the thermal resistance matrix

\[
\begin{align*}
T_1 - T_{hs} &= R_{11} \cdot P_1 + R_{12} \cdot P_2 + R_{13} \cdot P_3 \\
T_2 - T_{hs} &= R_{21} \cdot P_1 + R_{22} \cdot P_2 + R_{23} \cdot P_3 \\
T_3 - T_{hs} &= R_{31} \cdot P_1 + R_{32} \cdot P_2 + R_{33} \cdot P_3
\end{align*}
\]
The $R_{TH}/Z_{TH}$ matrix can be obtained from:

a) Measurements  
b) FEM thermal simulations  
c) Analytical thermal models (easier to implement automatically, however the circuit layout must be known)
Structure of the Electrothermal tool (2)

After $R_{TH}/Z_{TH}$ matrix calculation (or measurement), we need to generate the thermal networks which calculates the temperature in each device and link it to the original schematic -> “Electrothermal schematic” with electrothermal effects automatically embedded.

- **Experimental**
  - $R_{TH}/Z_{TH}$ matrix for different technologies are automatically evaluated from layout

- **R_th Calculation routine**
  - (analytical models)

- **FEM**
  - $R_{TH}/Z_{TH}$ matrix can be also provided externally when evaluated from measurements or FEM

- **E-T schematic**
  - ADS® (circuit simulation including ET feedback block)
Structure of the Electrothermal tool (3)

In order to connect the devices of the schematic to the proper nodes of the thermal network, the device model is modified by deactivating the default thermal network, and adding a node where the dissipated power is accessible.

(a 5-finger example)
Structure of the Electrothermal tool (4)

ET feedback block can be implemented by:
- Equivalent network
- Verilog-A: text file describing the ET-FB accepted & compiled by simulators supporting Verilog-A.
- SDD (Symbolically Defined Device): multiport components where current on one port is defined as e.g., voltage on another port; possible direct derivative calculation.
The electrothermal simulation tool also includes a post-processing routine. After the ET simulation is completed the routine imports the I-V ADS data, and plots the temperature map on the chip surface for a chosen bias condition (i.e., a simulation point).
ET software user interface (UI): an example (1)

- User is guided with a simplified user interface step-by-step.
- Interface has been written in Matlab but it is portable to any other programming language.
- User can choose to use a configuration file defined before or to proceed with “wizard”.
- This example simulates a step-by-step pre-processing task for a 3-finger case starting from layout.
ET software user interface (UI): an example (2)

- Thermal matrix is evaluated and a new schematic containing ET feedback block is generated.
- After ADS simulation, data can be provided to post-processor to evaluate temperature maps.

(3-finger example)
Temperature distributions: an example (1)
Temperature distributions: an example (2)
Electrothermal simulation: an example (1)

Array of 3 horse-shoe shaped GaAs HBTs (fabricated by Skyworks Inc.) with a center-to-center spacing of 24 µm and typical $f_T=47$ GHz.

- FEM simulations are used to evaluate thermal matrices for different devices configurations.
- Matrices are then provided to simulation tool in order to perform ET simulations.
Electrothermal simulation: an example (2)

An array of 3 devices with a center-to-center spacing of 24 µm.

An array of 3 devices with a center-to-center spacing of 72 µm.
Extension to dynamical thermal models

- The code will be also extended to include dynamic thermal models for large-signal/small-signal analysis.
- Similar to the thermal resistance, the thermal impedance matrix can be obtained by measurements, FEM thermal simulations or analytical models.
- Once the $Z_{TH}$ vs. time or frequency data have been obtained, an appropriate model must be created that can be included in the ADS environment.
- The single-pole network is then replaced by an optimized multi-pole circuit to better mimic the thermal evolution in time.
- An in-house code has been developed to convert Foster network to Cauer network.

\[
Z_{TH}(t) = \sum_i \left( 1 - e^{-\frac{t}{R_{TH_i}C_{TH_i}}} \right)
\]
The identification software has been tested on several silicon-on-glass (SOG) devices measured with good results. These devices are fabricated by DIMES (Delft, The Netherlands)
Electrothermal simulation: a transient example (1)

SOG electrothermal simulations performed with constant base-emitter voltage by varying collector-emitter voltage.

Transient evolution of collector current applying a step of $V_{CE}$ while keeping constant $V_{BE}$. 
Conclusions

• A novel electrothermal simulation tool relying on the fully automated employment of the commercial simulator ADS® has been developed.
• The thermal network can be either automatically calculated from the circuit layout or included by the user (e.g., when the thermal resistances are evaluated numerically/experimentally).
• New in-house electrothermal models for active/passive components have been developed and made available in the program libraries.
• Transient analyses are enabled through the adoption of equivalent RC Foster networks, which can be automatically optimized via an in-house routine.
• Another in-house routine has been developed to convert RC Foster networks to RC Cauer networks seamlessly.
• The proposed code has been successfully applied to various bipolar technologies (e.g., GaAs-based HBTs, multifinger SiGe HBTs, silicon-on-glass BJTs).