Sizing CMOS circuits by means of the $g_m/I_D$ methodology and a compact model.

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sizing....

find **D.C. currents and transistor sizes**

**meeting**:

- a prescribed gain-bandwidth product
- minimal power consumption
- minimal area
- large gain
- ....

low- voltage, low-power MOS circuits
Outline

Sizing...

• the Intrinsic Gain Stage (I.G.S.)
  \[ g_m/I_D \] semi-empirical methodology
  \[ g_m/I_D \] compact model methodology
  L-V, L-P, short channel I.G.S.

• the Miller Op. Amp.

Conclusion
**The Intrinsic Gain Stage (I.G.S.)**

Gain-bandwidth sizing:

find $I_D$ and $W/L$ achieving $\omega_T$

\[ g_m = \omega_T \cdot C \]

Gain-bandwidth sizing:

\[ g_m / I_D \cdot V_A \]

- 20 dB/decade

\[ \omega_T = \frac{g_m}{C} \]
1) (strong inversion)

\[ g_m = \omega_T C \]

\[ A = \frac{g_m}{I_D} V_A = \sqrt{\frac{2\beta}{nI_D}} V_A \]

\[ \beta = \mu C'_{ox} \frac{W}{L} \]

\[ g_m = \frac{\partial I_D}{\partial V_G} = \sqrt{\frac{2\beta I_D}{n}} \]

\[ \frac{W}{L} = \frac{n (\omega_T C)^2}{2\mu C'_{ox}} \cdot \frac{1}{I_D} \]

power decreases, gain increases
2) *weak inversion*)

\[ I_D = I_o \exp \left( \frac{V_G}{nU_T} \right) \]

\[ g_m = \frac{I_D}{nU_T} \]

\[ A_{\text{max}} = -\frac{V_A}{nU_T} \]

\[ I_D = nU_T \omega_T C \]

sizing in moderate inversion?
Outline

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• the Miller Op. Amp.

Conclusion
what does \( \frac{g_m}{I_D} \) represent?

\[
\left( \frac{g_m}{I_D} \right) = \frac{1}{I_D} \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} \log(I_D)
\]
why $g_m/I_D$?

- $g_m/I_D$ does not depend on the transistor width
  
  $g_m$ and $I_D$ are proportional to $W$

- $g_m/I_D$ bridges a small signal and a large signal quantity

  $$g_m \Leftrightarrow I_D$$

- $g_m/I_D$ controls gain, power consumption ...

  $$A = \frac{g_m}{I_D} V_A$$
The $g_m/I_D$ sizing methodology
(semi-empirical)

$$g_m = \omega_T C$$

$$I_D(V_{GS}) = \frac{g_m}{I_D}$$

$$W(V_{GS}) = \frac{I_D(V_{GS})}{I_D_{ref}(V_{GS})} (W)_{ref}$$

- measurements
- reconstructed data (BSIM, PSP...)
- model E.K.V...

monitors the mode of operation of the MOS transistor
Example

\[ W/L \]

parasitic drain junction

mobility degradation

\[ f_T = 1 \text{ GHz}; \quad C_o = 1 \text{ pf}; \quad L = 120 \text{ nm}; \quad V_S = 0; \quad V_{DS} = 0.6 \text{ V}; \quad W_{max} = 1 \mu\text{m}; \]
First paper

A $g_m/I_D$ Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA

F. Silveira, D. Flandre, P.G.A. Jespers

IEEE JOURNAL OF SOLID STATE CIRCUITS, VOL. 31, NO. 9, SEPTEMBER 1996
p. 1314 ...
Outline

Sizing...
• the Intrinsic Gain Stage (I.G.S.)
  \( g_m/I_D \) semi-empirical methodology
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Conclusion
The ACM and EKV compact models

- continuous model (saturation, weak to strong inversion)
- few parameters:
  - $n$ subthreshold slope factor
  - $I_{Su}$ unary specific current
  - $V_{To}$ threshold voltage
- uniformly doped substrate, no mobility degradation,
- gradual channel approximation (1D)

A.C.M.

- An MOS transistor model for analog circuit design
  Ana I. Cunha, M.C. Schneider, C. G. Montoro.

E.K.V.

- An analytical MOS transistor model valid in all regions of operation and dedicated to Low-Voltage and Low-current applications.
  Chr. C. Enz, F. Krummenacher, E. A. Vittoz.
The compact model (1)

\[ i = \frac{I_D}{I_S} \]

normalized drain current

\[ I_{Su} \]

specific current

\[ \frac{2nU_T^2\mu C_{ox}'}{W} \frac{W}{L} \]

\[ \frac{1}{2} nU_T^2\mu C_{ox}'' \frac{W}{L} \]

EWK

ACM

unary specific current \((W = L)\)
The compact model (2)

norm. drain current (saturation)

\[ i = q^2 + q \]

normalized mobile charge density

\[ q = -\frac{Q_i'}{2nU_TC_{ox}'} \]

channel voltage

\[ V_P - V = U_T \left[ 2(q - 1) + \log(q) \right] \]

pinch-off voltage

\[ V_P = \frac{V_G - V_{To}}{n} \]

gate voltage
The compact model \((3)\)

\[
I_D = I_{D\text{Forward}} - I_{D\text{Reverse}}
\]

\[
V_P - V_S = U_T \left[ 2(q_F - 1) + \log(q_F) \right] \quad V_P - V_D = U_T \left[ 2(q_R - 1) + \log(q_R) \right]
\]

\[
i = q_F^2 + q_F - (q_R^2 + q_R)
\]
Example: $I_{Du}(V_G)$ of grounded source ($V_S = 0$ V) saturated ($q \Rightarrow q_F$) transistor

Parametric method

\[
q_F \quad \begin{cases} 
  i &= q_F^2 + q_F \\ 
  V_P &= U_T(2(q_F-1) + \log q_F) 
\end{cases} \quad \implies \quad I_{Du} &= iI_{Su} \\
V_G &= nV_P + V_{To}
\]

% data
UT = .026;
n = 1.2;
Isu = 1e-6;
VTo = 0.4;

% compute
qF = logspace(-4,1.2,50);
i = qF.^2 + qF;
ID = i*Isu;
VP = UT*(2*(qF-1) + log(qF));
VG = n*VP + VTo;

% plot
semilogy(VG,ID); grid

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\[
\frac{g_m}{I_D} \text{ of the saturated transistor}
\]

\[
\frac{g_m}{I_D} = \frac{d \log(i)}{dV_G}
\]

\[
\begin{align*}
    \frac{d \log(i)}{i} &= \frac{2q_F + 1}{i} dq_F \\
    \text{and} \\
    dV_G &= n dV_P = n U_T \left( 2 + \frac{1}{q_F} \right) dq_F = n U_T \frac{2q_F + 1}{q_F} dq_F
\end{align*}
\]

\[
\frac{g_m}{I_D} = \frac{1}{n U_T} \frac{q_F}{i} = \frac{1}{n U_T} \frac{1}{q_F + 1}
\]
sizing the Intrinsic Gain Stage by means of the E.K.V. model

% data
\begin{align*}
  f_T &= 1e8; \\
  C &= 1e-12; \\
  n &= 1.2; \\
  I_{su} &= 1e-6; \\
  V_{To} &= 0.4;
\end{align*}

% compute
\begin{align*}
  U_T &= .026; \\
  \omega_T &= 2*\pi*f_T; \\
  g_m &= \omega_T*C; \\
  q_F &= \text{logspace(-4,1.5,50)}; \\
  g_moverI_D &= 1./(n*U_T*(1+q_F)); \\
  I_D &= g_m/g_moverI_D; \\
  I_{Du} &= I_{su}*(q_F+2 + q_F); \\
  WsL &= I_D/I_{Du}; \\
  V_P &= U_T*(2*(q_F+1) + \log(q_F)); \\
  V_G &= n*V_P + V_{To};
\end{align*}

% plot
\begin{align*}
  \text{loglog}(I_D,WsL,'b',I_D,V_G,'r');
\end{align*}
sizing the Intrinsic Gain Stage by means of the E.K.V. model

strong inversion approx.

weak inversion approx.

\[ f_T = 100 \text{ MHz} \]
\[ C = 1 \text{ pF} \]
The basic EKV / ACM model does not apply to short channel devices!

Real $I_D(V_{GS})$ characteristics however look very similar.

\[ L = 100 \text{ nm} \]

\[ L = 500 \text{ nm} \]

90 nm technology
N channel
$W = 10 \mu m$
$V_{SB} = 0 \text{ V}$
• The spatial distribution of electrical fields in the substrate boils down to a 2D problem controlled mainly by $L$, $V_{SB}$, $V_{DS}$, little by $V_{GS}$.

• The inversion layer confines to a 1D problem controlled by $V_{GS}$ and $L$, $V_{SB}$, $V_{DS}$.

• Is it possible to model $I_D(V_G)$ characteristics by means of the EKV / ACM model with parameters that are functions of $L$, $V_S$ and $V_D$?
E.K.V. Identification

to be performed in the common source configuration

For $L$, $V_S$ and $V_{DS}$

$\log(I_D)$

$g_m/I_D$

$1/nU_T$

$80$ to $70\%$

$V_{GS}$

$V_{To}$

mobility degradation
\( I_{su} \) (specific current)

\[
\frac{I_{Du}(V_{GS})}{i} = I_{su}(V_{GS})
\]

\[
\frac{V_{GS} - V_{To}}{n} = V_p \rightarrow q
\]

\[
I_{su} = 2nU_T^2 \mu_o C'_{ox} \theta(i)
\]

mobility degradation factor

polynomial fit

For \( L, V_S \) and \( V_{DS} \)
Verification: $I_u(V_{GS})$ reconstruction

$n, V_{To}$ and $I_{Suo}$

$n$ slope factor

‘experm.’ data

$+++ n, V_{to}, I_{suo}$ and $\theta(i)$

$V_{GS}$ (V)

$N$-channel; $L = 100\text{ nm}$; $V_{DS} = 0.6\text{ V}$; $V_{SB} = 0.6\text{ V}$. 
The graph shows the relationship between $g_m/I_D$ (in $V^{-1}$) and $V_{GS}$ (in $V$). The axes are labeled with $V_{DS} = 0.6\; V$, $V_{SB} = 0\; V$, and $L = 100\; nm$. The red line represents the 'experimental' data, the blue line represents the model, and the green line represents the model (no mob degradation). The graph queries whether there is an edge conductance effect. The text states that $V_{DS} = 0.6\; V$, $V_{SB} = 0\; V$, and $L = 100\; nm$. The graph also illustrates the concept of mobility degradation.
Outline

Sizing...
- the Intrinsic Gain Stage (I.G.S.)
  \( g_m/I_D \) semi-empirical methodology
  \( g_m/I_D \) compact model methodology
  L-V, L-P, short channel I.G.S.

Conclusion
\[
\frac{g_m}{I_D} \quad \text{does not depend on } \ W
\]

as long as \( W \gg W_{\text{min}} \)

(true for most analogue circuits)

depends on \( L, V_{\text{DS}} \) and \( V_{\text{SB}} \) for

- \( V_T \) roll-off
- D.I.B.L.
- C.L.M.
- mobility degradation
- ....
$f_T = 1 \text{ GHz}; \ C_o = 1 \text{ pf}; \ L = 120 \text{ nm}; \ V_S = 0; \ V_{DS} = 0.6 \text{ V};$

strong inversion approx.

weak inversion approx.

$n, V_{To} \text{ and } I_{suo} \text{ no mobility degradation: } \theta = 1$
$f_T = 1 \text{ GHz}; \ C_o = 1 \text{ pf}; \ L = 120 \text{ nm}; \ V_S = 0; \ V_{DS} = 0.6 \text{ V};$

strong inversion approx.

$W/L$

$n, V_{To}$ and $I_{suo}$ with mobility degradation: $\theta(t)$

weak inversion approx.

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Add drain junction cap. to $C_o$

$f_T = 1 \text{ GHz}; \ C_o = 1 \text{ pf}; \ L = 120 \text{ nm}; \ V_S = 0; \ V_{DS} = 0.6 \text{ V}; \ W_{max} = 1 \mu\text{m}.$
Comparison with semi-empirical method (+++ )

\[ f_T = 1 \text{ GHz}; \quad C_o = 1 \text{ pf}; \quad L = 120 \text{ nm}; \quad V_S = 0; \quad V_{DS} = 0.6 \text{ V}; \quad W_{max} = 1 \mu\text{m}; \]
Param. dependence on $V_{DS}$

1) $n$ small
2) $V_{To}$

$V_{SB} = 0$ V.

D.I.B.L.

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Param. dependence on $V_{DS}$

1) $n$ small
2) $V_{To}$
3) $I_{Su}$

-channel length modulation
-mobility degradation (vert)
-mobility (longitudinal)

$V_{SB} = 0$ V.
Param. dependence on $V_{DS}$

1) $n$ small
2) $V_{To}$
3) $I_{Suo}$

$V_{SB} = 0$ V.

$L \ \mu m$
0.100
0.110
0.120
0.130
0.140
0.160
0.500
1.000
4.000

C.M.L.
Param. dependence on $V_{DS}$

1) $n$ small
2) $V_{To}$
3) $I_{suo}$
4) $\theta(i)$

$V_{SB} = 0$ V.
Verification: $I_{Du}(V_{DS})$ reconstruction (S.I.)

- **Experimental model** 
- Model (no mob degradation)

**Verification:** $I_{Du}(V_{DS})$ reconstruction (S.I.)

- 'Experimental'
- Model
- Model (no mob degradation)

---

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Verification: \( I_{Du}(V_{DS}) \) reconstruction (W.I.)

\[ X \times 10^{-9} \]

- Red line: ‘experimental’
- Crosses: model
- Pink line: model (no mob degradation)

\[ V_{GS} \]

- 0.10 V
- 0.05 V
- 0.00 V

\[ V_{DS} \]

- 0.00 V
- 0.20 V
- 0.40 V
- 0.60 V
- 0.80 V
- 1.00 V
- 1.20 V

D.I.B.L.

BWRC, Dec 12, 2008. P.G.A. Jespers
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Conclusion
1) fix **NDPole** and **Zero** with respect to $\omega_T$ to meet phase margin

$$\omega_T = \frac{g_{m1}}{C_m}$$

$$z = \frac{g_{m2}}{C_m} = Z\omega_T$$

$$\omega_{ndp} = \frac{g_{m2}^2}{C_m} \left( \frac{C_m^2}{C_1+C_2} \right) C_m + C_1C_2 = \text{NDP}\omega_T$$

**e.g.** $Z = 10$ and **NDP** = 4…5

for phase margin of approx. 60°
2) Size the ‘A’ transistors.

\[ g_{m1} = \omega r C_m \]

\[ I_{D1} = \left( \frac{g_{m1}}{I_D} \right) \]

\[ \frac{W_1}{L_1} = \frac{I_{D1}}{I_{Du1}} \]

\[ g_{m2} = Z g_{m1} \]

\[ I_{D2} = \frac{g_{m2}}{\left( \frac{g_m}{I_D} \right)_2} \]

\[ \frac{W_2}{L_2} = \frac{I_{D2}}{I_{Du2}} \]
3) Size the ‘B’ transistors.

more constraints

• zero systematic offset

\[ V_{G3} = V_{G2} \]
\[
\left( \frac{W}{L} \right)_3 = \frac{I_{D1}}{I_{Du2}}
\]

• choose bias so that Q4 and Q5 are in strong inversion

\[ I_{Du4} = I_{Du5} \]
\[
\left( \frac{W}{L} \right)_4 = \frac{I_{D2}}{I_{Du4}}
\]
\[
\left( \frac{W}{L} \right)_5 = \frac{2I_{D1}}{I_{Du4}}
\]
4) Estimate $C_1$, $C_2$, $C_3$ and compute $C_m$

Choose …

L\(_1\) medium (voltage gain)
L\(_2\) min. size
L\(_3\) large for min 1/f noise (beware from doublet!)
L\(_4\) matching + size
L\(_5\) matching + common mode rejection

- the parasitic cap. are estimated knowing $W$'s and $L$'s + techno. data
- a new $C_m$ is extracted from inverted NDP equation

$$C_m = 0.5 \frac{NDP}{Z} \cdot \left[ C_1 + C_2 + \sqrt{(C_1 + C_2) + 4 \frac{Z}{NDP} C_1 C_2} \right]$$

reiterate until $C_m$ gets constant
example

Spec:

\[
f_T = 50 \text{ MHz};
C = 1 \text{ pF};
VDD = 1.2 \text{ V};
\]

\[
q_{F1} = 0.0316 \rightarrow 3.16 \\
q_{F2} = 0.10 \rightarrow 2 \\
q_{F4} = 2.90
\]

\[
Z = 10 \\
NDP = 4
\]

\[
L1 = 1 \text{ \mu m} \\
L2 = 0.5 \text{ \mu m} \\
L3 = 1 \text{ \mu m} \\
L4 = 0.5 \text{ \mu m} \\
L5 = 1 \text{ \mu m}
\]
constant active area (µm$^2$)
constant supply (A)

constant active area (µm²) 48
constant gain (dB)
constant supply (A)
constant active area ($\mu m^2$)
constant gain (dB)  
current supply (A)  
constant active area (μm²): 50
The selected point

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<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
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<td>1</td>
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<td>1</td>
<td></td>
</tr>
</tbody>
</table>

\[
gain = 81 \text{ dB}
\]

\[
power \text{ consump.} = 191 \ \mu W
\]
Conclusion

\( g_{m}/I_D \)

- relates a small signal param. to a large signal quantity
- does not vary with transistor widths
- controls the mode of operation, power consump., gain ...

paves the way for sizing CMOS circuits

- semi-empirically
  (look-up tables : \( I_D, g_m, g_d, \ldots \))
- by means of the E.K.V./A.C.M. model
  (parameters look-up tables or fitting functions)
  - simple expressions of \( I_D, g_m/I_D, g_d/I_D \)
  - \( q_F \) monitors mode of operation
  - increased physical insight

suitable for sub-micron low-voltage low-power circuits
$g_m/I_D$ sizing methodology for low-power/voltage CMOS circuits

by P.G A. Jespers

to be published 2009 by Springer

paul.jespers@uclouvain.be
A list of references concerning the $g_m/I_D$ methodology:

1) **A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA.**
   F. Silveira, D. Flandre and P.G.A. Jespers
   (the first reference)

2) **A CAD methodology for optimizing transistor current and sizing in analog CMOS design.**
   *IEEE Trans. on computer-aided design of integrated circuits and systems*,

3) **gm/ID-based mosfet modeling and modern analog design.**
   D. Foty, D. Binkley, Matthias Bucher.

4) **Une méthodologie de conception des amplificateurs opérationnels à faible consommation**
   P. Jespers.

5) **Automated design methodology for CMOS analog circuit blocks in complex systems.**
   contact Prof Vladimirescu, UC Berkeley, BWRC, 2208 Allston Way, Berkeley, CA 94704.

6) **Sizing of MOS transistors for amplifier design.**
   *ISCAS 2000.*

7) **A behavioral model of a 1.8-V flash A/D converter based on device parameters.**
   *IEEE Trans. on computer-aided design of integrated circuits and systems*, vol 19, n° 1,
   Jan 2000, p 69-82