ANALOG SCALING CHALLENGES
AND COMPACT MODELS

Mustafa Badaroglu, Marie-Garcia Bardon, Morin Dehan

IMEC, Leuven, Belgium
badar@imec.be
OUTLINE

Device scaling roadmap
Analog scaling induced by logic
Compact modeling at IMEC
Extrinsic parasitics
Conclusions
FUTURE APPLICATION REQUIREMENTS

HIGH-PERFORMANCE COMPUTING

- Increased performance at constant power density
- Constraints = Thermal and energy budget
- Device: low-Vt, mobility boosters

HIGH-PERFORMANCE MOBILE

- Increased performance at constant leakage
- Constraints = Battery, Leakage in multi-cores
- Device: Strong SCE control
IMEC LOGIC SCALING ROADMAP

V_{dd} 1.0-1.1V 0.9-1.0V 0.8-0.9V 0.7-0.8V 0.6-0.7V 0.5-0.6V < 0.5V

Strain & Advanced Gate Stack Engineering

- SD/stressors
- Metal Gate + High-k

Fully-depleted Channel for Improved Electrostatics

- Ultra-Thin SOI
- Multi-gate FETs

Band-Engineered Channel for Enhanced Transport

- High-Mobility Channels
- Nanowires/Tunnel FETs

- SiGe, Ge IIIV

Novel Materials/New Transport/Extreme Electrostatics

- 2D Materials
- Quantum/Spin Devices

(Bi-layer Graphene)

Tech Node

- 32/28nm
- 14nm
- 7nm

- 45nm
- 22/20nm
- 10nm
- 5nm

- Feature Dimension & Voltage Scaling are concurrent drivers
- Material & Device Architecture Innovations Enablers of continual scaling

imec
SYSTEM SCALING DRIVERS = PPAC

Node-to-node scaling targets

- >50% area downscaling node-to-node
- >30% more fmax node-to-node at constant power
- >20% more fmax at constant leakage
- >35% more fmax at constant energy
- <15% process cost

Pitch scaling to ensure 50% area downscaling

IMEC pitch targets – [nm]

<table>
<thead>
<tr>
<th>Technology node – [nm]</th>
<th>CPP</th>
<th>MP</th>
<th>FP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>110</td>
<td>90</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>82</td>
<td>64</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>58</td>
<td>44</td>
<td>42</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>40</td>
<td>30</td>
</tr>
</tbody>
</table>

CPP=Contacted Poly Pitch (Gate); MP=Metal Pitch; FP=FinFET pitch
DOES DIGITAL-CENTRIC SCALING ENABLE ANALOG SCALING?

**Digital**

- **Short-channel Devices**
  - Reduce delay (CV/I)
  - Reduce power (Vdd)
  - Increase Ion/Ioff
  - Reduce area
  - Improve matching (AVt)
  - Reduce cost / Mgates

**Analog**

- **Short/Long-channel devices**
  - Higher frequency (fT, fmax)
  - Higher intrinsic gain (gm/gds)
  - Higher linearity (IIP3~gm/Id)
  - Lower noise (I/f)
  - Higher matching (AVt)
  - Higher Cratio with high Q

**Passives (add-ons? + existing?)**

- Higher density (R,L,C)
- Higher matching (R, C)
- Higher quality factor (L, C)
- Higher linearity (R,C)
- Lower leakage (C)
- Better temperature behavior (R)

Scaling Drivers of advanced nodes
MPU/SoC is a system with logic, memory, and analog
- PLLs for clock generation
- Bandgap based temperature sensors
- DLLs for the logic and memory interface
- SERDES for high-speed IOs
- Linear DACs for the video display
- Power supply regulators
- IO circuits

More-or-more convergence of RF front-end with digital
- LNA
- Mixers
- LC-VCOs
- ADC
- Power amplifier
SCALING IMPACT ON ANALOG FOMS: ASSUMING AN IDEAL LONG-CHANNEL DEVICE

<table>
<thead>
<tr>
<th>Technology</th>
<th>Quasi-Static</th>
<th>Fixed Vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$K^{-1/2}$</td>
<td>1</td>
</tr>
<tr>
<td>Lateral dimensions</td>
<td>$K^{-1}$</td>
<td>$K^{-1}$</td>
</tr>
<tr>
<td>Vertical dimensions - $t_{ox}$</td>
<td>$K^{-1}$</td>
<td>$K^{-1/2}$</td>
</tr>
<tr>
<td>Doping concentration</td>
<td>$K$</td>
<td>$K$</td>
</tr>
<tr>
<td>$Id_{sat}$</td>
<td>$I$</td>
<td>$K^{1/2}$</td>
</tr>
<tr>
<td>Transconductance (gm)</td>
<td>$K^{1/2}$</td>
<td>$K^{1/2}$</td>
</tr>
<tr>
<td>Out. conductance (gds)</td>
<td>$K^{3/4}$</td>
<td>$K$</td>
</tr>
<tr>
<td>$Cd/Co$</td>
<td>$K^{-1/4}$</td>
<td>1</td>
</tr>
<tr>
<td>SS</td>
<td>$&gt;1$</td>
<td>1</td>
</tr>
<tr>
<td>$1/f$ noise</td>
<td>$I$</td>
<td>$K^{1/2}$</td>
</tr>
<tr>
<td>Long channel index</td>
<td>$K^{-1/6}$</td>
<td>$K^{-1/3}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Circuit parameter</th>
<th>Quasi-Static</th>
<th>Fixed Vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain – gm/gds</td>
<td>$K^{-1/4}$</td>
<td>$K^{-1/2}$</td>
</tr>
<tr>
<td>Voltage gain – 2 stage opamp</td>
<td>$K^{-1/2}$</td>
<td>$K^{-1}$</td>
</tr>
<tr>
<td>Power density</td>
<td>$K^{3/2}$</td>
<td>$K^{5/2}$</td>
</tr>
<tr>
<td>Miller capacitance - $Cc$</td>
<td>$K^{-1}$</td>
<td>$K^{-3/2}$</td>
</tr>
<tr>
<td>Gain bandwidth – gm/Cc</td>
<td>$K^{3/2}$</td>
<td>$K^2$</td>
</tr>
<tr>
<td>Slew rate ($Id_{sat}$ / (Vdd.Cc))</td>
<td>$K^{3/2}$</td>
<td>$K^2$</td>
</tr>
<tr>
<td>SNR – low-frequency apps</td>
<td>$K^{-1/2}$</td>
<td>$K^{-1/2}$</td>
</tr>
</tbody>
</table>

(Source: Wong, IEEE JSSC 1983)

How about non-idealities: short channel, advanced devices, novel layout strategies, ...?
IMPACT OF SCALING ON DEVICE FOMS

Lgate versus tox scaling
Doping control
Workfunction tuning
Advanced devices

Careful layout
Reduced capacitance
Reduced gate and S/D resistance

[Source: ITRS]
NEW DEVICE ARCHITECTURES IMPROVE GM/GDS

less short-channel effect → higher intrinsic gain (gm/gds)

\[ \frac{g_m}{g_{ds}} \]

\[ V_{GS} - V_t = 0.2V \]

FinFET

planar

L_G (nm)

100

1000

10

100

V_{GS} - V_t = 0.2V
FinFETs give a better trade off between speed and gain WRT planar

FinFETs offer a serious alternative to planar Devices for digital and low frequency analog applications...
A BETTER SCE IMPROVES ALSO THE CURRENT EFFICIENCY – NARROW FIN BRINGS BETTER LINEARITY
I/F NOISE GETS BETTER WITH TECHNOLOGY SCALING

[source: IEDM ‘10 C.H. Jan]
COMPACT MODEL IS DETRIMENTAL IN DESIGN-TECHNOLOGY ASSESSMENT

- Process assumptions
  - Design rules
  - Compact models
  - Parasitics
- Standard cell
  - SRAM
  - SoC PPA-C

TCAD $\rightarrow$ CM

CELL

EXTRINSIC PARASITICS
IMEC PRE SILICON ROADMAP

Technology definition

Process / technology assumptions

Experimental vehicles

TCAD results

Reference data

Compact models

System assessment

PPAC

Performance

Power

Area

Cost

ring oscillators to system level

Change layout

Applications targets met?

Change assumptions and process flow

Change parameters

Experimental vehicles

TCAD results

Reference data

Compact models

PPAC

Performance

Power

Area

Cost

ring oscillators to system level

Change layout

Applications targets met?
COMPACT MODELLING APPROACH

- Follow compact models industry standards
- Develop ad hoc macro models
- Silicon validation

- First model to get early electrical simulations
- Add effects in function of need and data availability
  Macro models
- Corners, Vt flavors, variability
- Verify and validate on imec chips

- Technology assumptions
- Silicon data

- Target model
  - Active area size
  - Gate last / gate first
  - Local interconnect

- Post-layout simulations
  - Proximity effects

- Back annotations
**EXAMPLE: FINFET SCALING @ IMEC**

- Unique FinFET Reliability & RTN
- Special Implants & Doping
- Advanced Gatestack for FinFETs
- Enabling of aggressive 14nm FEOL+BEOL platform
- Scaling platform to accelerate 10nm & beyond R&D

Variability Bulk Vs. SOI

S/D Epi stressors (SiGe & Si:C)
EXAMPLE: INCLUDING LDE IN BFF14 MODEL

TCAD stress simulations

Analytical stress profiles
stress = f(sa, sb)

Stress to electrical parameters

Compact model
imec macro

Compact model BSIM CMG

Experimental data
BFF14

Structures for Layout dependent effects

Inclusion of layout dependent effects in macro
Considering stress from
• EPI Source/Drain
• STI
• Replacement Metal Gate
• Local interconnect
• ...

Physics based compact model

calibration
2013
BUILDING COMPACT MODEL

TCAD ELECTROSTATIC

W_in = 10 nm
H_fin = 30 nm

Physical parameter inputs for BSIM CMG physical MODEL:
- FW FH
- Lg
- Tox
- channel doping
- Gate work function
- geometry and doping for parasitic capacitances and resistances
EXAMPLE: INCLUDING LDE IN BFF14 MODEL

From layout dependent stress to RO performance

NFET
STI tensile 1 GPa

PFET
SiGe no recess 3 Pa
STI tensile 1 GPa

TCAD stress along fin

Peak stress

Mobility

Ion currents

RO frequency

EXAMPLE: INCLUDING LDE IN BFF14 MODEL
From layout dependent stress to RO performance
TwinPeaks test-site T/O
- 14nm CPP58/62, FP45
- 10nm CPP40/45/50, FP30

FET arrays, Matching, LDE

Ring Oscillators

14nm design exploration
- Standard cell architecture
- Technology options (PDK)
- PPA-C
DEVICE ARCHITECTURE INFLUENCES EXTRINSIC PARASITICS

Parasitic resistances might become larger than the channel resistance

Parasitic capacitance might become larger than the one of intrinsic gate capacitance
# 20nm Device Options:
- Bulk Planar
- UTB SOI
- Bulk FinFET

## 20nm BPL/UTB/BFF (193i DP)

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF width</td>
<td>16</td>
</tr>
<tr>
<td>FF height</td>
<td>35</td>
</tr>
<tr>
<td>FF pitch</td>
<td>64</td>
</tr>
<tr>
<td>Mgate width</td>
<td>22</td>
</tr>
<tr>
<td>Mgate pitch</td>
<td>82</td>
</tr>
<tr>
<td>Mgate cut</td>
<td>50</td>
</tr>
<tr>
<td>Mgate-active extension</td>
<td>30</td>
</tr>
<tr>
<td>IM1 bottom width</td>
<td>22</td>
</tr>
<tr>
<td>IM1 pitch</td>
<td>82</td>
</tr>
<tr>
<td>IM2 bottom width</td>
<td>24</td>
</tr>
<tr>
<td>IM2 pitch</td>
<td>82</td>
</tr>
<tr>
<td>Via0 size*</td>
<td>50x40</td>
</tr>
<tr>
<td>Via0 pitch_horz</td>
<td>82</td>
</tr>
<tr>
<td>Via0 pitch_vert</td>
<td>64</td>
</tr>
<tr>
<td>M1 width</td>
<td>32</td>
</tr>
<tr>
<td>M1 pitch</td>
<td>64</td>
</tr>
<tr>
<td>M1 tip-to-tip (same/split)</td>
<td>80/40</td>
</tr>
</tbody>
</table>

*physical Via0 is generated with a Boolean (AND) operation from the drawn via0 & metal gds layers – based on dual damascene Cu process assumption

## Similar assumption for Everest LI28 (under processing..)

![Diagram of 20nm BPL/UTB/BFF (193i DP)](image)

Double patterning M1 (LELE)
LOCAL INTERCONNECT (IM1) TO GATE COUPLING IS DOMINANT

On Fin

Between Fins

Average Gate to IM1 Capacitance

- 20nm node

+57%

+50%

Gate to IM1 spacing, nm

Capacitance, ff/um
AN INVERTER WITH PARASITICS

<table>
<thead>
<tr>
<th></th>
<th>UTBSOI with FBB</th>
<th>BFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Li1 to gate capacitance</td>
<td>170 aF/um</td>
<td>300 aF/um</td>
</tr>
<tr>
<td>Li2 to gate capacitance</td>
<td>140 aF/um</td>
<td>140 aF/um</td>
</tr>
<tr>
<td>Li1 to active resistance</td>
<td>0.25 Ω/um²</td>
<td>0.25 Ω/um²</td>
</tr>
<tr>
<td>M1 to gate capacitance</td>
<td>14 aF/um</td>
<td>14 aF/um</td>
</tr>
<tr>
<td>Via0 resistance</td>
<td>17.9 Ω</td>
<td>17.9 Ω</td>
</tr>
<tr>
<td>M1 routing capacitance</td>
<td>16.5 aF/um</td>
<td>16.5 aF/um</td>
</tr>
<tr>
<td>M1 routing resistance</td>
<td>0.84 Ω/□</td>
<td>0.84 Ω/□</td>
</tr>
<tr>
<td>Li1 routing resistance</td>
<td>29.45 Ω/□</td>
<td>14.73 Ω/□</td>
</tr>
</tbody>
</table>

Wp=192n, Wn=160n  Wp=258n, Wn=258n

Planar / UTB-SOI inverter

Bulk finFET inverter
STAND-ALONE IMPACT OF A PARASITIC WHEN OTHERS ARE EXCLUDED

- IM1-to-gate coupling capacitance impacts the delay most
- Its stand-alone impact in delay is 42.3%

Overall impact = 60.2%
CONCLUSIONS

Analog scaling challenged by parasitics, matching, and low headroom

- Mitigated with circuit and device innovations that exploits advantages of scaling

New device architectures help analog scaling in logic technologies

- Lower gm/gds is mitigated by new device architectures
- Advanced gate stack engineering improves 1/f and device reliability

Compact model must be compatible with the process assumptions baseline

FinFETs suffer from extrinsic parasitics: particularly due to capacitance between gate and S/D
ACKNOWLEDGMENTS

IMEC’s (sub-)22nm CMOS partners including Intel, Micron, Panasonic, Samsung, TSMC, Elpida, SK-Hynix, Sony, Fujitsu, GlobalFoundries, and Toshiba/Sandisk

European Commission and Regional Authorities for their support of European collaborative projects