PSP model update

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outline

- some history
- brief overview of PSP
  - benefits for analog/RF design
- recent updates
  - simulation speed (not shown)
  - self heating
  - improved thermal noise model implementation
- summary

history

PSP is available as built-in model in all major circuit simulators
Verilog-A code & documentation available from http://psp.ewi.tudelft.nl
C-code (SiMKit) available from http://www.nxp.com/models

- 2005: PSP created by merging SP (Pennsylvania State University) and MOS Model 11 (Philips)
- 2005: PSP 102 is elected as CMC standard MOS model
  - Arizona State University (formerly PennState): supporting institution
  - NXP Semiconductors (formerly Philips): co-developer
- 2005-2010: several model improvements, introduction of PSP103
- 2011
  - cooperation CMC and Arizona State University ends
  - NXP and Delft University of Technology start cooperation on PSP
- 2012
  - CMC re-instates PSP as CMC-standard model
  - Delft University of Technology (Prof. Ramses v.d. Toorn): supporting institution
  - December: first PSP release (103.2) from Delft University of Technology

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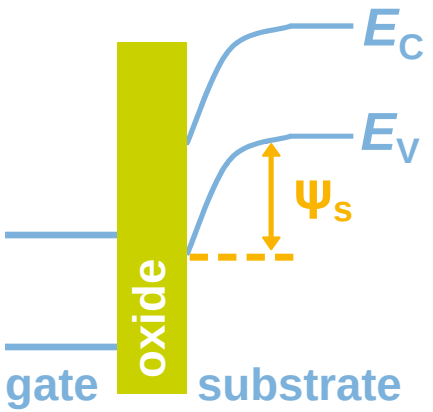
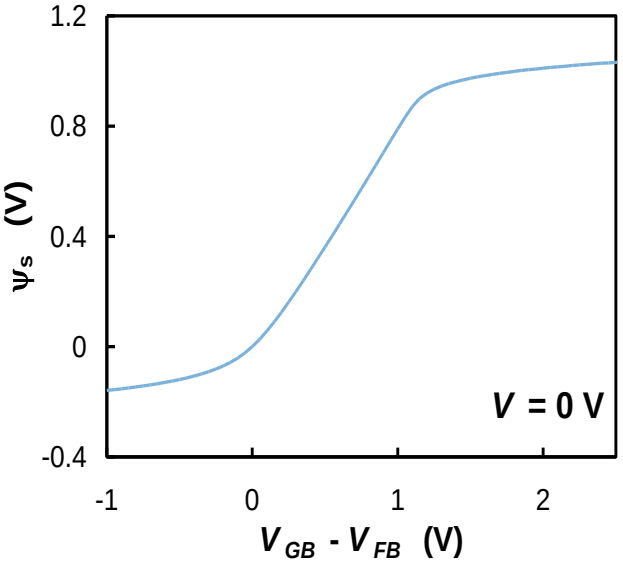
core model: surface potential calculation

- Poisson equation + Gauss's law leads to *implicit* equation for ψ_s

$$\left(\frac{V_{GB}-V_{FB}-\psi_s}{\gamma_o}\right)^2 = \psi_s + \varphi_T \cdot e^{\frac{-\varphi_B - V}{\varphi_T}} \cdot \left(e^{\frac{\psi_s}{\varphi_T}} - 1\right) + \varphi_T \cdot \left(e^{-\frac{\psi_s}{\varphi_T}} - 1\right)$$



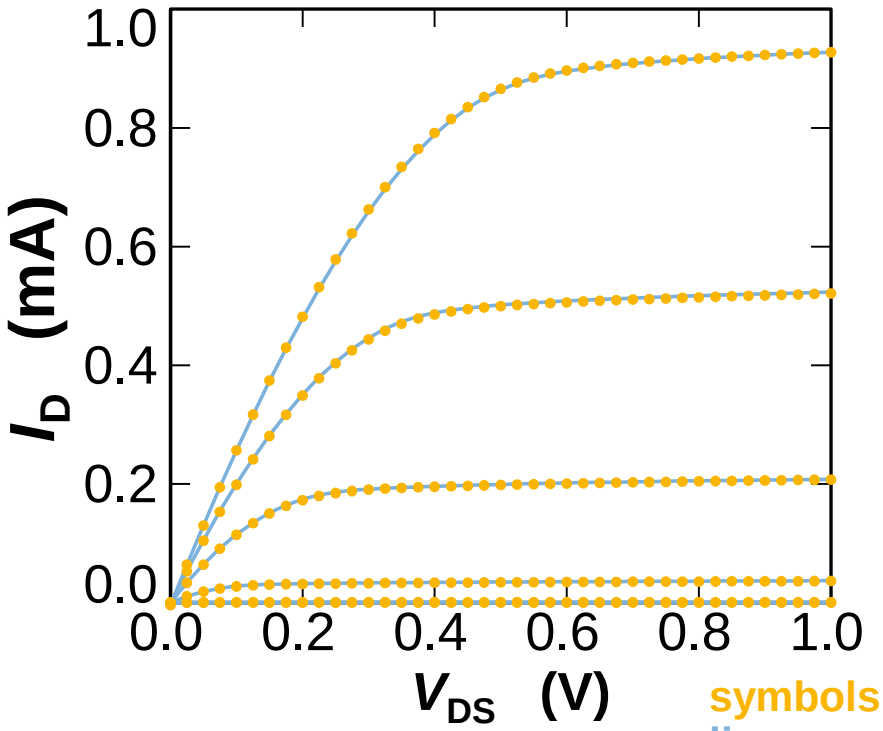
- ψ_s can be calculated
  - with iterative methods (HiSIM, MM1102)
  - with analytical approximations (PSP, SP, MM1101)
- PSP: explicit analytical approximation
  - accuracy <1nV under all relevant conditions)

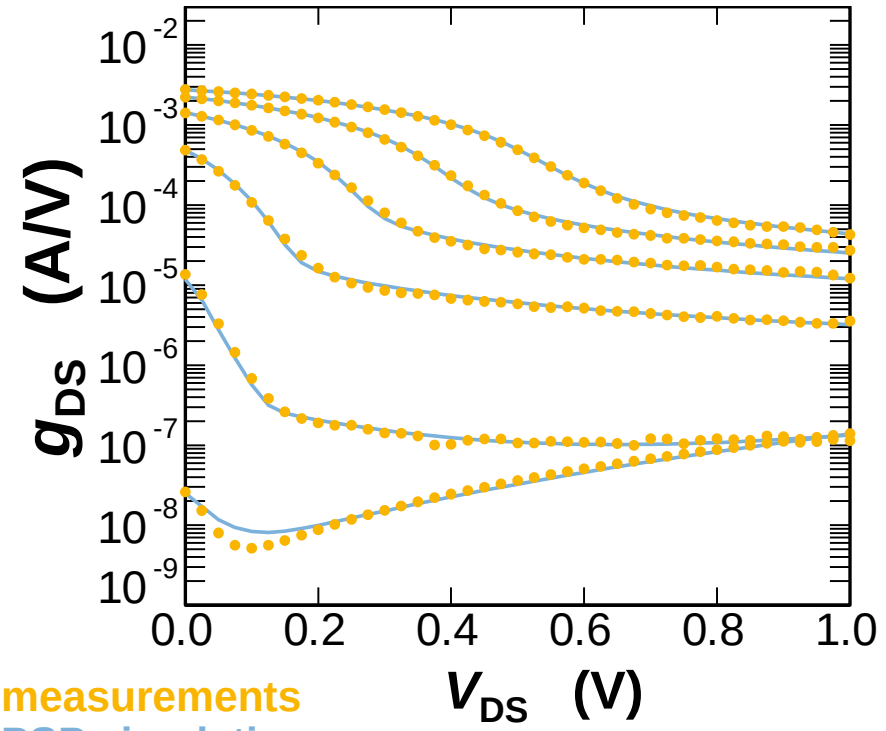


long channel output conductance

crucial for analog design!

I_D-V_{DS} and g_{DS}-V_{DS} for V_{SB}=0V and T=25°C



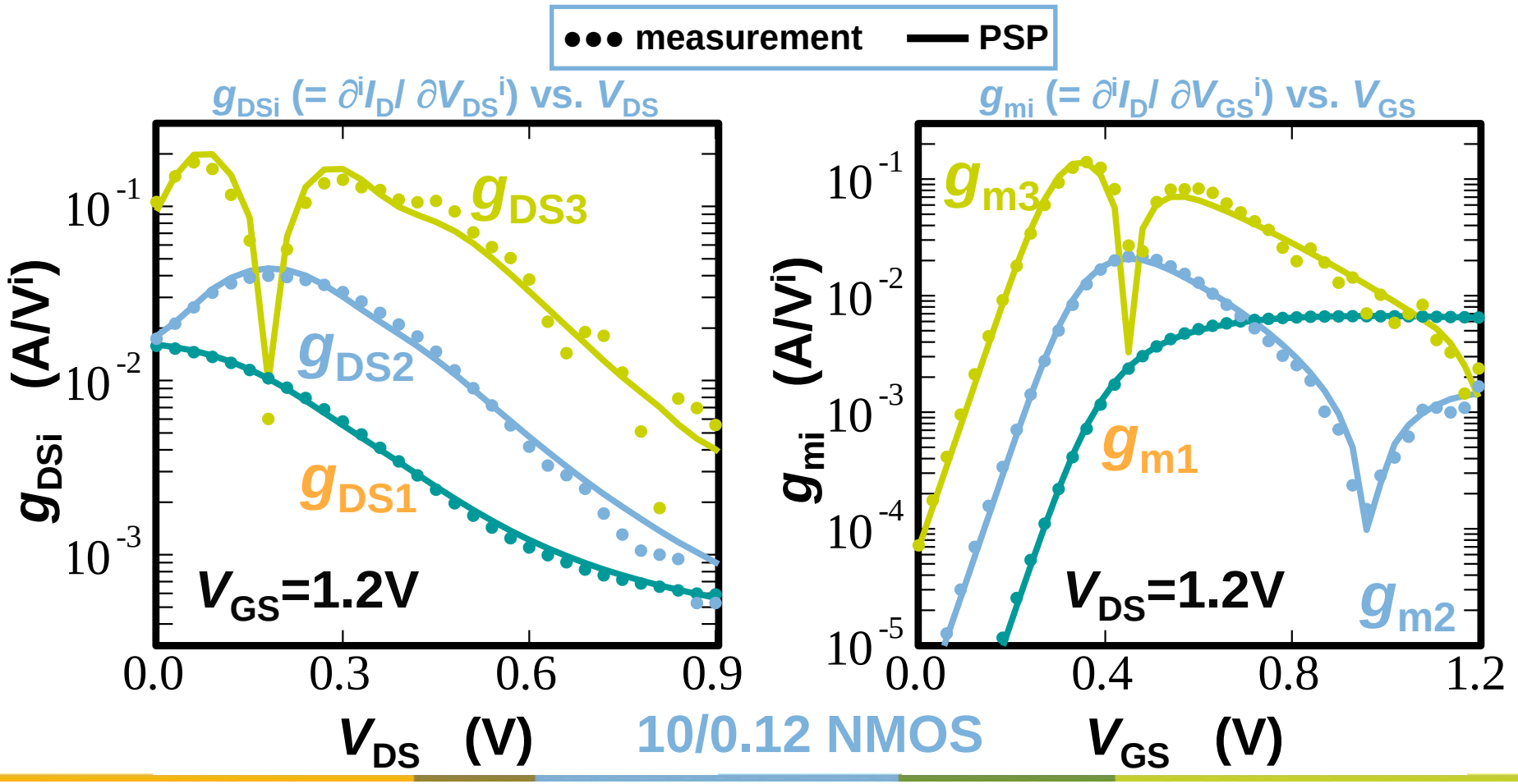


symbols measurements
lines PSP simulations

10µm/1µm NMOS (65nm process technology)

higher order conductance

crucial for distortion (IP3) modeling

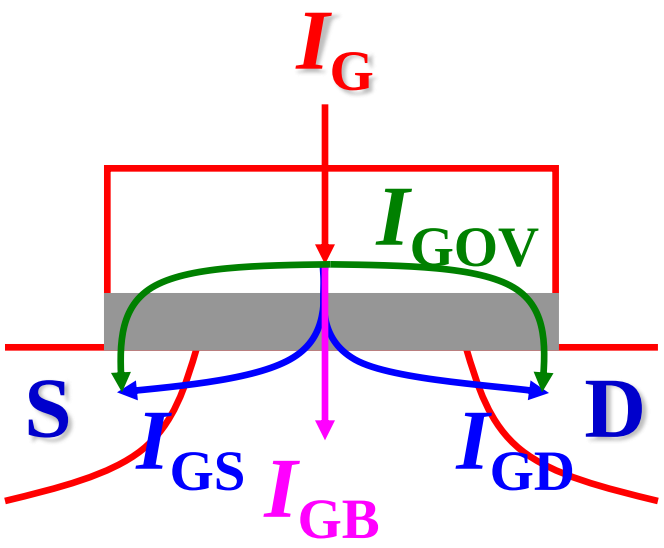


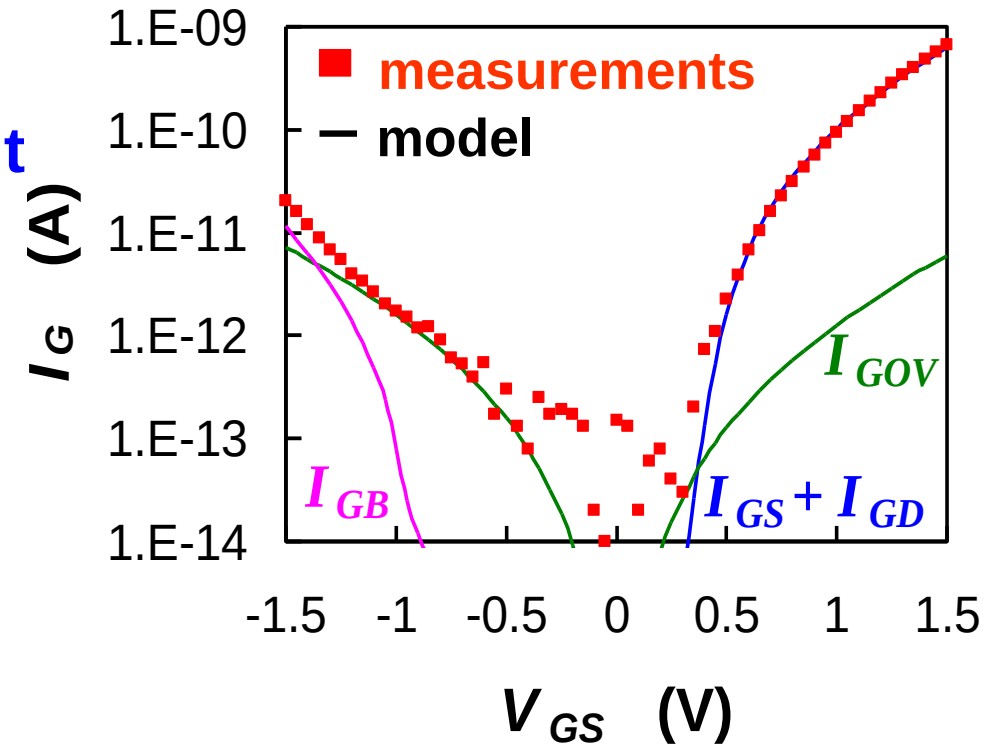
good results due to PSP's mobility model and implementation of SCEs

leakage: gate current

3 components:

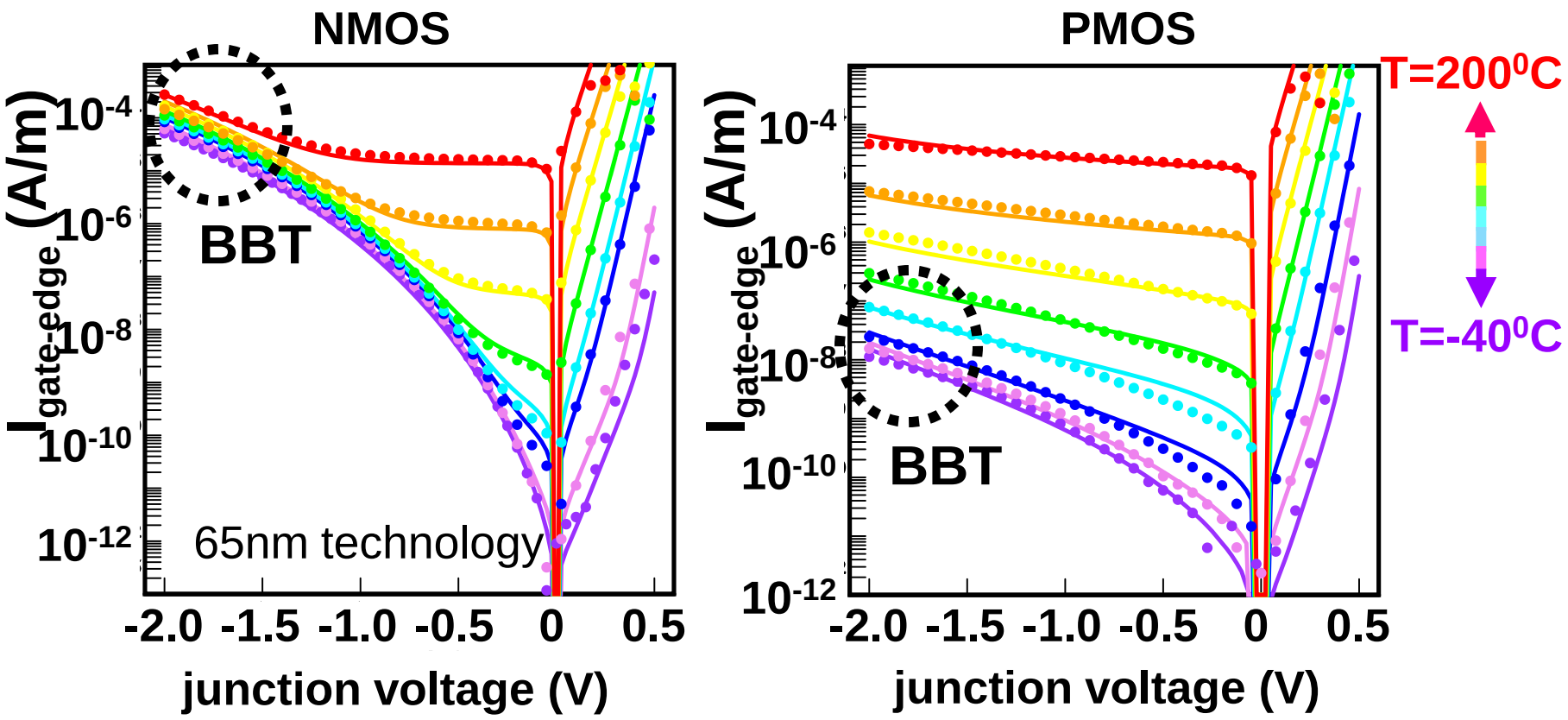
- gate-to-channel current
- gate-overlap current
- gate-to-bulk current





PSP features dynamic (bias dependent) S/D-partitioning of gate current

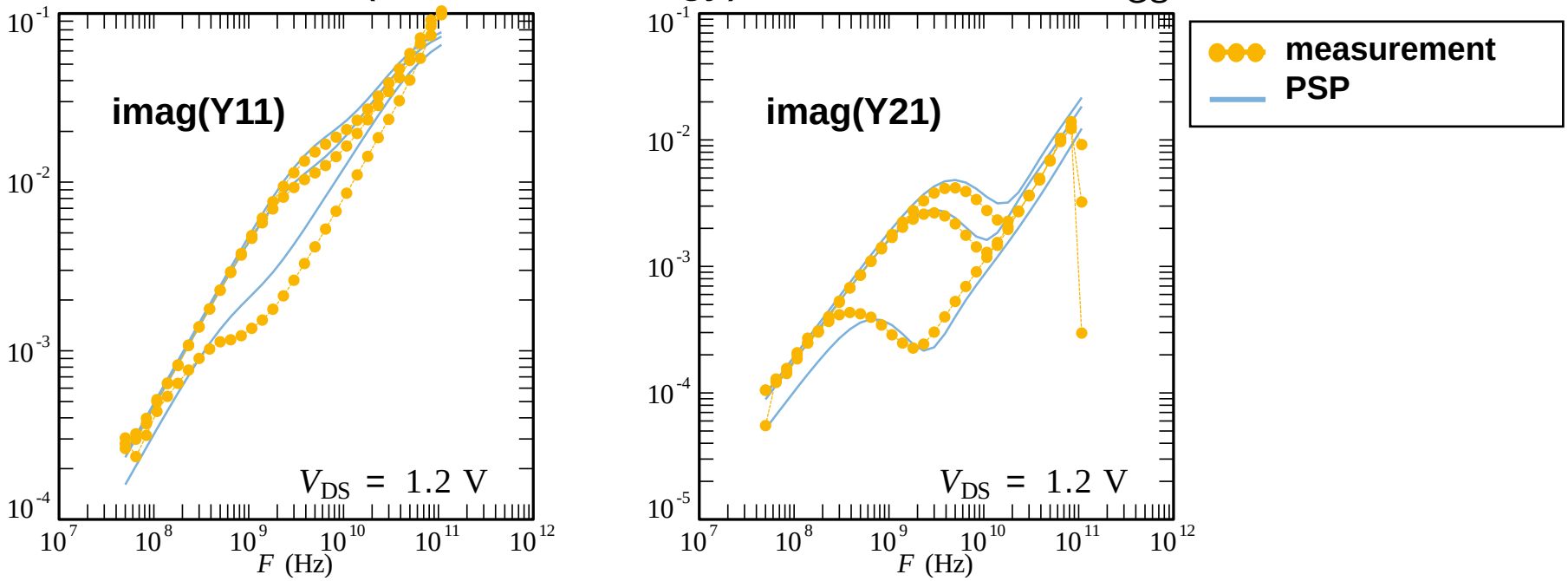
leakage: junction current



advanced CMOS: increasing importance of BBT

Non-quasi-static effects

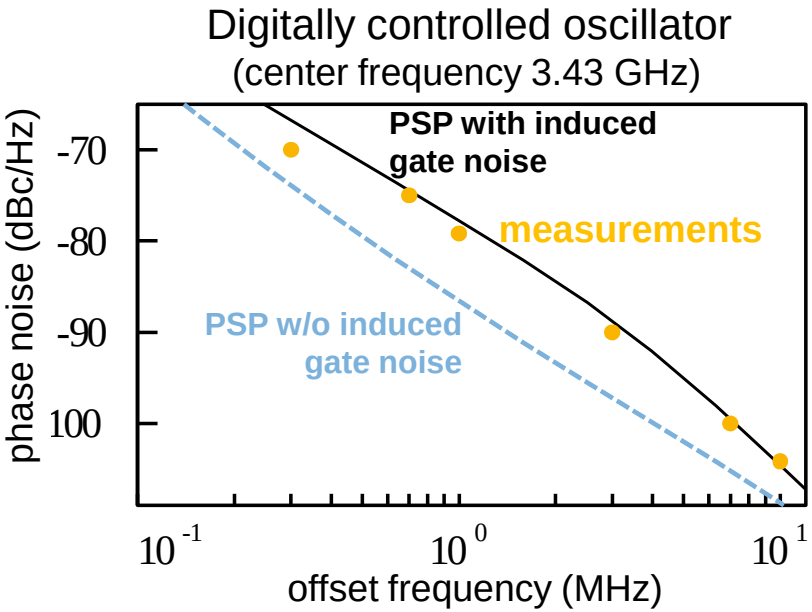
L=2um (90nm technology), NMOS, various V_{GS}

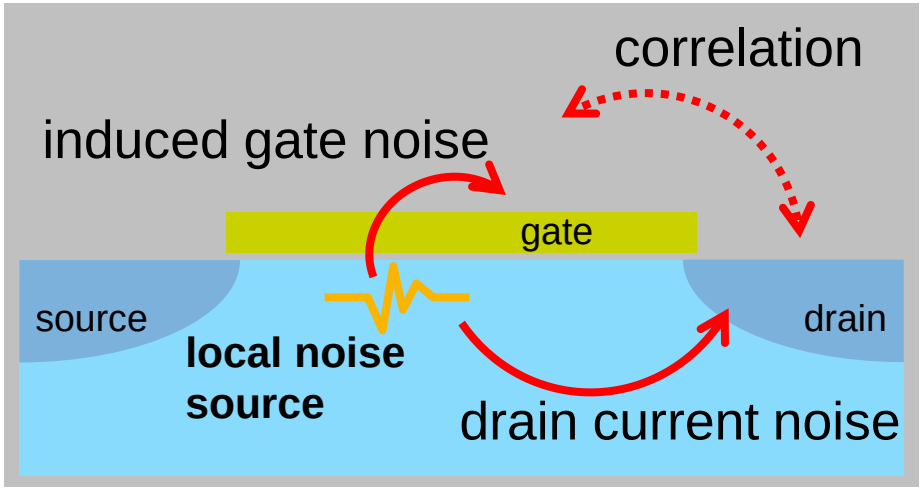


- PSP NQS model based on ‘spline collocation method’
  - predictive model (no parameter extraction needed)
  - based on same physics as segmentation
  - more computationally efficient

thermal noise modeling

- thermal noise originates from resistive nature of MOSFET channel
- PSP has a predictive model for thermal noise
  - based on pure thermal noise
  - includes drain current noise, induced gate noise, and correlation
  - proper integration along channel, correct transfer to terminals
  - valid in all operating regions (linear, saturation, sub-threshold)





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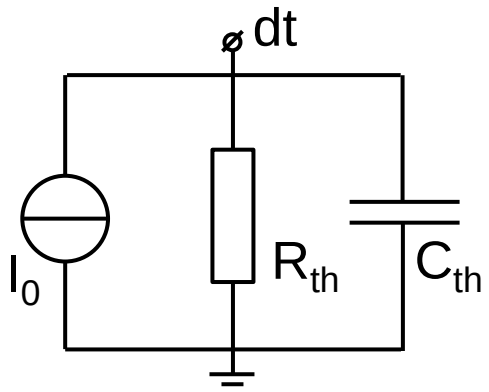
new in PSP: self heating (i)

- motivation:
  - create possibility to use PSP in macro model for DMOS devices
  - possibly also useful for ‘normal’ high-power devices
  - useful when analyzing simulation/measurement discrepancies
- simple RC thermal network, external thermal node
  - $V(\mathrm{dt})=\Delta T$
  - $I_0 = P_{diss} = I_{ds} * V_{ds} + \ldots$

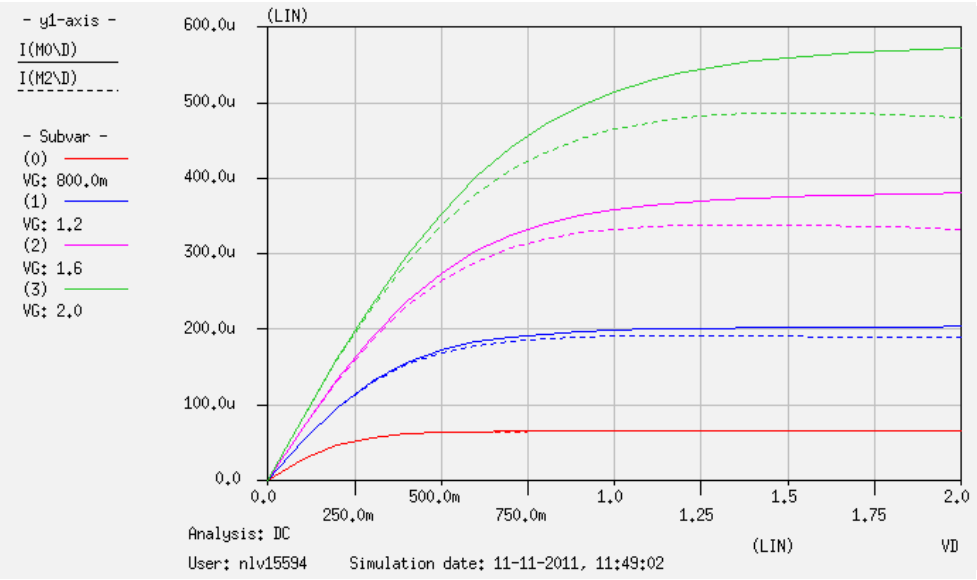


new in PSP: self heating (ii)

- identical parameter sets; with and without self heating

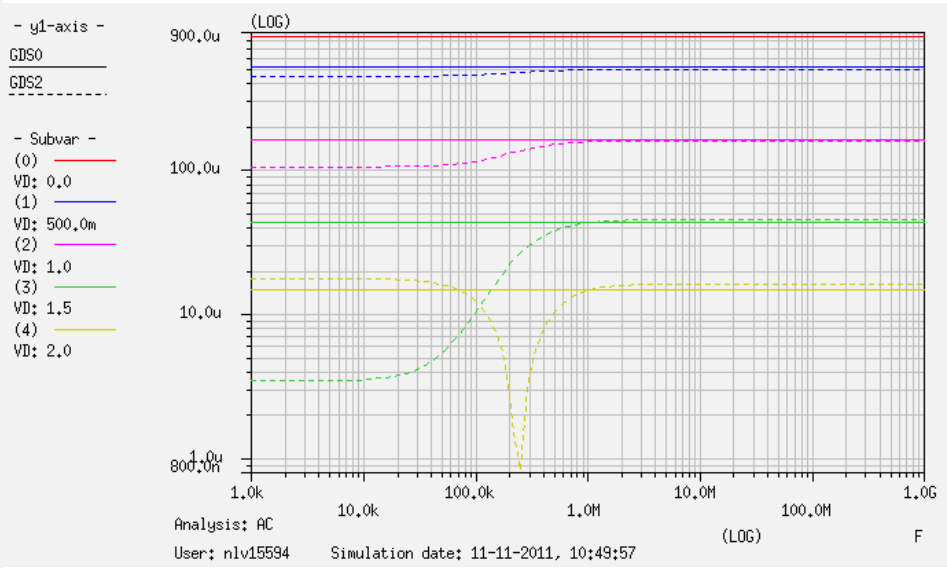
——— PSP103
-------- PSP103t

Id vs. Vd



(dc-simulation)

gds vs. frequency

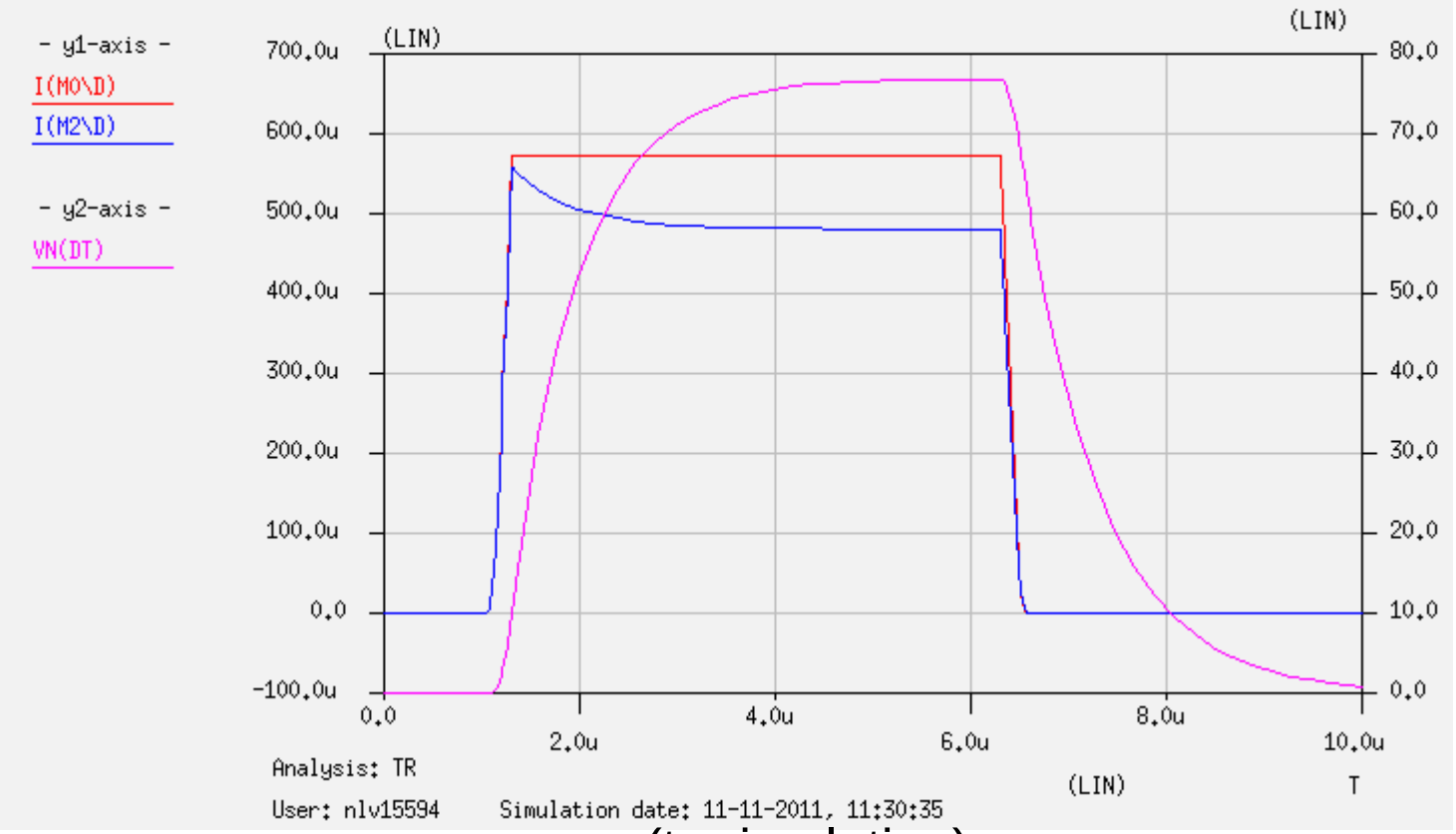


(ac-simulation)

new in PSP: self heating (iii)

- Vds=2V, pulse Vgs 0→2V and 2→0V

PSP103
PSP103t
ΔT



(tr-simulation)

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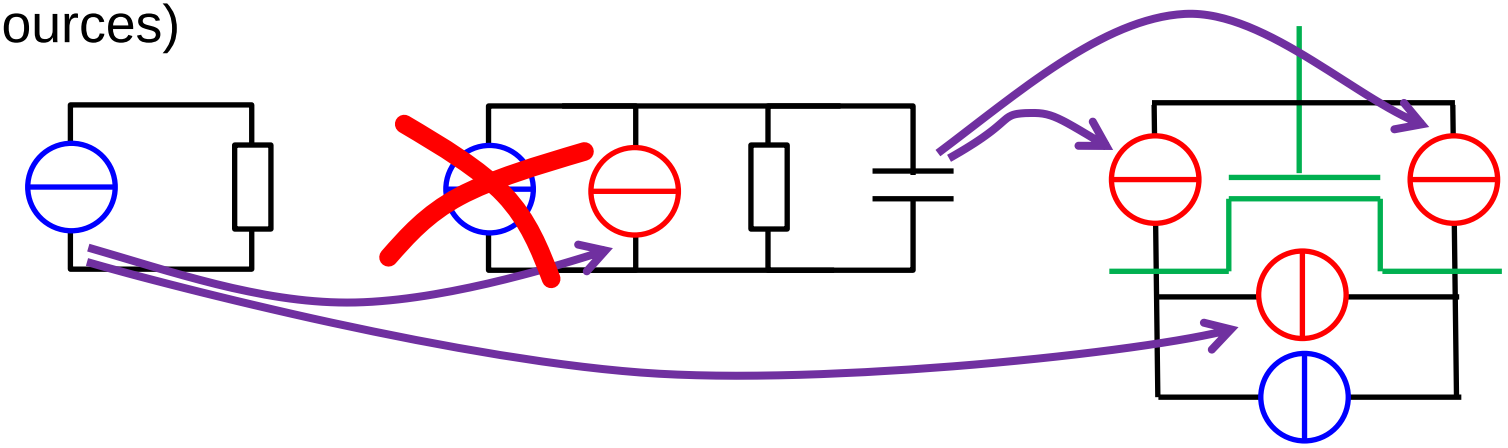
new in PSP: improved noise implementation (i)

simplified verilog-A implementation

- **originally**: three independent white noise sources (+ four controlled sources)

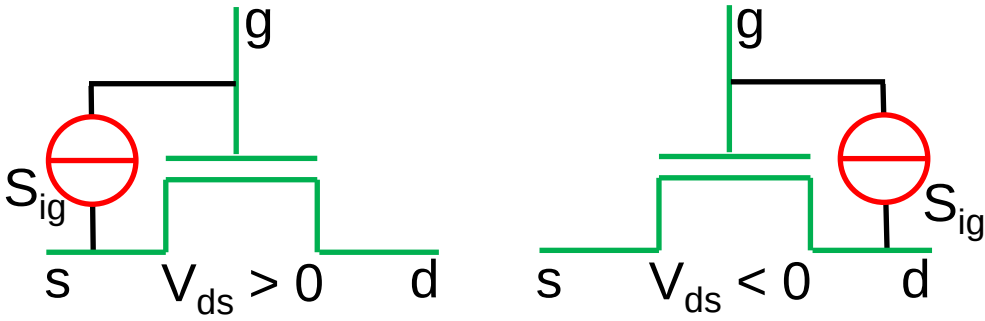


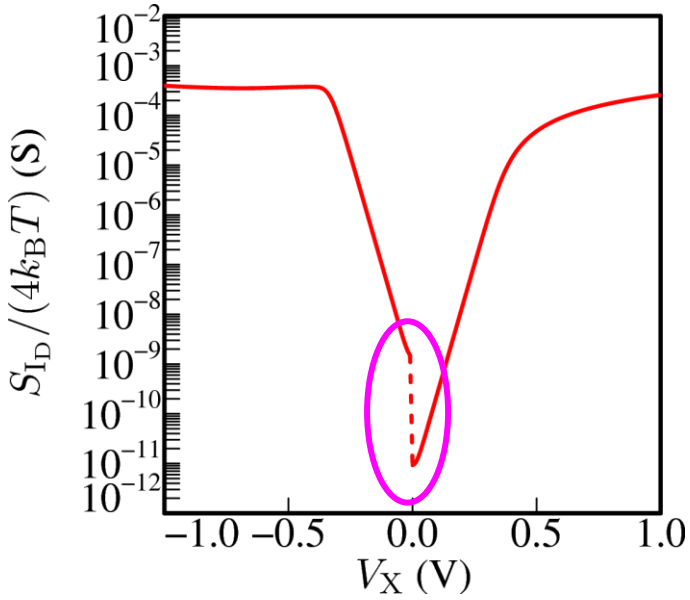
- **new**: two independent white noise sources (+ four controlled sources)
  - *two* independent sources are sufficient to create two (partially) correlated sources
  - noise powers and transfer ratios adjusted to ensure unchanged results
  - noise powers now all have ‘physical’ values

new in PSP: improved noise implementation (ii)

improved symmetry

- PSP 103.1.1 and before: S_{ig}-source changes location when V_{ds} crosses 0
- causes a discontinuity in drain current noise around V_{ds}=0
  - only visible at very high frequency
  - thought to be harmless
  - recently found that this may cause non-convergence in transient noise analysis

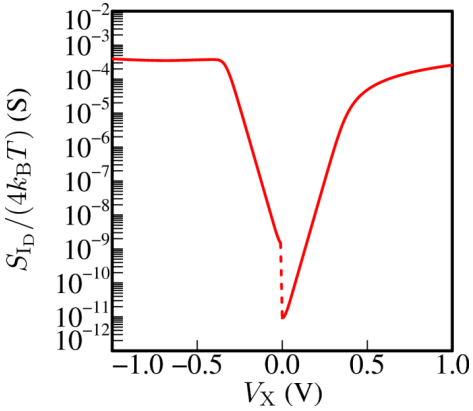




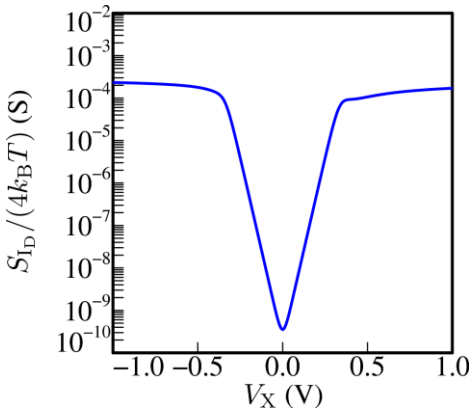
N.B. V_X on drain, $-V_X$ on source

new in PSP: improved noise implementation (iii)

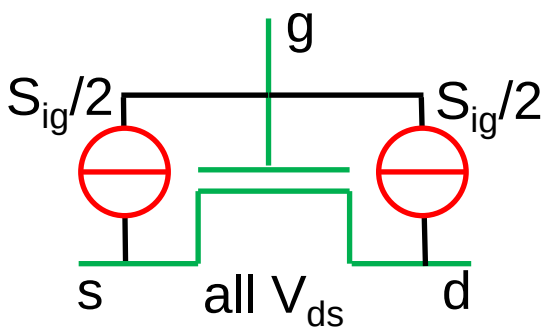
- solution: induced gate noise partitioning over source and drain
  - fully physical, bias-dependent, partitioning seems over-the-top
  - PSP103.2: 50/50 partitioning (removes discontinuity and solves convergence issue)



older PSP



PSP 103.2

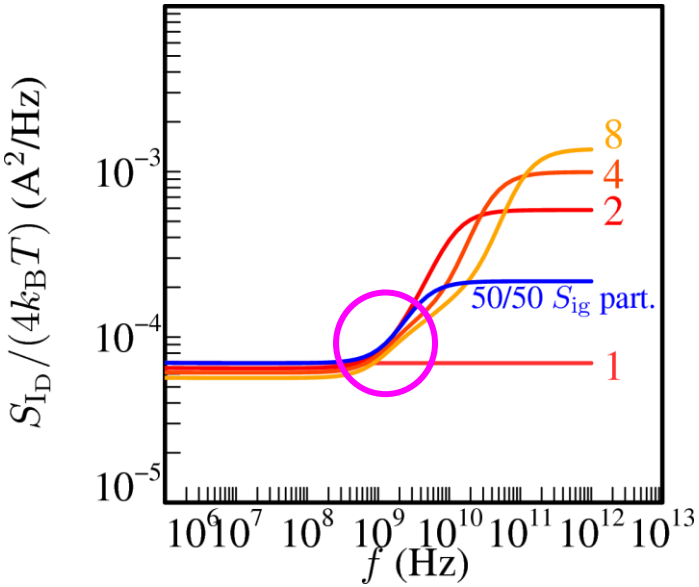


PSP 103.2

N.B. A truly symmetrical plot is obtained when plotting S_{Id}+S_{Is}, but such a plot fails to show the original problem in S_{Id} itself!

new in PSP: improved noise implementation (iv)

- bonus from 50/50 partitioning:
  1st-order NQS effect in S_{id}!
- explanation:
  - induced gate noise is essentially a NQS effect
  - same effect gives f-dependence on S_{id}
- old model (PSP103.1.1 and before):
  - induced gate noise source between g & s
  - no NQS effect in drain current noise
- new model (PSP 103.2.0):
  - 50/50 partitioning
  - induced-gate noise partly flows to drain
  - correct 1st-order *f*-dependence in S_{id}!



comparison of segmentation (1, 2, 4, 8 segments) with 1-segment model with 50/50 partitioning

summary

- PSP is re-instated as CMC-standard model
- supporting institution: Delft University of Technology
  - Prof. Ramses van der Toorn
  - also hosts MEXTRAM model
- co-developer: NXP Semiconductors
- new PSP 103.2 recently released
  - improved simulation speed
  - self heating
  - improved implementation of thermal noise model

self heating: scaling

- geometrical scaling
  - adapted from first version: more PSP-like parameter names and constant term added

$$\mathbf{RTH} = \mathbf{RTHO} + \frac{\mathbf{RTHW1}}{\mathbf{RTHW2} + (W_\mathrm{E}/W_\mathrm{EN}) \cdot [1 + \mathbf{RTHLW} \cdot (L_\mathrm{E}/L_\mathrm{EN})]}$$

$$\mathbf{CTH} = \mathbf{CTHO} + \mathbf{CTHW1} \cdot \{\mathbf{CTHW2} + (W_\mathrm{E}/W_\mathrm{EN}) \cdot [1 + \mathbf{CTHLW} \cdot (L_\mathrm{E}/L_\mathrm{EN})]\}$$

- T-scaling for **RTH**
  - exponential T-scaling with parameter **STRTH**
  - base on *ambient* temperature (not device-T), to avoid convergence issues

$$\mathbf{R}_\mathrm{TH} = \mathbf{RTH} \cdot \left(\frac{T_\mathrm{KA}}{T_\mathrm{KR}}\right)^{\mathbf{STRTH}}$$

induced gate noise & S/D interchange (iv)

- For comparison:
  BSIM4, 4.7, tnoimod=2
- same problem as previously in PSP, but smaller magnitude
  - in BSIM4, induced gate noise is limited to 2x drain current noise
  - as a consequence, discontinuity cannot be larger than factor of 2