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Characterization of wearout mechanisms on MOSFET behavior

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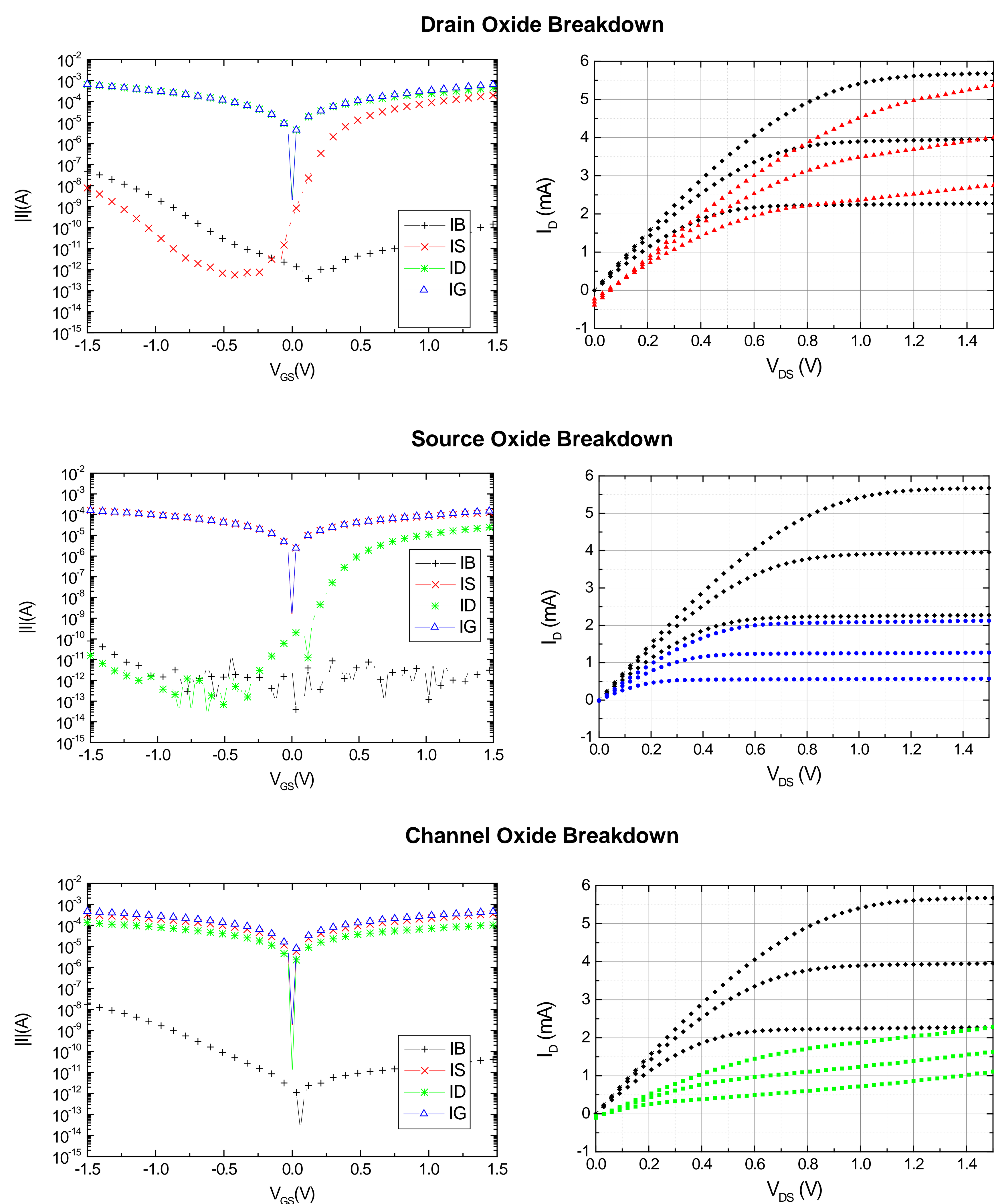
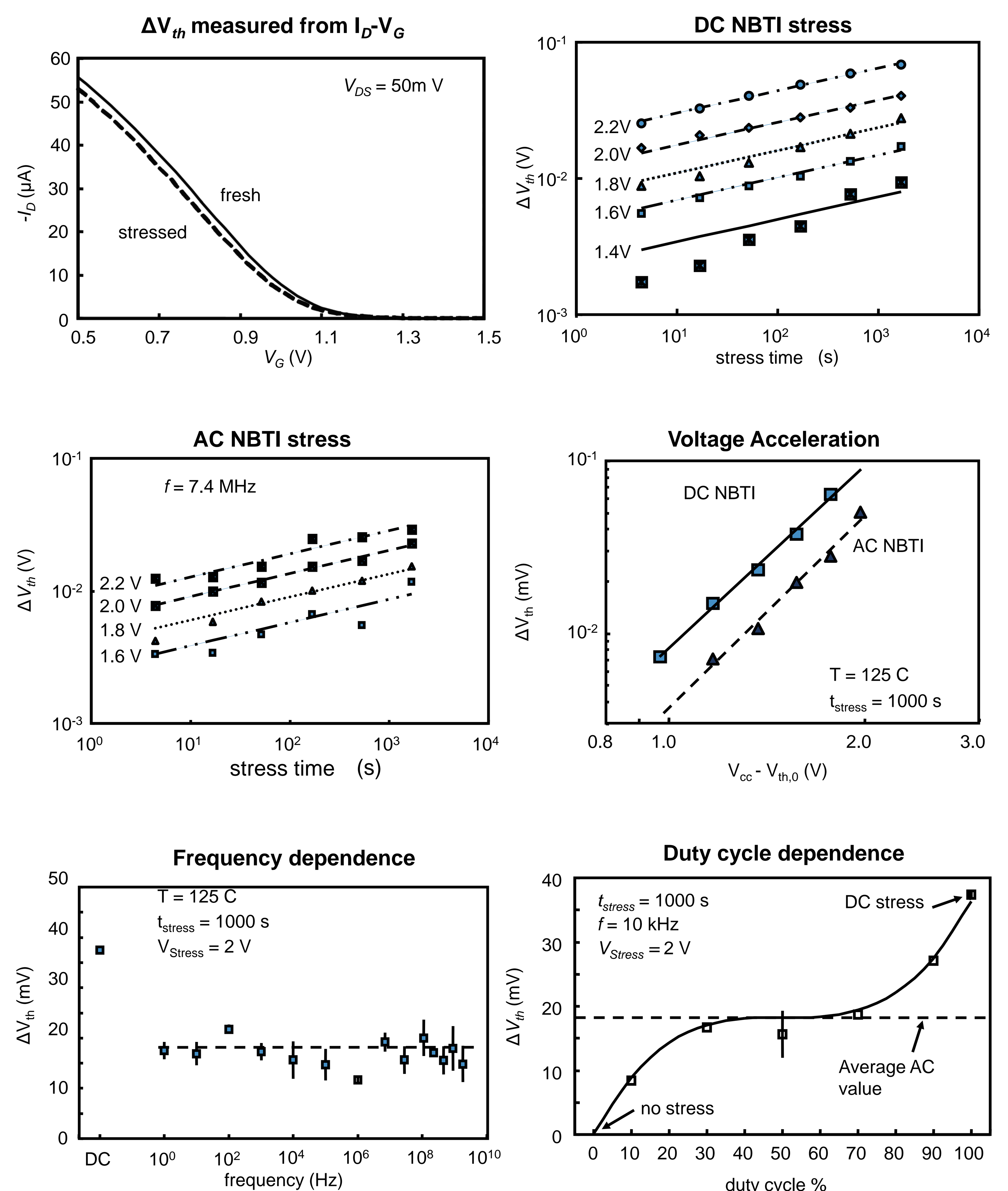
Introduction

- In order to achieve the speed requirements of digital devices, MOSFET downscaling has been continuously produced. The dimensions are actually in the nanometer range.
- At nanometer range, the reliability has become in a major bottleneck in MOSFET downscaling.
- In order to predict the circuits functionality at nanometer range, the wearout problems should be included in MOSFET models.
- Before modelling a deeply characterization of wearout mechanism should be done.
- In this work, the impact of Time Dependent Dielectric Breakdown (TDDB) and Negative Bias Temperatures Instability (NBTI) on MOSFET behaviour are shown.

TDDB



NBTI



Conclusions

- Time dependent dielectric breakdown.
  - After BD a gate-drain and/or gate-source current flows, depending of BD location.
  - The post-BD current gate depends of breakdown hardness.
  - The post-BD MOSFET output behavior depends of breakdown location and hardness.
- Negative Bias Temperature Instability.
  - NBTI increases the V_{TH} of pFET with a power law dependence.
  - AC and DC voltage acceleration are similar.
  - NBTI is observed independent of the stress frequency.
- Work is in progress in order to include this behaviour in compact MOSFET models.