New threshold voltage model for symmetrical undoped DGMOSFET

Paweł Sałek, Lidia Łukasiak, Andrzej Jakubowski

Institute of Microelectronics & Optoelectronics, WUT, Koszykowa 75, 00-662 Warszawa, POLAND

Introduction

Double-gate (DG) structure (Fig. 1) improves SCE control, and, if undoped, reduces the problem of the fluctuations of impurity concentration [1]. The standard threshold definition is no longer valid in undoped devices, therefore a new threshold voltage model is proposed for symmetrical undoped double gate MOS transistor (DGMOSFET).

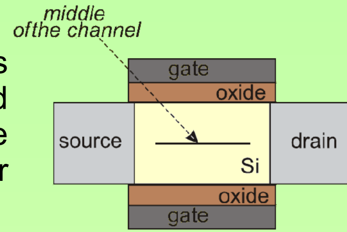

Fig.1. Simplified cross-section of a symmetrical double-gate MOSFET

Threshold definition

The dependence of surface potential on gate voltage (Fig.2) is linear in the subthreshold region ($\varphi_S \approx V_{GS}-V_{FB}=V_G$) and non-linear above threshold. The new definition states that threshold is at the point where this dependence deviates sufficiently (by $\Delta\varphi_S$ – a fitting parameter) from linearity. The value of $\Delta\varphi_S$ will be established later by means of a comparison with ATLAS [2] simulations.

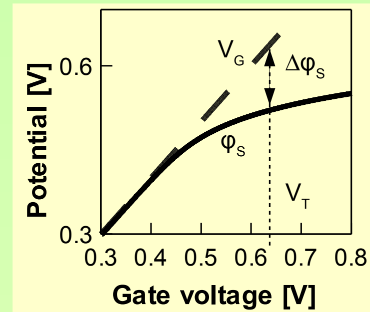

Fig.2. Surface potential (φ_S) vs. gate voltage at zero drain voltage

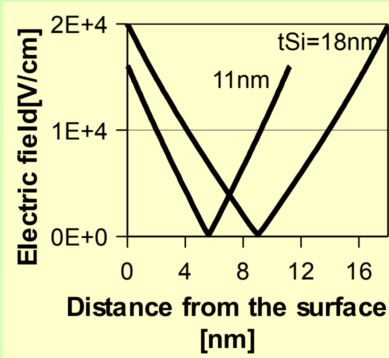

Fig.3. Electric field across the channel

Calculations

Derivation of an analytic description of V_T requires a closed form model of the φ_S versus V_G dependence.

Since the electric field (Fig.3) across the channel is almost a linear function of position, the potential across the channel can be approximated as:

$$\phi(x,V_G,...)=g(V_G,...)x^2+p(V_G,...)x+h(V_G,...)$$

Solving Poisson's equation in the middle of the channel, one obtains:

$$\phi(x,V_G)=\frac{kT}{q}\mathrm{W}\left(\frac{t_{Si}^2+\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}{kT}\frac{q^2 n_i}{2\varepsilon_{Si}}e^{q\frac{(V_G-V_b)}{kT}}\right)\left(\frac{x^2}{t_{Si}^2+\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}-1\right)+V_G$$

Where: t_{Si} channel thickness

t_{ox} dielectric thickness, other symbols have their usual meaning

Using this formula with the threshold definition described above yields:

$$V_T=\frac{kT}{q}\ln\left(\frac{2\varepsilon_{ox}\Delta\varphi_S}{q n_i t_{ox} t_{Si}}\right)+\Delta\varphi_S\left(\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}+1\right)+V_b$$

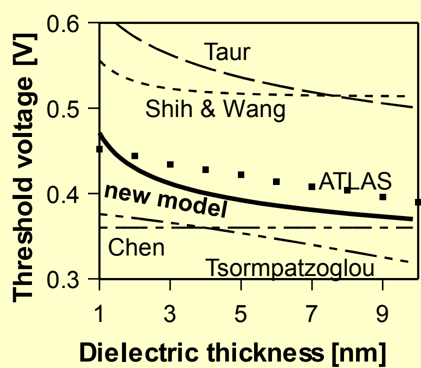

Fig.4. Threshold voltage vs. dielectric thickness for t_{Si}=20nm

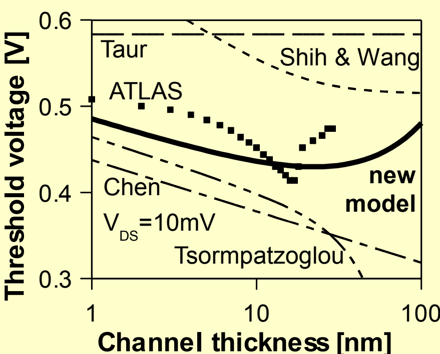

Fig.5. Threshold voltage vs. channel thickness for t_{ox}=2nm

Summary

A comparison of the threshold voltage calculated according to the new model with that extracted from ATLAS simulations of I-V characteristics for a wide range of device parameters (channel and oxide thickness) indicated that the best fit is obtained when $\Delta\varphi_S$ is 1.1 kT/q. The relative error does not exceed 10 percent over the entire range of channel and dielectric thickness interesting for modern microelectronics. Comparison with other existing models [3-6] (Figs. 4, 5) shows that the proposed model can be effectively used as a basis for more complex considerations.

It is also worth noting that the accuracy of the proposed approximate potential description is similar to the more complex model presented in [7].

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