Analytical Two-Dimensional Model for the Parasitic Source/Drain Resistance in DG-MOSFETs

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Motivation & Device Structure

Since DG-MOSFETs reached channel length down to 20nm the parasitic source/drain resistances get more important and can't be neglected. To calculate these resistances in such devices a two-dimensional model in analytical closed form has been derived by using the conformal mapping technique. The model describes accurately the influence of source/drain geometries on access resistances. Bias dependency is obtained by introducing two fitting parameters.

Calculation of the Parasitic Source/Drain Resistances

The parasitic resistances have been calculated using the conformal mapping technique by Schwarz-Christoffel for closed polygons. With this transformation it is possible to map a potential problem given in plane z into the upper half of the complex w-plane to simplify the problem.

We used the following complex potential function to calculate the current flow and from that the resistances in w-plane:

\[ P = \phi + j \pi = \phi_2 + j \left( \frac{\phi_2 - \phi_1}{\pi} \right) \coth \left( \frac{\pi}{\alpha} \right) \]

To keep the analytical model as simple as possible we assumed the mobility in source/drain region to be constant. In source extension region (S) the mobility \( \mu_s \) only depends on \( V_s \) and in the drain extension region (D) we used a mobility model depending on \( V_s \) and \( V_d \) (\( \mu_{eff} \)).

\[ \mu_s = \frac{1 + \Theta(V_{gs} - V_{th})}{1 + \Theta(V_{gs} - V_{th}) + \Theta(V_{ds} - V_{d0})} \]

To get the total parasitic resistance the results from the separated areas are superposed.

Comparison Model versus TCAD Sentaurus

In the following we assume a device having a channel width of 1µm. The first figure shows the voltage drop across the total access resistances for DG-MOSFETs with and without raised source/drain (RSD) structures. It can be noticed that a significant voltage drop only occurs for \( V_{gs} > V_{th} \). Therefore in the following plots we focus on operation in strong inversion mode.

In the second figure below we compare our analytical model for the parasitic resistance characteristics for the same devices. The voltage \( V_{gs} \) is set to 0.55V. As we can see the model is in good agreement to the simulation results. One important result is the proof of bias dependent parasitic resistance. The fitting parameters for the bias dependency are kept constant for both structures. The DG-MOSFET with RSD structure has reduced parasitic resistances (about 30 Ohms) compared to a normal DG-MOSFET. This reduction is due to the bigger contact landing area which lowers the contact resistance considerably. This effect is accurately predicted by our model.

In the right figure we compare a DG-MOSFET with RSD structure against a DG-MOSFET with RSD structure and wrapped contacts (w. c.). One can observe a slight decrease in parasitic resistance which is due to the wrapped contacts. This means the current flows mainly through the back contact at source/drain length of 25nm.

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