Analytical Modelling of Short Channel Planar FDSOI and Triple-gateFET Transistors

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1. Context & motivations
- Triple-gate (TGFETs) devices [1,2]: better electrostatic control of the body
- During channel etch, the BOX can be overetched: FETs [3], DFETs [4].
- This paper: definition of a short channel analytical model for TGFET/planar FDSOI transistors.

2. Subthreshold Currents
- 3D solution of the Laplace’s equation, using Fourier’s series development [5]:
- ‘Most leaky path’ approximation and integration of the potential, subthreshold current expressed as:

\[ I_{ss} = \frac{q}{2} \int_{-W/2}^{W/2} \left( \frac{v_L}{V_F} \right)^{1/2} \left( \frac{V_D}{V_F} \right) \, dx \]

3. Device Scaling
- Model extensible to a wide range of transistors (NFET, TGFT, DGFT, FinFETs, GAA, planar FDSOI transistors):
- Necessary devices dimensions (criterion: SS > 15 mV/dec) vs. gate length for planar FDSOI, DGFTs, TGFTs, PGFTs and GAA transistors. Coloured areas: results obtained with the natural length [1,6].

4. Full characteristics
- Using a simplified expression for the strong inversion and interpolation functions for the moderate inversion:

\[ I_{ss} = \left( \frac{v_L}{V_F} \right)^{1/2} \left( \frac{V_D}{V_F} \right) \frac{V_D}{V_F} + \left( \frac{v_L}{V_F} \right)^{1/2} \left( \frac{V_D}{V_F} \right) \]

5. Conclusions
- Analytical model for the subthreshold current of NFET/TGFT/FinFET/DGFT/GAA/planar FDSOI transistors.
- Application to device scaling of Multiple-gate devices.
- Extension of the analytical model in strong and moderate inversion for short channel planar FDSOI and TGFT transistors.

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