Analytical Modelling of Short Channel Planar FDSOI and Triple-gateFET Transistors

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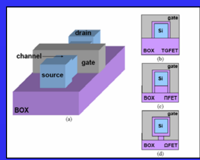
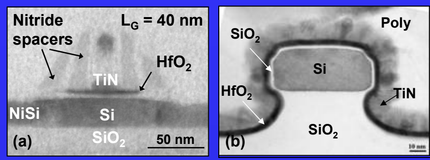
1. Context & motivations

- Triple-gate (TGFETs) devices [1,2]: better electrostatic control of the body
- During channel etch, the BOX can be overetched: ΠFETs [3], ΩFETs [4].
- This paper: definition of a short channel analytical model for TGFET/planar FDSOI transistors.



TGFET (a-b), ΠFET (c) and ΩFET (d) transistors.



Longitudinal (a) and transversal (b) cut of a ΩFET transistor.

2. Subthreshold Currents

. 3D solution of the Laplace's equation, using Fourier's series development [5]:

$$\varphi(x,y,z)=\varphi_{Top-gate(TG)}(x,y,z)+\varphi_{Back-gate(BG)}(x,y,z)+\varphi_{Lateral-gates(LG)}(x,y,z)+\varphi_{Source/Drain(SD)}(x,y,z)$$

$$\varphi_{TG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_C(m)F_C(n)\sin(\frac{m\pi x}{W})\sin(\frac{n\pi z}{L_G})\left[\cosh(\sqrt{(\frac{m}{W})^2+(\frac{n}{L_G})^2}\pi y)\Big/\cosh(\sqrt{(\frac{m}{W})^2+(\frac{n}{L_G})^2}\pi(H+t_{OV}))\right]$$

$$\varphi_{LG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_P(m)F_n(n)\sin(\frac{m\pi z}{L_G})\sin(\frac{(2n+1)\pi(H+t_{OV}-y)}{2(H+t_{OV})})\left[\frac{\sinh(\sqrt{(\frac{m}{L_G})^2+(\frac{2n+1}{2(H+t_{OV})})^2}\pi(W-x))+\sinh(\sqrt{(\frac{m}{L_G})^2+(\frac{2n+1}{2(H+t_{OV})})^2}\pi x)}{\sinh(\sqrt{(\frac{m}{L_G})^2+(\frac{2n+1}{2(H+t_{OV})})^2}\pi W)}\right]$$

$$\varphi_{SD}(x,y,z)=\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_P(m)F_n(n)\sin(\frac{m\pi x}{W})\sin(\frac{(2n+1)\pi(H+t_{OV}-y)}{2(H+t_{OV})})\left[\frac{V_S\sinh(\sqrt{(\frac{m}{W})^2+(\frac{2n+1}{2(H+t_{OV})})^2}\pi(L_G-z))+V_D\sinh(\sqrt{(\frac{m}{W})^2+(\frac{2n+1}{2(H+t_{OV})})^2}\pi z)}{\sinh(\sqrt{(\frac{m}{W})^2+(\frac{2n+1}{2(H+t_{OV})})^2}\pi L_G)}\right]$$

$$\varphi_{BG}(x,y,z)=\varphi_{S3}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_P(m)F_P(n)\sin(\frac{m\pi x}{W})\sin(\frac{n\pi z}{L_G})\left[\sinh(\sqrt{(\frac{m}{W})^2+(\frac{n}{L_G})^2}\pi(H+t_{OV}-y))\Big/\sinh(\sqrt{(\frac{m}{W})^2+(\frac{n}{L_G})^2}\pi(H+t_{OV}))\right]$$

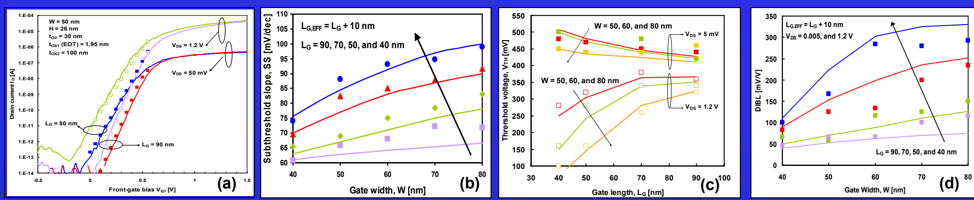
with:

$$\varphi_{S3}=(V_{G2}-V_{FB2})\Big/\left(1+\frac{\varepsilon_{Si}}{\varepsilon_{BOX}/(t_{OX2}-t_{OV})}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_P(m)F_P(n)\sin(\frac{m\pi}{2})\sin(\frac{n\pi}{2})\left[\sqrt{(\frac{m}{W})^2+(\frac{n}{L_G})^2}\pi\Big/\tanh(\sqrt{(\frac{m}{W})^2+(\frac{n}{L_G})^2}\pi(H+t_{OV}))\right]\right)$$

W being the fin width, H the fin height, L_G the gate length, t_{OV} the overetch depth, ε_{BOX} the BOX permittivity, ε_{Si} the silicon permittivity, V_{FB1} (resp. V_{FB2}) the front-gate (resp. back-gate) flat band voltage. The series coefficient F_p, F_n, and F_c are defined in the Appendix.

. 'Most leaky path' approximation and integration of the potential, subthreshold current expressed as:

$$I_{DS}=\frac{\mu q n_i V_T}{L_G}(1-e^{V_{DS}/V_t})WH\frac{2e^{\varphi(W/2,t_{OV},Z_C)/V_t}+e^{V_{G1}/V_t}}{3}$$

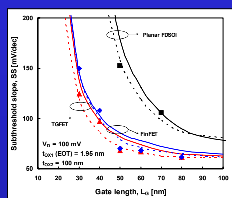


Comparison model/measurements: subthreshold currents (a), Subthrershold slope, Roll-off (c) and DIBL (d).

Correct description of the short channel subthreshold performance of ΠFET transistors

. Simplifying the subthreshold current, approximated subthreshold slope expressed as:

$$SS(L_G,W,H)=(\frac{\partial\ln(I_D)}{\partial V_G})^{-1}=V_T\ln(10)\frac{1}{\left[\sum_{m=1}^{N}\sum_{n=1}^{N}\frac{F_C(m)F_C(n)\sin(\frac{m\pi}{2})\sin(\frac{n\pi Z_C}{2})}{\cosh(\sqrt{(\frac{m}{W})^2+(\frac{n}{L_G})^2}\pi H)}+\sum_{m=1}^{N}\sum_{n=0}^{N}F_P(m)F_N(n)\sin(\frac{m\pi Z_C}{L})(-1)^n\frac{2\sinh(\sqrt{(\frac{m}{L_G})^2+(\frac{2n+1}{2H})^2}\pi\frac{W}{2})}{\sinh(\sqrt{(\frac{m}{L_G})^2+(\frac{2n+1}{2H})^2}\pi W)}\right]}$$



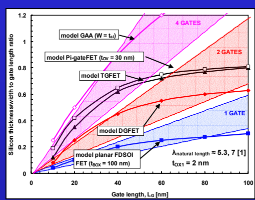
Comparison between subthreshold slope obtained with the analytical solution (dashed lines), the approximated formula (solid lines) and numerical simulations (TGFET – triangles , FinFET –diamonds, Planar FDSOI devices - squares).

Pseudo-compact (N~5) of the subthreshold slope with a 20% precision

3. Device Scaling

. Model extensible to a wide range of transistors (ΠFET, TGFET, DGFET, FinFETs, GAA, planar FDSOI transistors):

Structure	Features
Pi-gateFET (core structure)	$t_{OV}\neq 0$
TGFET	$t_{OV}\approx 0$
Planar FDSOI	$t_{OV}\approx 0$, W>>H
DGFET/FinFET	$t_{OV}\approx 0$, W<<H
Gate All Around	$t_{OV}\approx 0$, $\varphi_{S3}=V_{G1}-V_{FB1}$



Necessary devices dimensions (criterion: SS = 75 mV/dec) vs. gate length for planar FDSOI, DGFETs, TGFETs, PiFETs and GAA transitors. Coloured areas: results obtained with the natural length [1,6].

Correct description of the short channel subthreshold performance of ΠFET transistors

4. Full characteristics

. Using a simplified expression for the strong inversion and interpolation functions for the moderate inversion:

➢ Total drain current expressed as:

$$I_{D,TOT}=\left(\frac{I_{D,SI}^{1/\eta_1}}{1+\left(\frac{I_{D,SI}}{I_{D,WI}}\right)^{1/\eta_1}}\right)^{\eta_1}$$

with:

Weak inversion:

$$I_{D,WI}=\frac{\mu q n_i V_T}{L_G}(1-e^{V_{DS}/V_t})WH\frac{2e^{\varphi(W/2,t_{OV},Z_C)/V_t}+e^{V_{G1}/V_t}}{3}$$

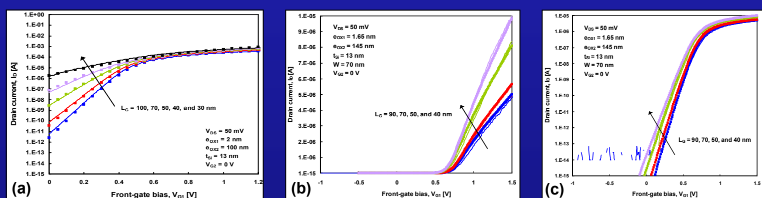
Strong inversion:

$$I_{D,SI}=\mu C_{OX1}\frac{W+2H}{L_G}V_{DS}\eta_2\ln\left[1+\exp(\frac{V_{G1}-V_{TH}-\frac{V_{DS}}{2}}{\eta_2})\right]$$

With η_1, η_2 two fitting parameters related to the moderate inversion regime.

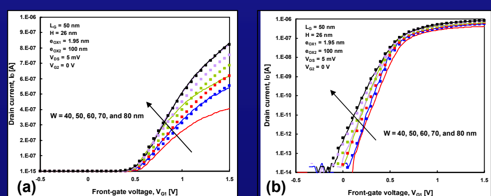
Analytical model valid in weak, moderate and strong inversion

. Planar Fully Depleted SOI transistors (t_{Si} = 13 nm):



Comparison model/simulations (a) and model/measurements (b-c) in the linear regime for planar FDSOI devices.

. TGFET transistors (H = 26 nm, W = 40 to 80 nm):



Comparison model/measurements (a-b) in the linear regime for TGFET devices.

5. Conclusions

- Analytical model for the subthreshold current of ΠFET/TGFET/FinFET/DGFET/GAA/planar FDSOI transistors.
- Application to device scaling of Multiple-gate devices.
- Extension of the analytical model in strong and moderate inversion for short channel planar FDSOI and TGFET transistors.

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