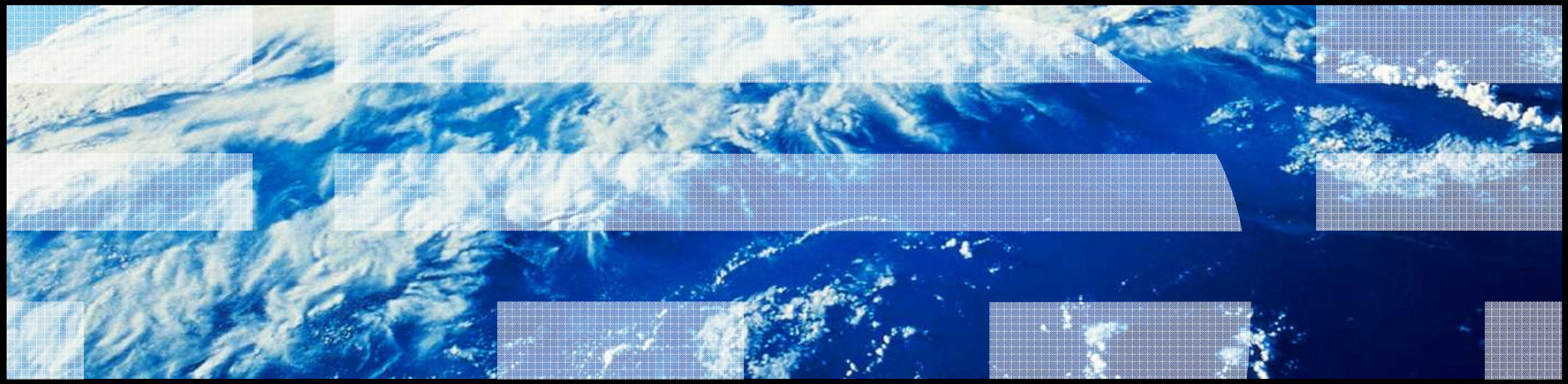
Josef Watts IBM, Compact Model Council

17 September 2010

Modeling Standardization: Enabling the worldwide design community



Outline

Why compact model standardization?

Model selection

Model standardization and QA

Continuous improvement

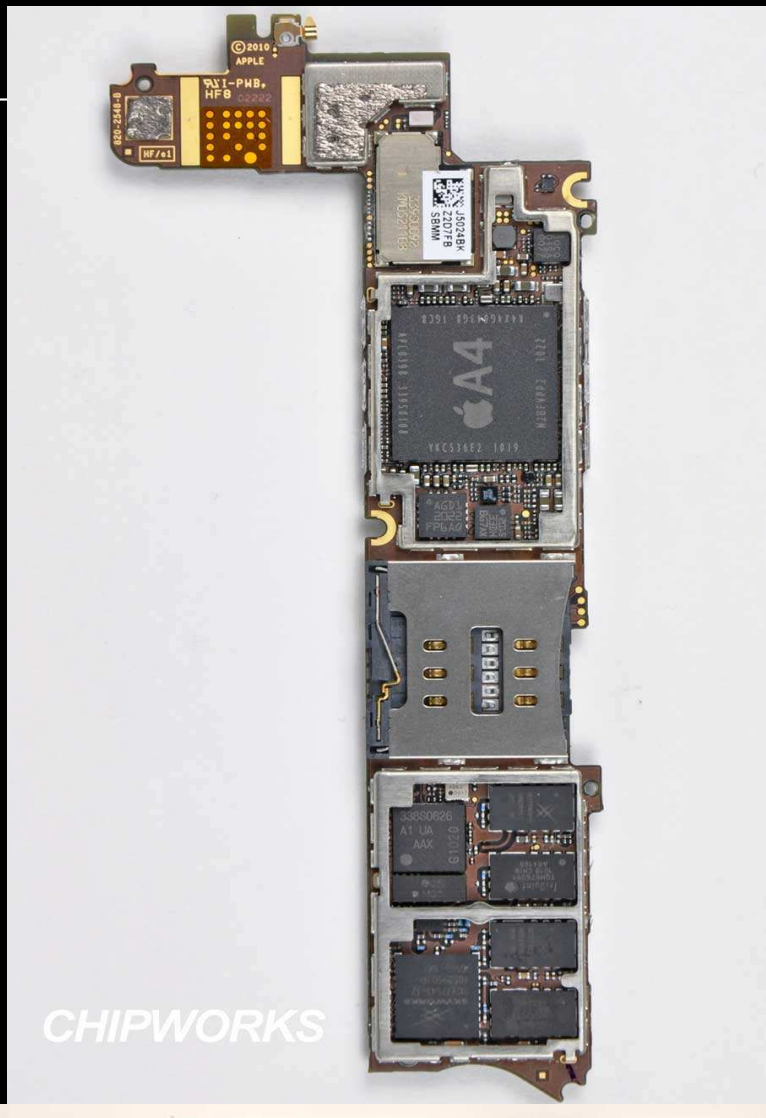
Verilog-A

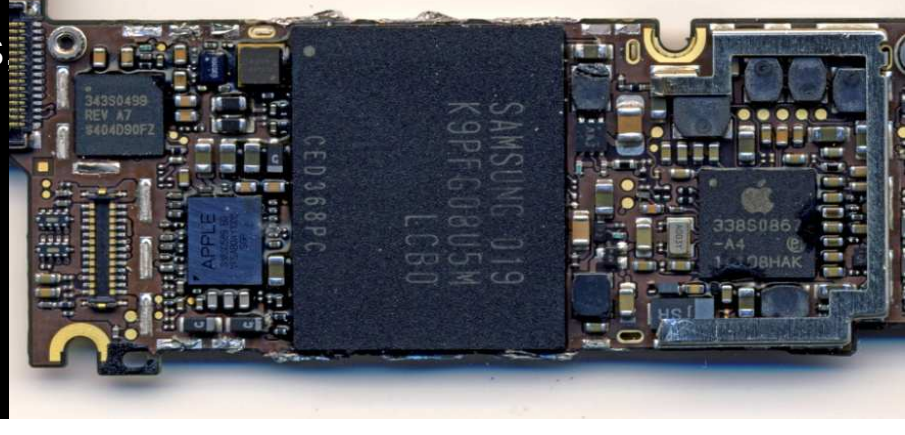
Other Standards

Summary

Look at the Apple I-phone for a view of the shape of our industry

- Most chips are *not* designed by Apple
- Chips from a dozen different companies
- Apple designed chips are not fabbed by Apple
- Why?
  - Chip fabs are very expensive to build
  - And to run
  - There are huge economies of scale
- Most designers use commercial (not inhouse) design tools
- Designers, EDA vendors and fabs need common models to communicate
- The CMC was formed in 1995 as a collaboration of foundries, fabless companies and EDA vendors





Source: Chipworks.com webpage

The CMC Mission

- **Charter:** To promote the international, nonexclusive standardization of compact model formulations and the model interfaces.
- **Vision:** Standardized compact models for all major technologies so that customer communication and efficiency can be enhanced. Standard interfaces so that models can be tested faster and implemented easier. Better compact models for the latest technologies, allowing leading edge design development cycles to shorten.
- **Strategy:** Examine, promote and standardize compact modeling efforts based upon business needs. Encourage developers to dwell on current and near-term problems that will advance compact modeling. Provide industry resources for monitoring/mentoring compact model development. Provide a standardization process to the compact model developers.

Source: Chipworks.com webpage

What the CMC does

- Standardize models existing transistor models
  - Competitive selection
  - Rigorous testing
  - Version Control
  - Continuous improvement
  - CMC funding for university support
- Create standard models for passives
  - Created and maintained by industry volunteers
- Standard modeling interfaces
  - Verilog-A
  - TMI-2 API
  - Proximity effect instance parameters
  - Standard Spice Language
  - Statistical modeling standard

Source: Chipworks.com webpage

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Select device types to support with standard models

- Is there a need for a (new) standard model?
- Is there potential financial support for a standard model?
- Do models of sufficient quality exist?
- Current CMC Standards
  - 1996 BSIM3

CMOS logic design, .25l

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Short channel MOSFET

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SOI MOSFET for CMOS logic

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  - 2004 MEXTRAM
  - 2004 HICUM

Bipolar, include SiGe HBT for RF

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  - 2004 MEXTRAM
  - 2004 HICUM
  - 2005 R2_CMC

Poly & Metal resistors
(2 terminal)

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  - 2005 R2_CMC
  - 2006 PSP

MOSFET model for analog especially operating thru Vds=0

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  - 2006 PSP
  - 2007 HiSIM_HV

High voltage MOSFET such as LDMOS

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  - 2005 R2_CMC
  - 2006 PSP
  - 2007 HiSIM_HV
  - 2007 R3_CMC

Defused Resistor
(3 terminal)

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  - 2005 R2_CMC
  - 2006 PSP
  - 2007 HiSIM_HV
  - 2007 R3_CMC
  - 2008 MOSVAR

MOS Varactor

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  - 2005 R2_CMC
  - 2006 PSP
  - 2007 HiSIM_HV
  - 2007 R3_CMC
  - 2008 MOSVAR
  - 2009 Diode_CMC

Designed Diode

CMC is currently working on standards for

- Partially depleted SOI MOSFET for analog application including Vds=0
- Dynamic depletion SOI MOSFET
- Multigate MOSFET
- Fully Depleted (ultra-thin) MOSFET
- GaN HEMT

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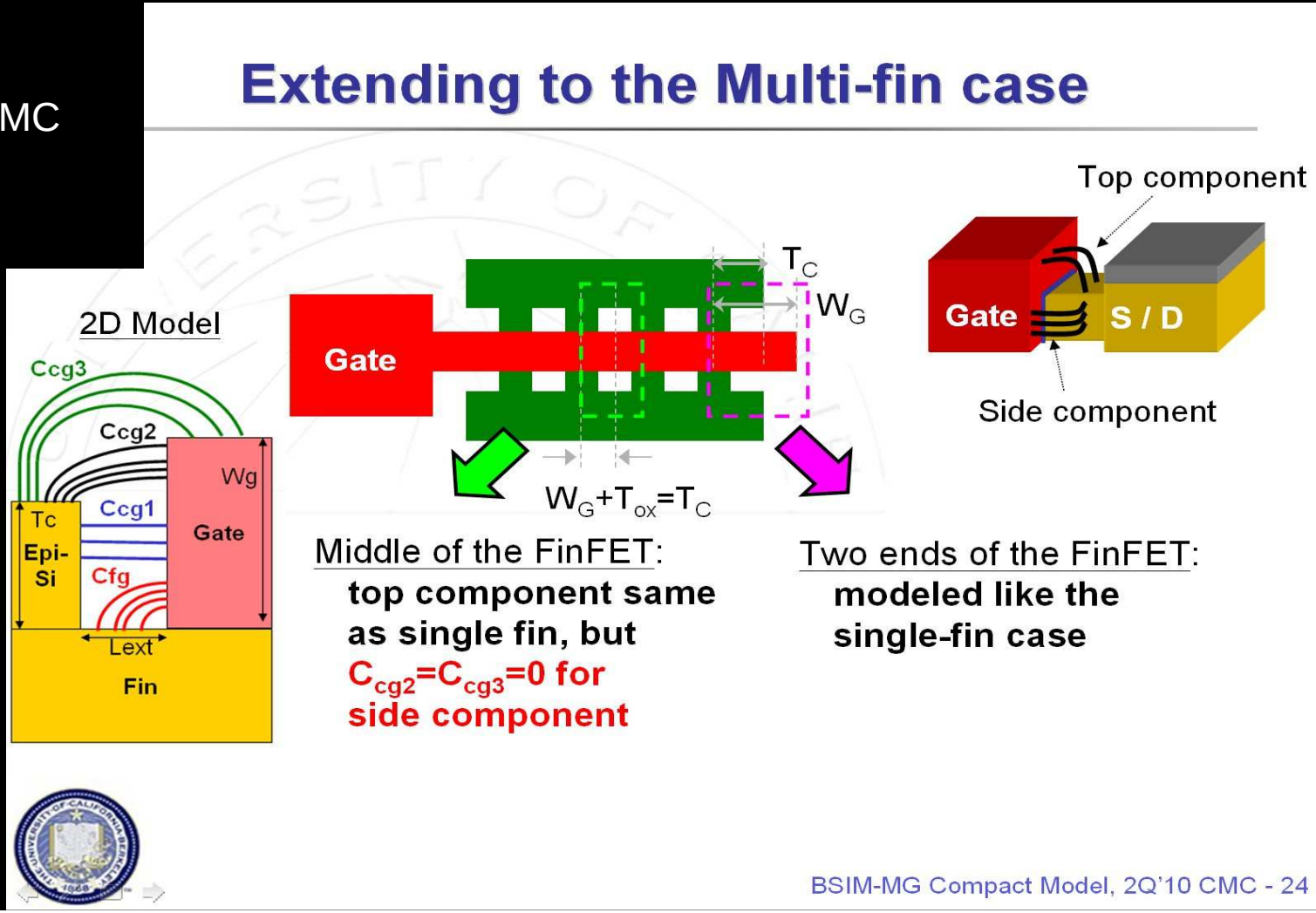
Summary

Four Phase Standardization Process

- Phase I—Search and review of available models
- Phase II—Developer and sponsor(s) fit to data and complete physicality tests
- Phase III—CMC test models, using model cards from Phase II and/or own data
- Models passing Phase III will eventually be CMC standards
- Phase IV—Models readied for release

Phase I—Search and review of available models

- Model must appear able to meet all requirements within a reasonable time
  - Including support and IP requirements
- Model must attract at least 1 CMC member as a sponsor



Phase II—Developer and sponsor fit data and complete physicality tests

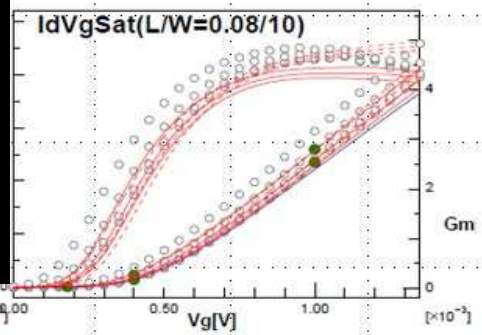
- Model must fit the data adequately
- Model must pass physicality tests
- Phase II produces “Frozen code & Model cards”

Overlay : PMOS IV-Sweep 0315 vs 0202

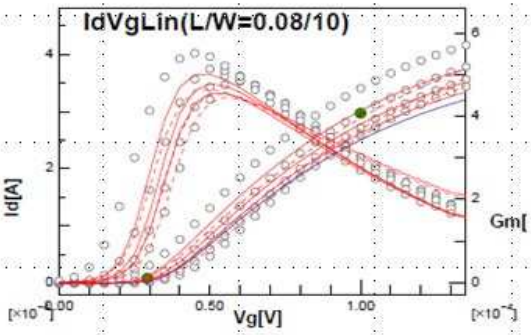
FUJITSU

W/L=10um/0.08um *Short Wide*

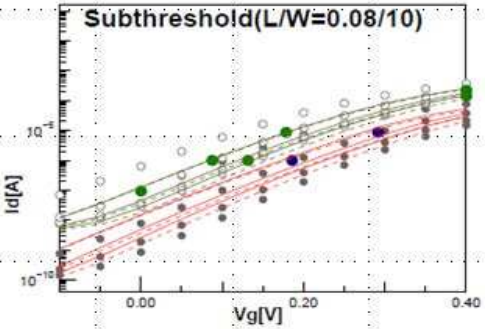
Id-Vg-Vb@Vd=1V



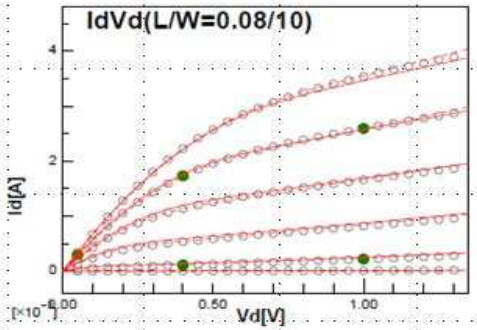
Id-Vg-Vb@Vd=0.05V



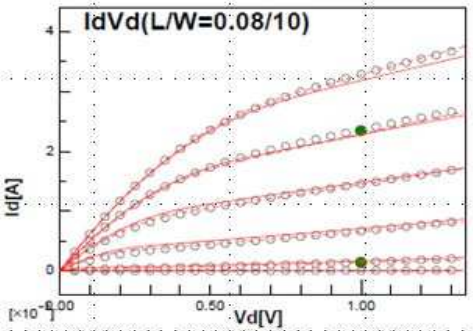
Log(Id)-Vg-Vb@Vd=1V,0.05V



Id-Vd-Vg@Vb=0V



Id-Vd-Vg@Vb=-0.75V



Phase III—CMC test models, using model cards from Phase II and/or own data

- Model must be judged by CMC members to be significant improvement over what is publically available
- Ideally one but sometimes two models
- Models passing Phase III will eventually be CMC standards

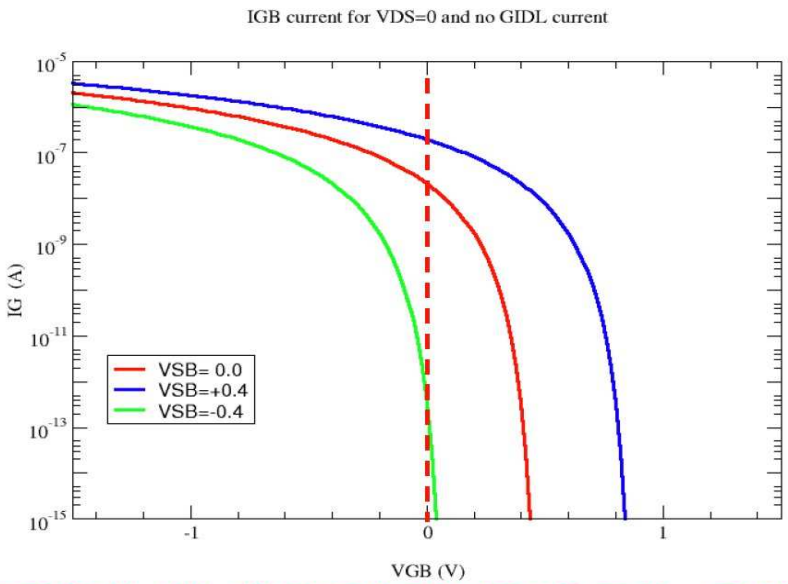
PSP runtime

Comparison of Global CPU time: Bsim4.5, PSP 102.1/Juncap, PSP102.1/Juncap express

Circuit	Number of transistors	BSIM 4.5		PSP 102.1 JUNCAP		PSP 102.1 JUNCAP Express	
		CPU Time (s)	Ratio	CPU time	Ratio	CPU time	Ratio
Comprt	17	3.88	1	6.37	1.641752577	5.04	1.298969072
Fadd32	288	4.4	1	6.67	1.515909091	4.7	1.068181818
Inv	10	4.46	1	7.05	1.580717489	5.51	1.235426009
Nand1	44	2.44	1	2.82	1.155737705	2.29	0.93852459
Nand3	132	6.06	1	5.94	0.98019802	5.16	0.851485149
Nor1	44	2.6	1	2.93	1.126923077	2.19	0.842307692
Nor3	132	20.87	1	18.58	0.890273119	15.18	0.727359847
Ring3	66	2.82	1	3.05	1.081560284	2.44	0.865248227
Ring_rc	42	10.31	1	10.18	0.987390883	8.46	0.820562561
Ro19	38	5.65	1	7.98	1.412389381	6.47	1.145132743
Sram	1008	301.02	1	366.42	1.217261312	290.71	0.965749784
Ring	36	12.25	1	15.45	1.26122449	11.19	0.913469388
Average			1		1.237611452		0.972701407

Convention: Green <1.1< Orange < 1.3< Red

$I_{gs}=0$
$I_{gd}=0$
$I_{gate,s}=0$
$I_{gate,d}=0$
only I_{gb}



should be zero for $V_{GB}=V_{SB}=0$; should only depend on V_{GB}, not V_{SB}

Phase IV—Models readied for release

- Fix problems found in phase II & III
- Model must fully meet requirement
- 2/3 yes vote
- Negative comments resolved (Resolved means)
  - explained to the satisfaction of the commenter
  - Or Fixed
  - Or Set aside by the chairman
- If “substantial” fixing is require a new ballot will be required

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Verilog-A

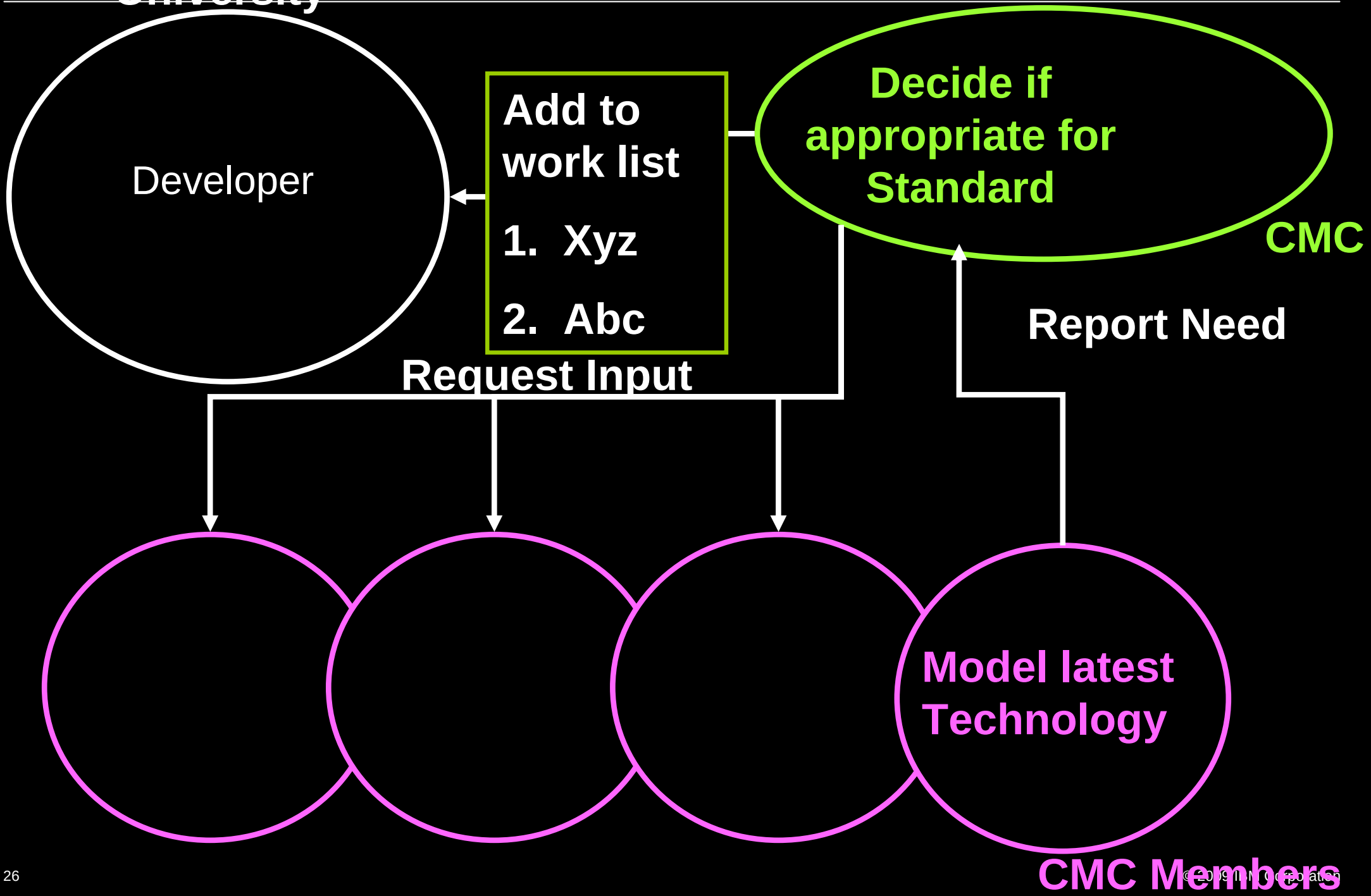
Other modelling standards

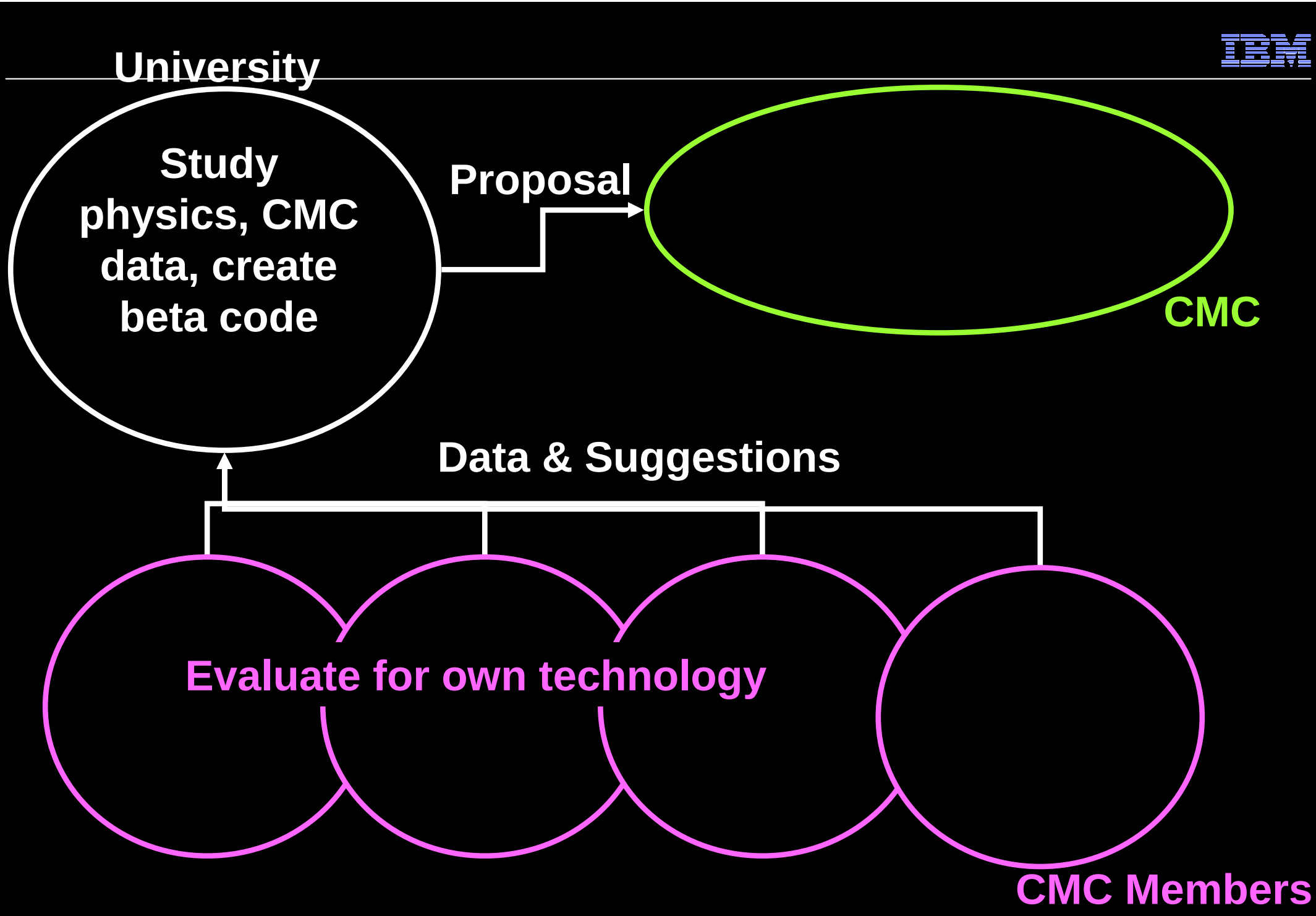
Summary

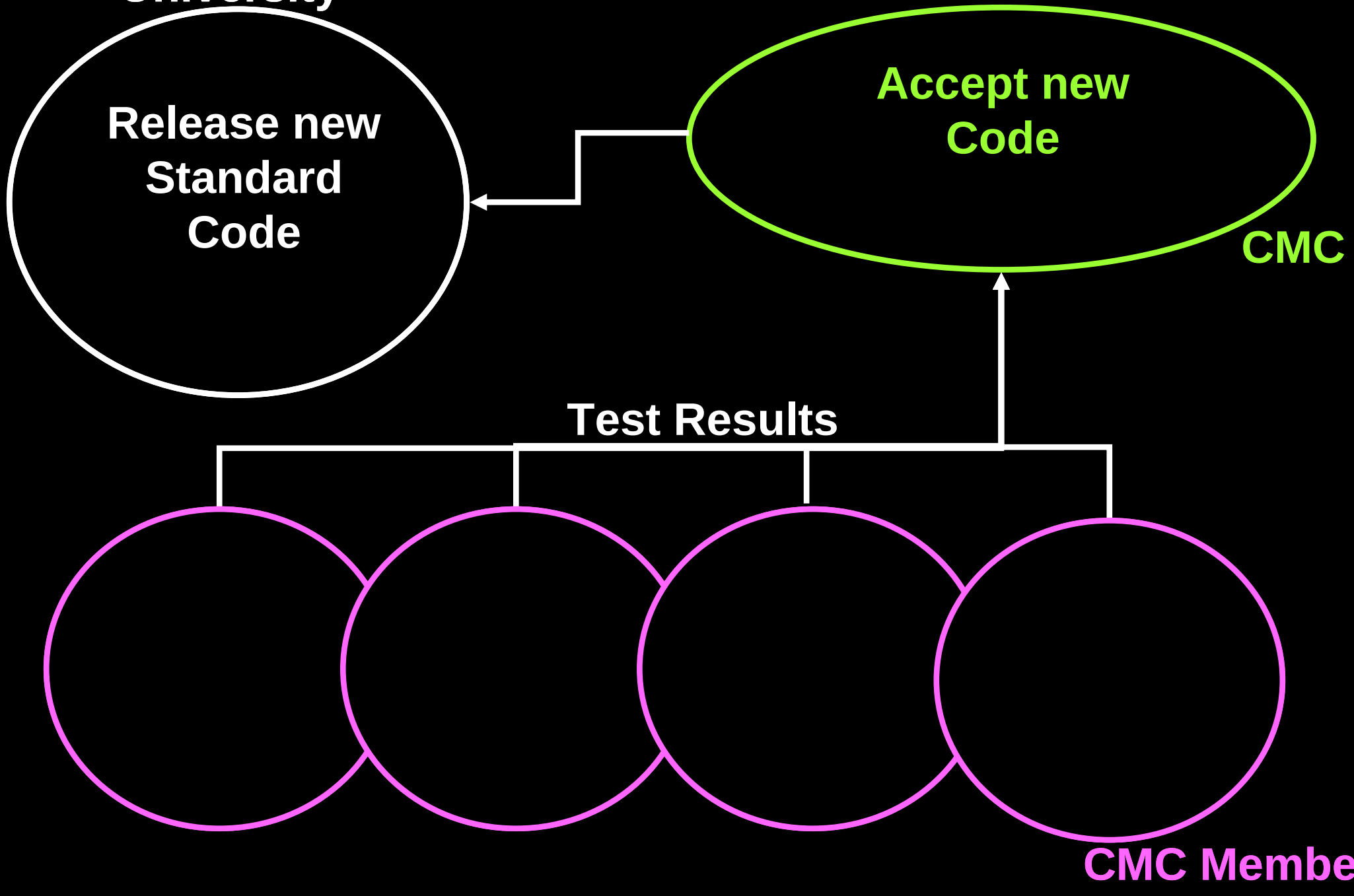
CMC models do not remain static

- Most enhancements are requested by members but they can also come from the developer
- CMC decides which enhancements they want to pursue
- CMC members test enhancements before they are released as a standard

University







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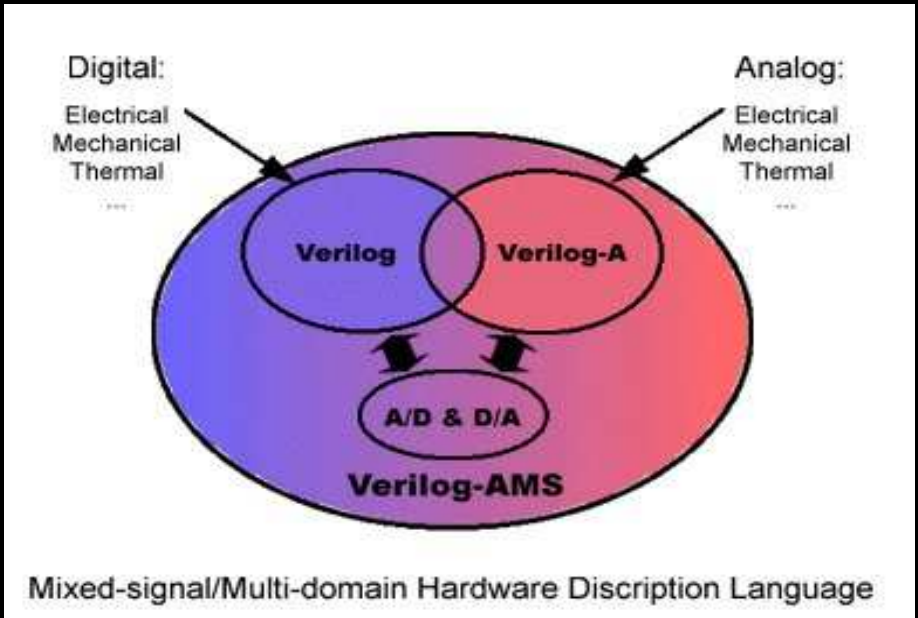
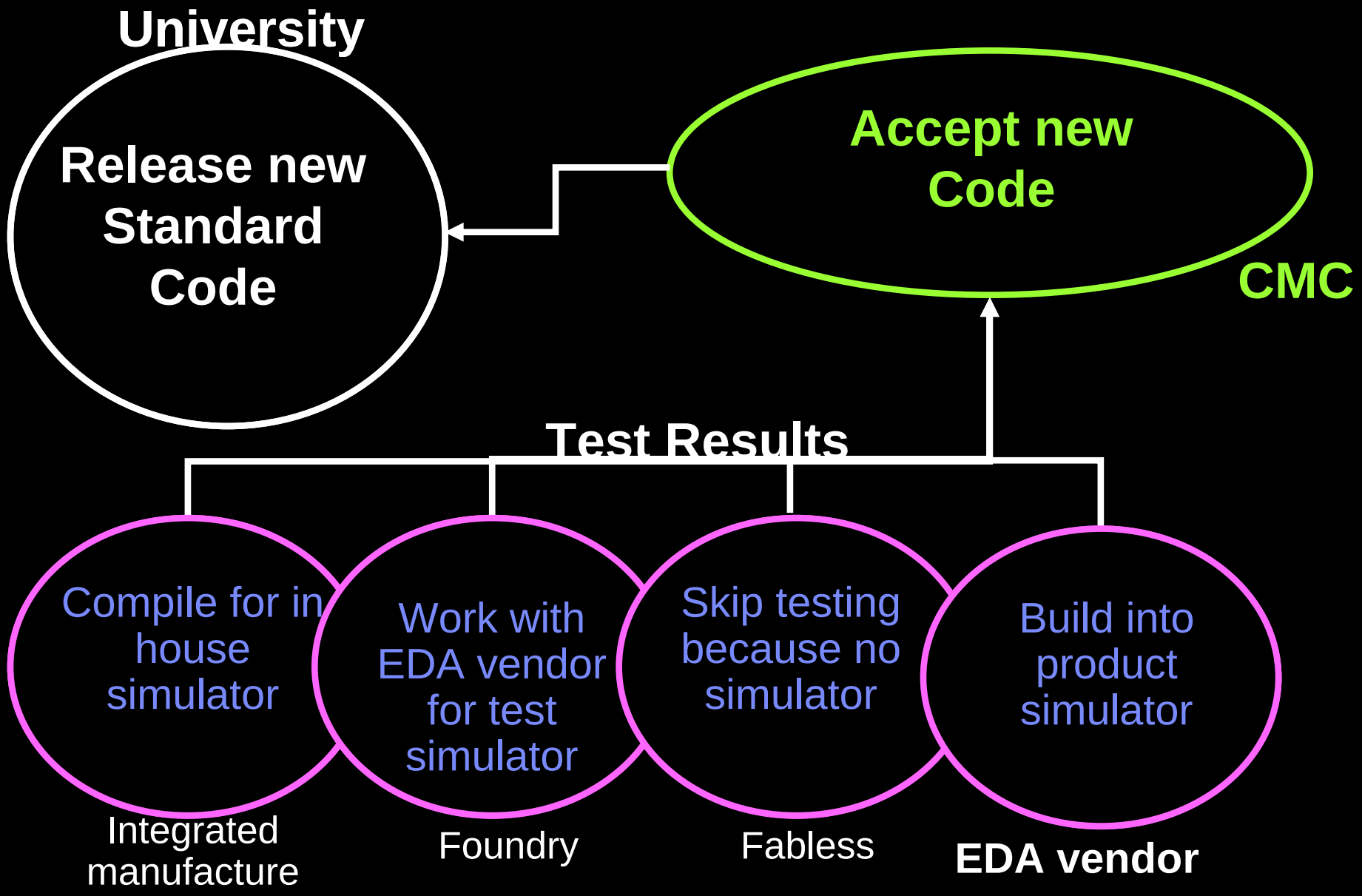
What & Why of Verilog-A for compact models

- Verilog-A is a part of verilog-AMS, a high level description language for analog and mixed signal circuits
- For standard compact models it has two compelling advantages
  - All simulators now support Verilog-A so collaborative model development and testing is simplified
  - All the derivatives are created automatically so there are no derivative errors in the code

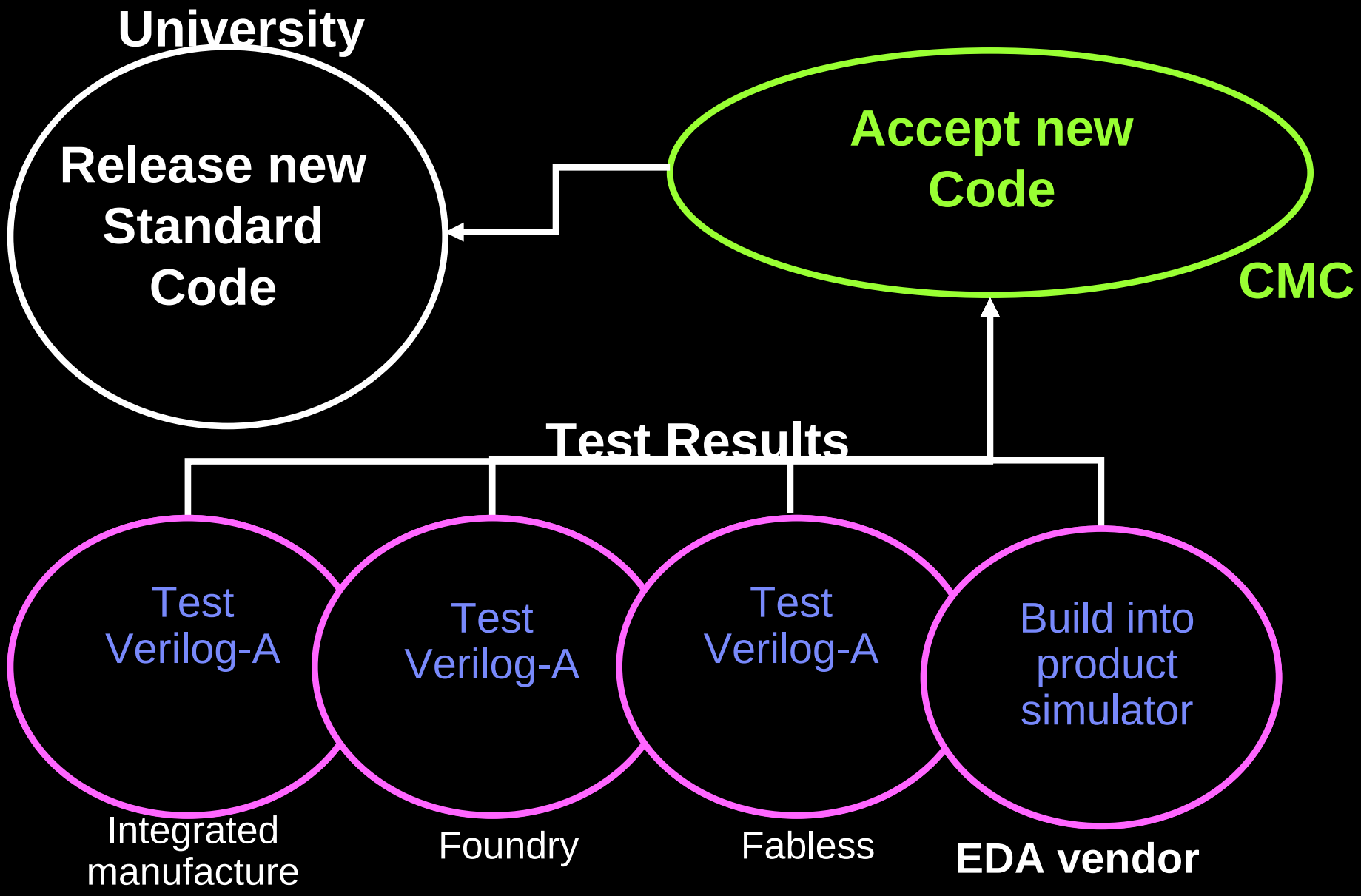


From the Accellera group website

Collaborative model development



Collaborative model development



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Standard Spice Language

- Defining a standard netlist and model file language
- List of 35 requirements was collected from CMC membership
- CurrentlyDrafting a language document
- Goal is to incorporate functionality of existing languages in a standard way (unless it is not a good idea)

Some features

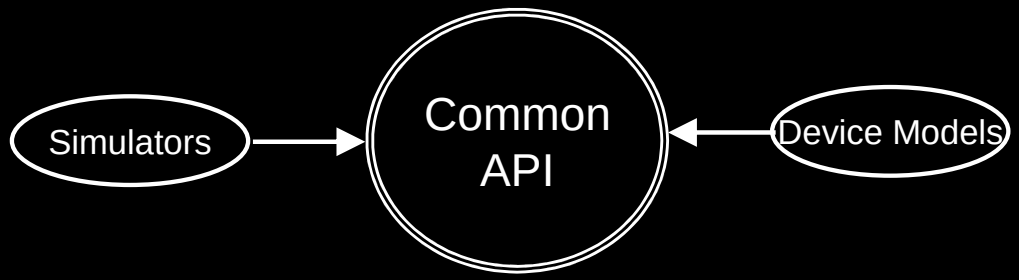
- Based on Berkeley-Spectre language
- Formal grammar
- Case-sensitive
- No positional arguments (except terminals)
- No key letters to identify components
- Conditional instantiation
- Formally defined hierarchy and scoping rules
- Method to combine different design kits in the same netlist
- Support for statistical variation
- Should play together well with Verilog A

Statistical Modeling Recommended Practice

- Define physical variation sources and their significance (MOS)
- Deliverables: Categorize sources & physical effects per category to be modeled.

- Modeling the different variation sources
- Deliverables: Standardize the communication of the different variability sources.

Common Model-Simulator API



- Allows for fast simulation of extra physical effects through compiled C code

- A common API makes it easier to interface to CMC standard models.
- One API to code and support … instead of multiple API's
- model extensions much easier to implement
- Future enhancement to support Aging simulations

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- The CMC enables the fabless—foundry semiconductor business model by
- Providing high quality device models
- Providing a forum and mechanism to keep them current to industry needs
- Standardizing model interfaces and usage

- The CMC is a member driven organization open to any company in the semiconductor business