



MOS-AK Workshop, Seville, Spain, Sep.17th, 2010

■ Progress in Applying
On-Wafer Calibration Techniques
for Advanced High-Speed
Silicon Technologies

Andrej Rumiantsev^{1), 3)}, Franck Pourchon²⁾

1) Cascade Microtech
Dresden GmbH, Suss-
Strasse, 1, D-01561
Sacka, Germany

2) STMicroelectronics,
850 rue Jean Monnet, F-38926
Crolles, France.

3) Dresden University of
Technology,
CEDIC, D-01062 Dresden,
Germany

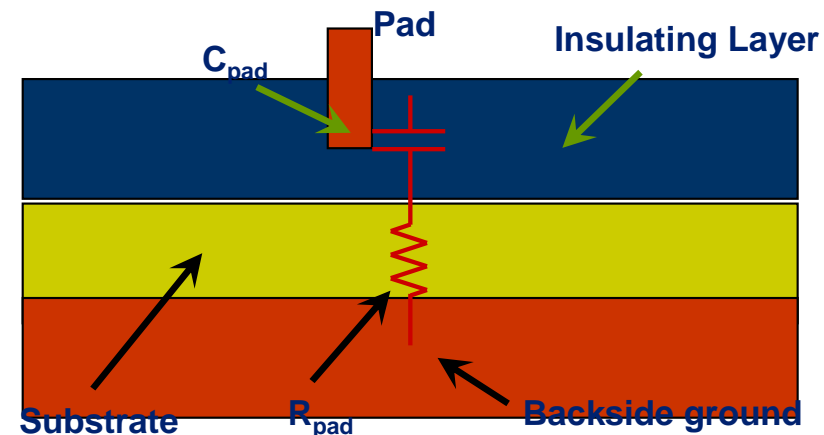
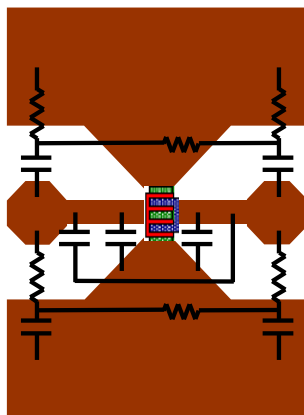


■ Outline

- Motivation
- On-Wafer Calibration
- Design of Calibration Standards
- Comparison Results
- Conclusion

■ Transistor Measurement Challenges

- A transistor cannot be contacted (probed) directly:
 - Contact pads and interconnects are required
- Increase of measurement and operation frequency:
 - Impact of contact pads parasitics significantly increases

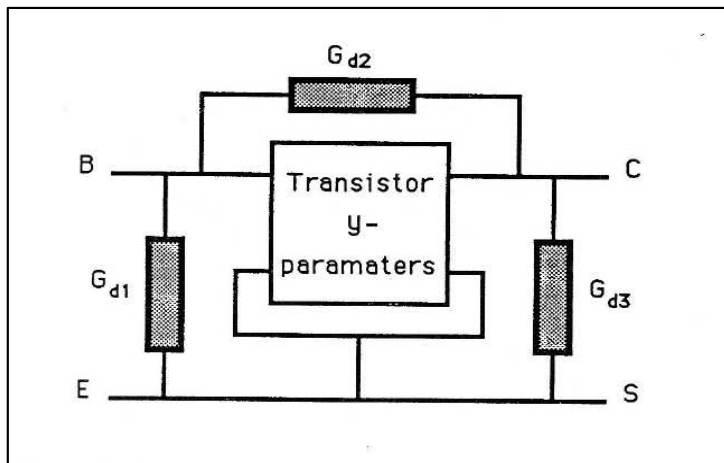


How to get rid of parasitics?

Conventional Method: Pad De-Embedding

- Complexity increases with an increase of frequency

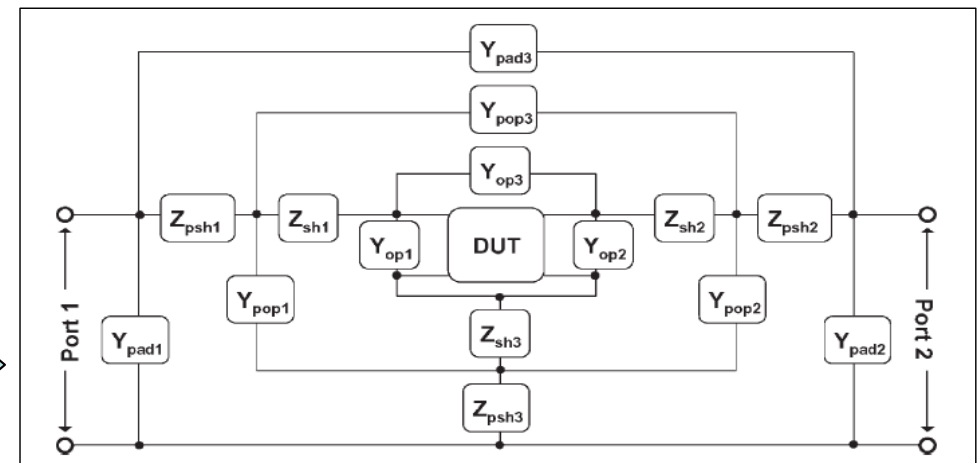
One-Step (few GHz)



Frequency increase



Five-Steps (<50GHz)



Alternative methods are required

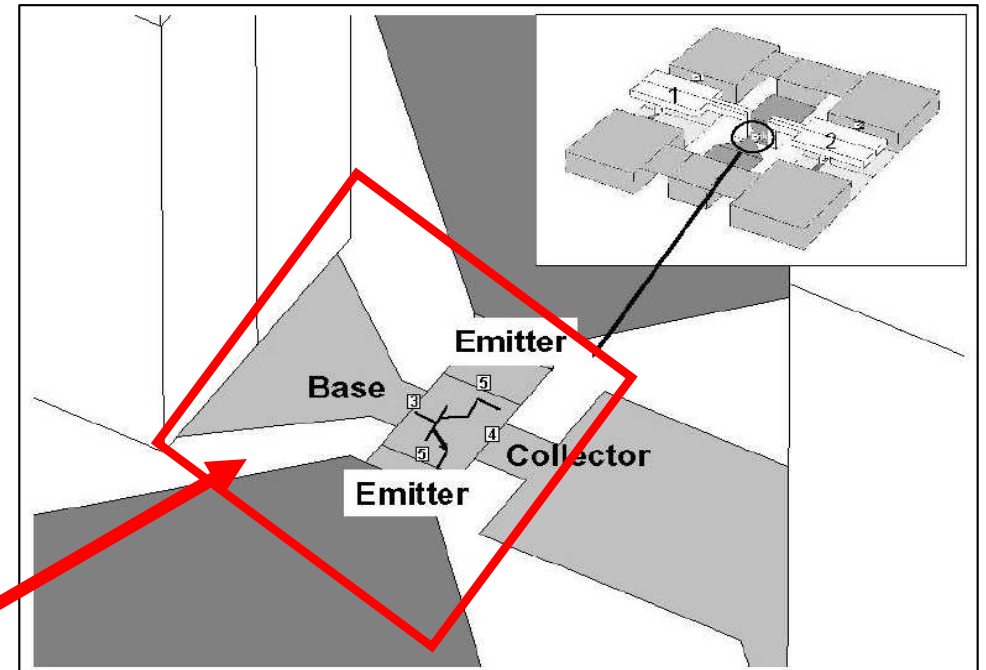
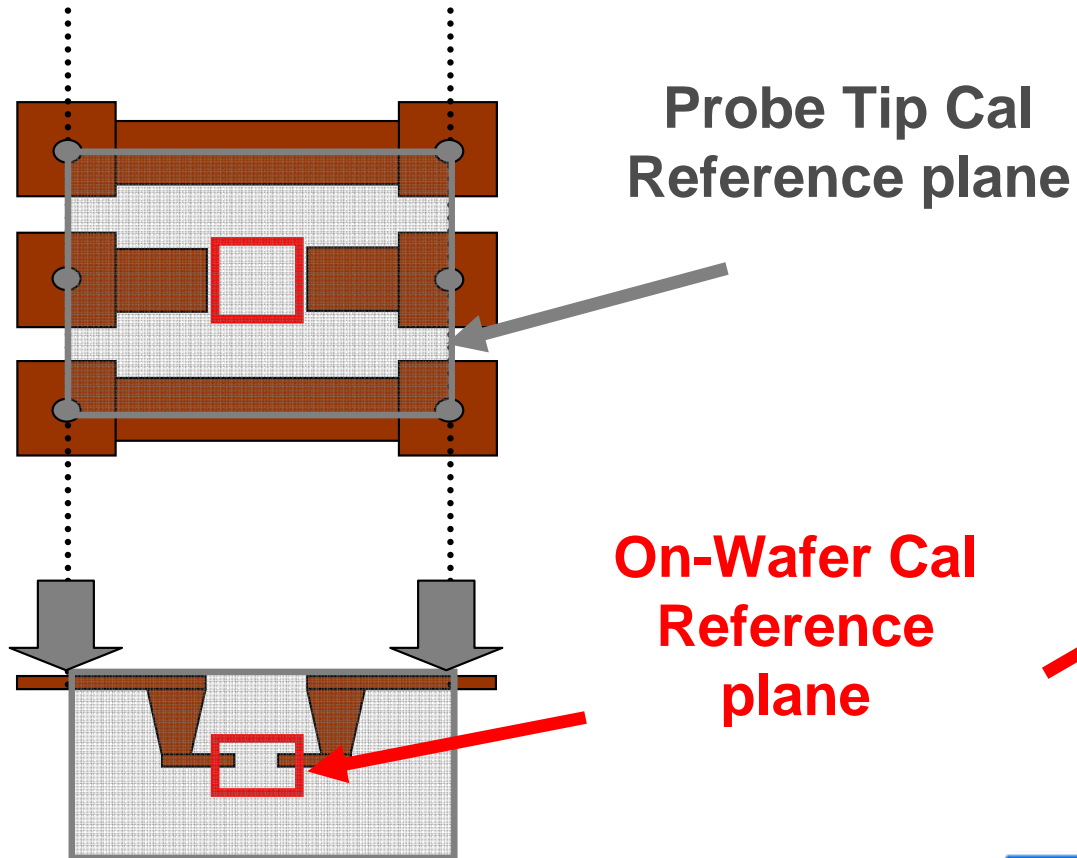
I. M. Kang, S.-J. Jung, T.-H. Choi, J.-H. Jung, C. Chung, H.-S. Kim, H. Oh, H. W. Lee, G. Jo, Y.-K. Kim, H.-G. Kim, and K.-M. Choi, "Five-step (Pad-Pad Short-Pad Open-Short-Open) de-embedding method and its verification," Electron Device Letters, IEEE, vol. 30, pp. 398-400, 2009.

■ Outline

- Motivation
- On-Wafer Calibration
- Design of Calibration Standards
- Comparison Results
- Conclusion

On-Wafer Calibration Goal

- To move the measurement reference plane close to the DUT terminals in just one step



Picture: R. Groves, BCTM, 2006

■ Suitable Calibration Methods

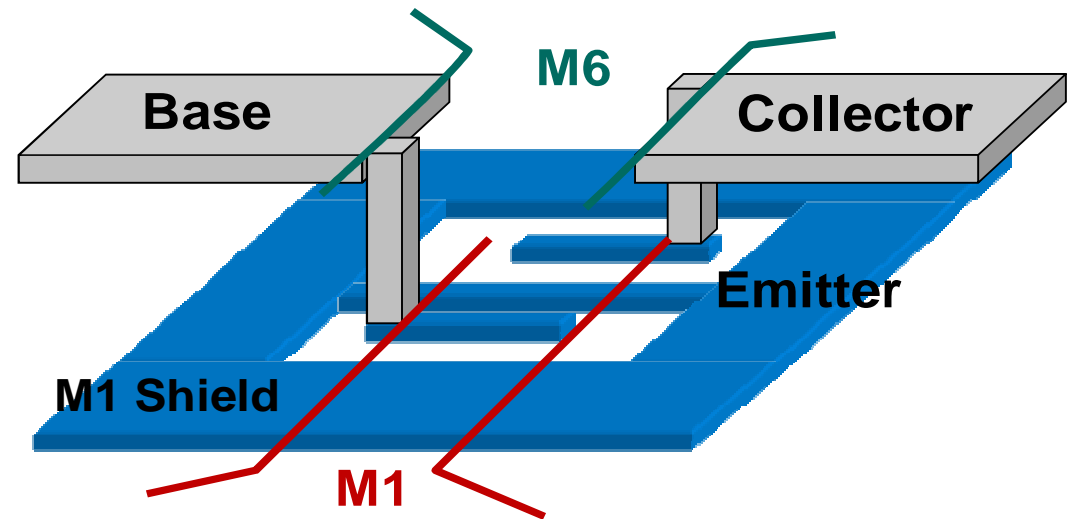
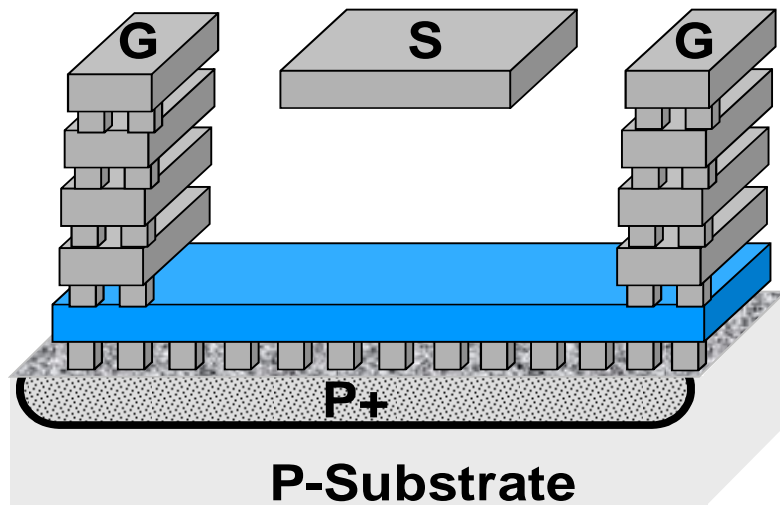
- Multiline TRL:
 - Developed at NIST in early 90s
 - Original application: semi-insulating wafers (GaAs)
 - End of 90s: application techniques for Si
- LRM+:
 - First application: SiGe:C
 - Comparison vs. multiline TRL: GaAs, bulk Si

■ Outline

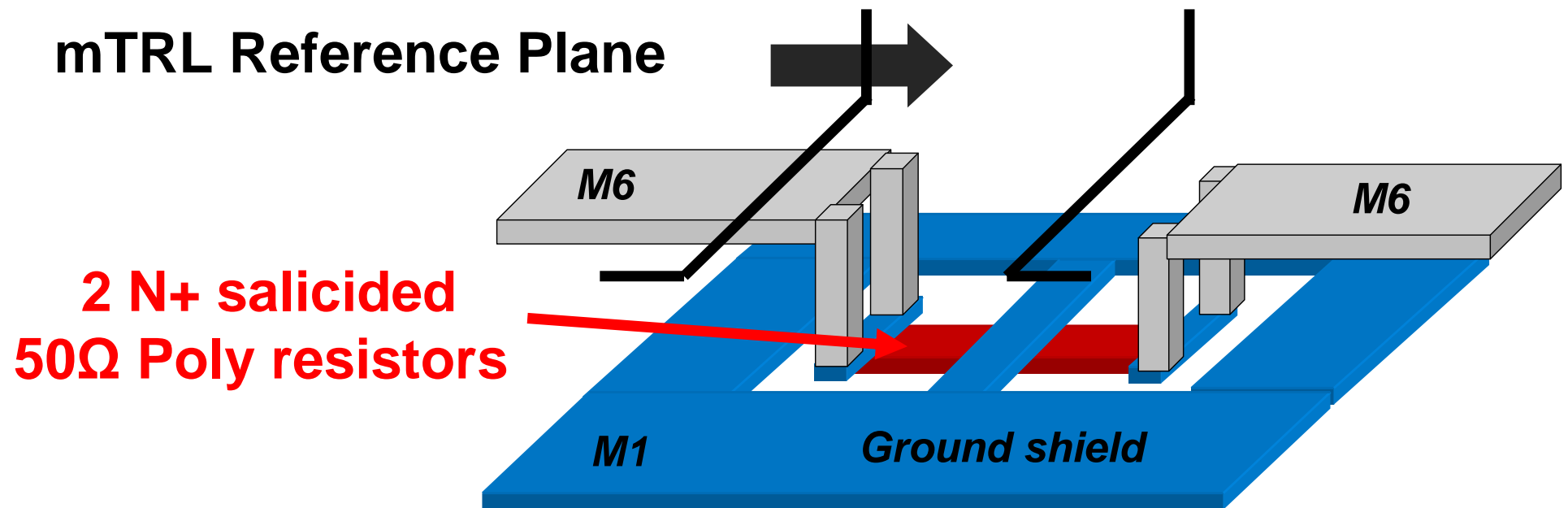
- Motivation
- On-Wafer Calibration
- Design of Calibration Standards
- Comparison Results
- Conclusion

■ Design of Calibration Standards

- Calibration reference plane tradeoff:
 - As close as possible to the DUT terminals
 - Locate standards as far as possible from Si (top metal)



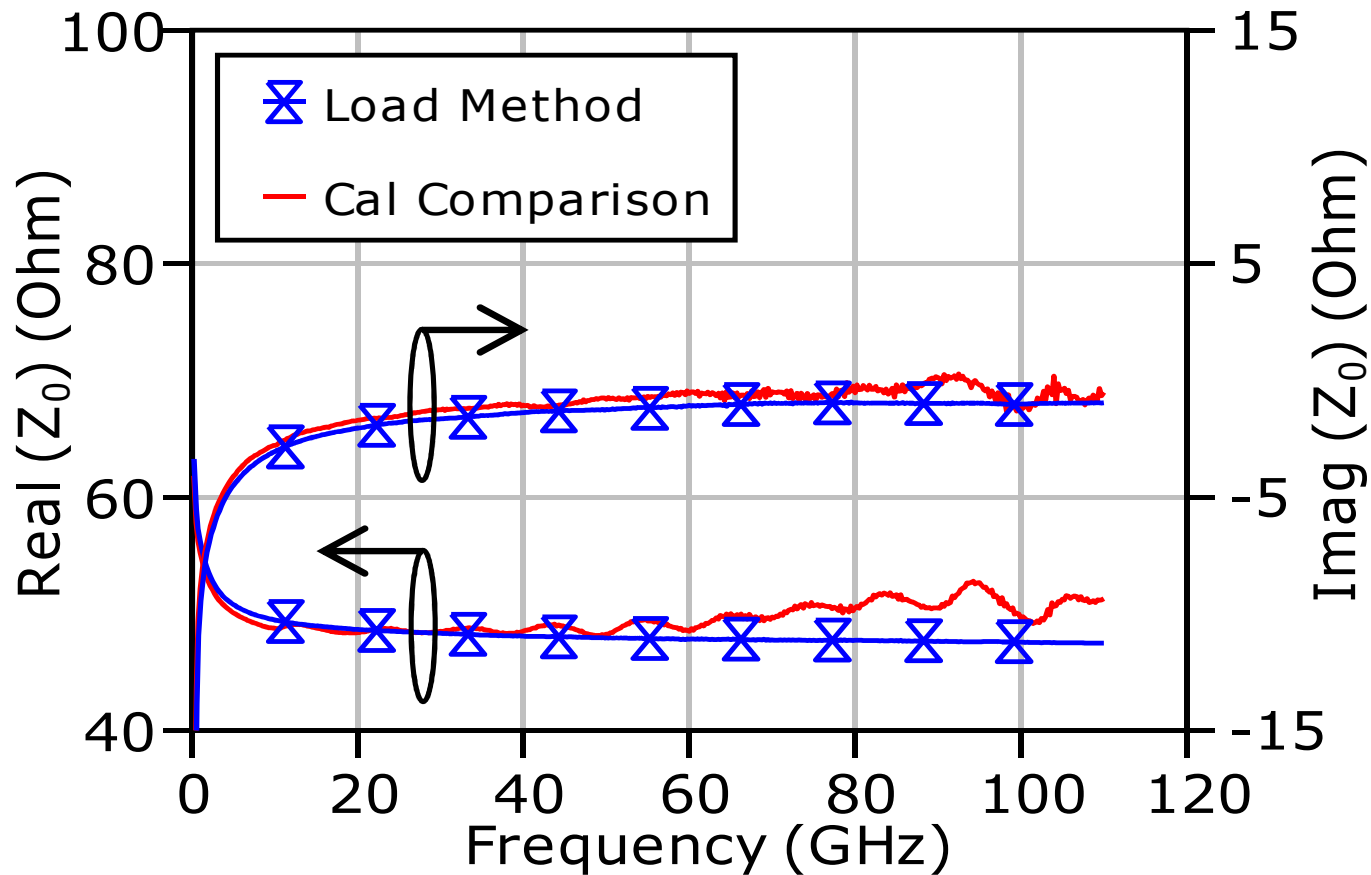
■ Design of Calibration Standards: Load



■ Characteristic Impedance of CPW

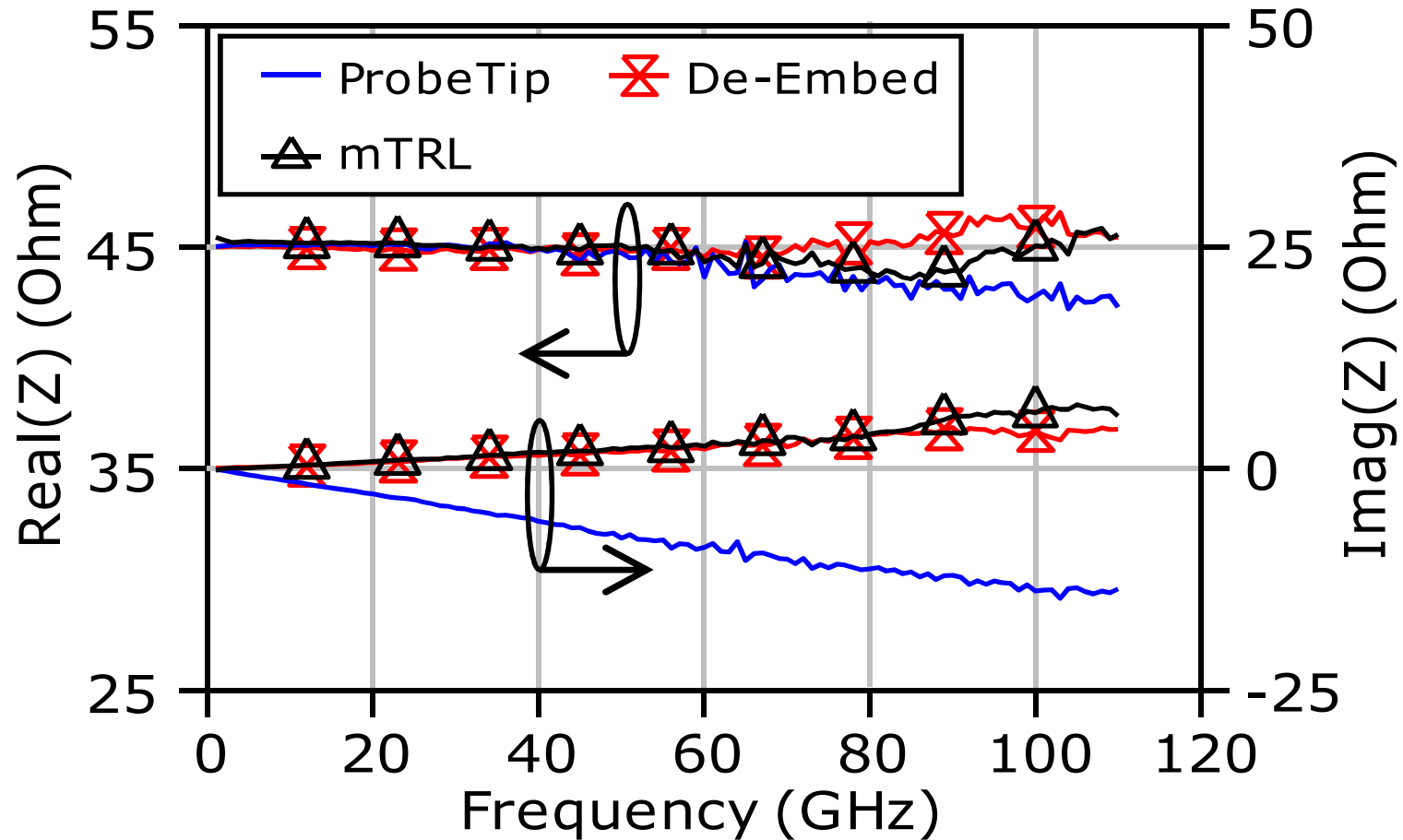
- Lumped Load Method:
 - Requires resistor (Load) embedded in the CPW launch
 - Load resistance R can easily be measured
 - Difficulties:
 - Impact of Load reactance can decrease accuracy
- Calibration Comparison Method:
 - Requires initial reference calibration (probe tip, on ISS)
 - Z_0 of the test line is extracted from the second-tier cal
 - Difficulties:
 - Accurate reference calibration at mm-wave frequencies
 - Impact of the Si line launch can decrease accuracy

Standards: Measurement of Line Z_0



Lumped load method provided sufficient accuracy

Standards: Measurement of Load Impedance



Two-step de-embedding provided comparable results

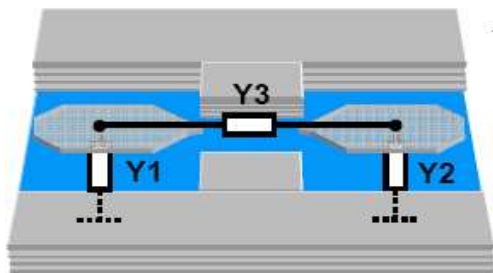
■ Outline

- Motivation
- On-Wafer Calibration
- Design of Calibration Standards
- Comparison Results
- Conclusion

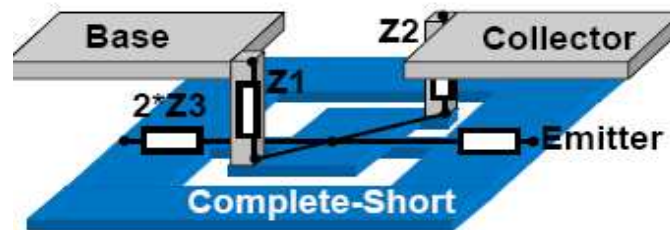
■ Calibration Verification Results

- Four calibration conditions:
 - Probe Tip
 - Probe Tip + De-embedding (conventional)
 - On-wafer mTRL, reference plane M6
 - On-wafer mTRL, reference plane M1
- Three elements: DUT Open, DUT Short, DUT:

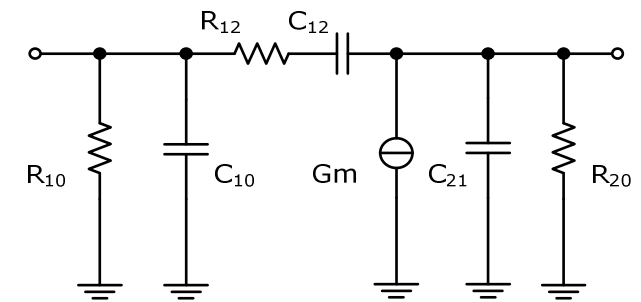
DUT Open



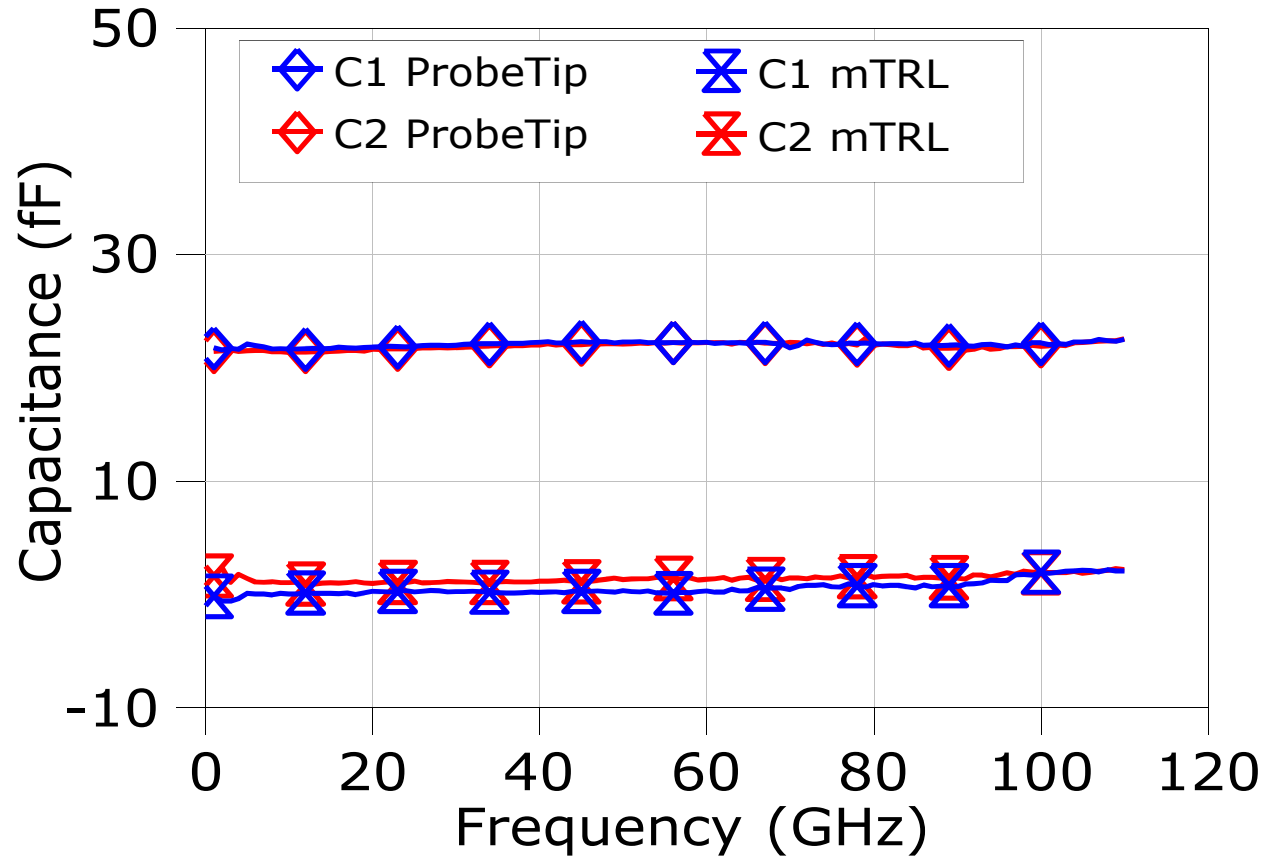
DUT Short



DUT

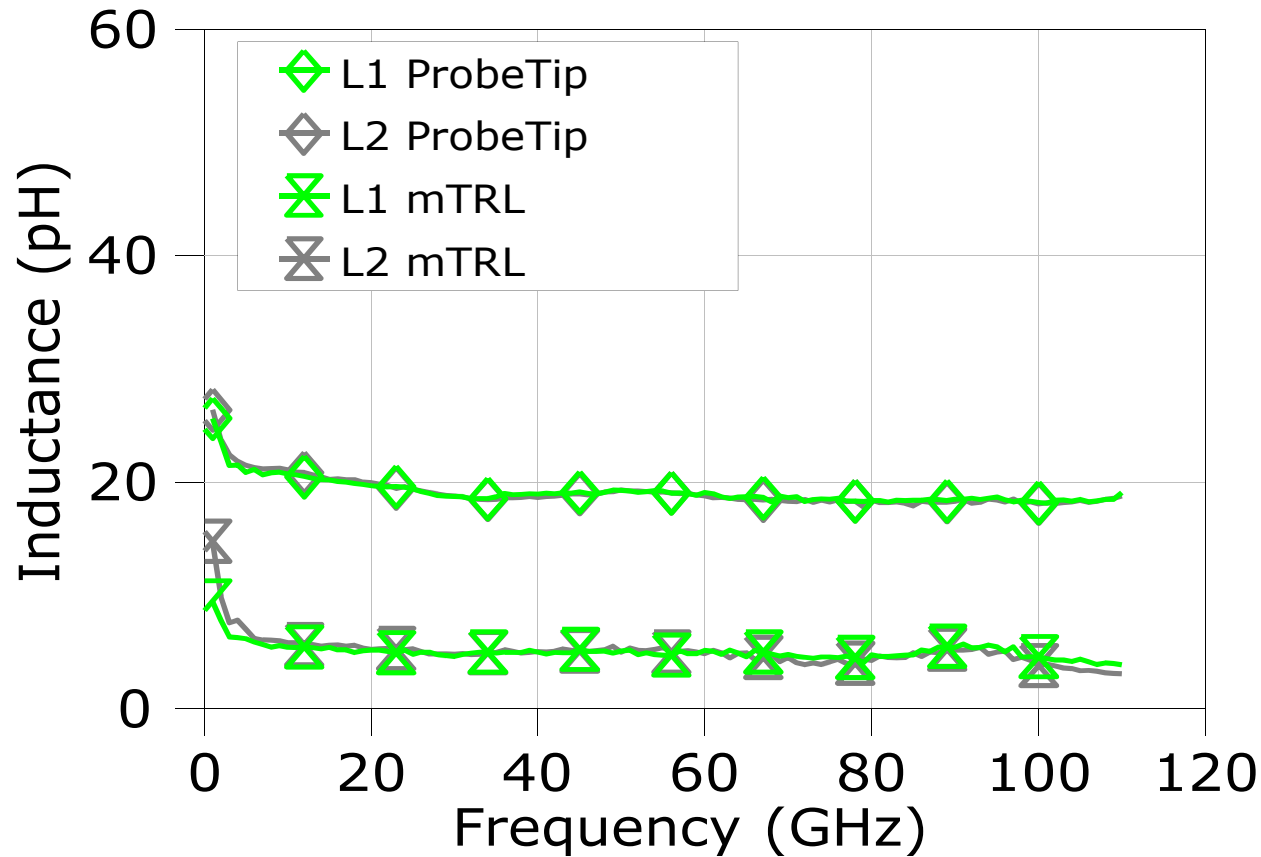


■ Capacitance of the Open Dummy



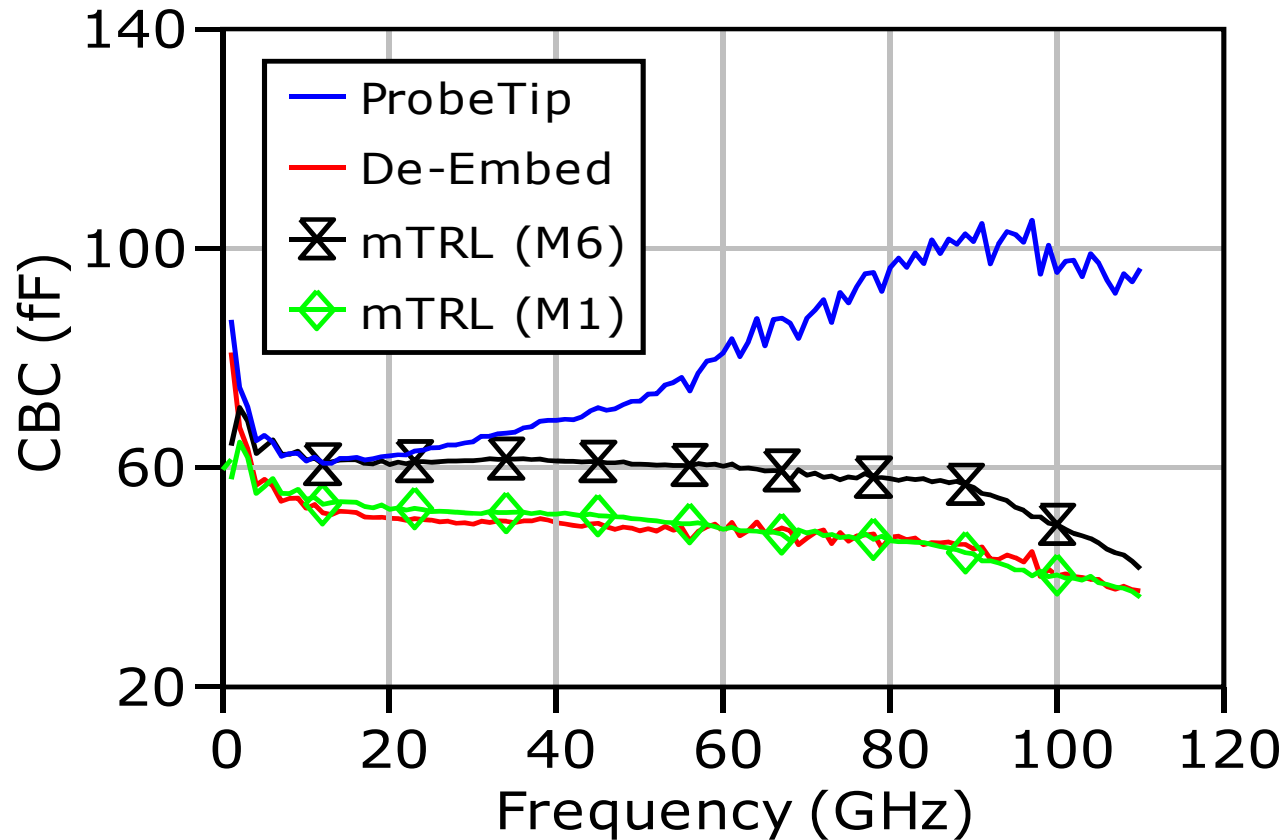
Equivalent capacitances decreased down to $< 1\text{fF}$

■ Inductance of the Short Dummy



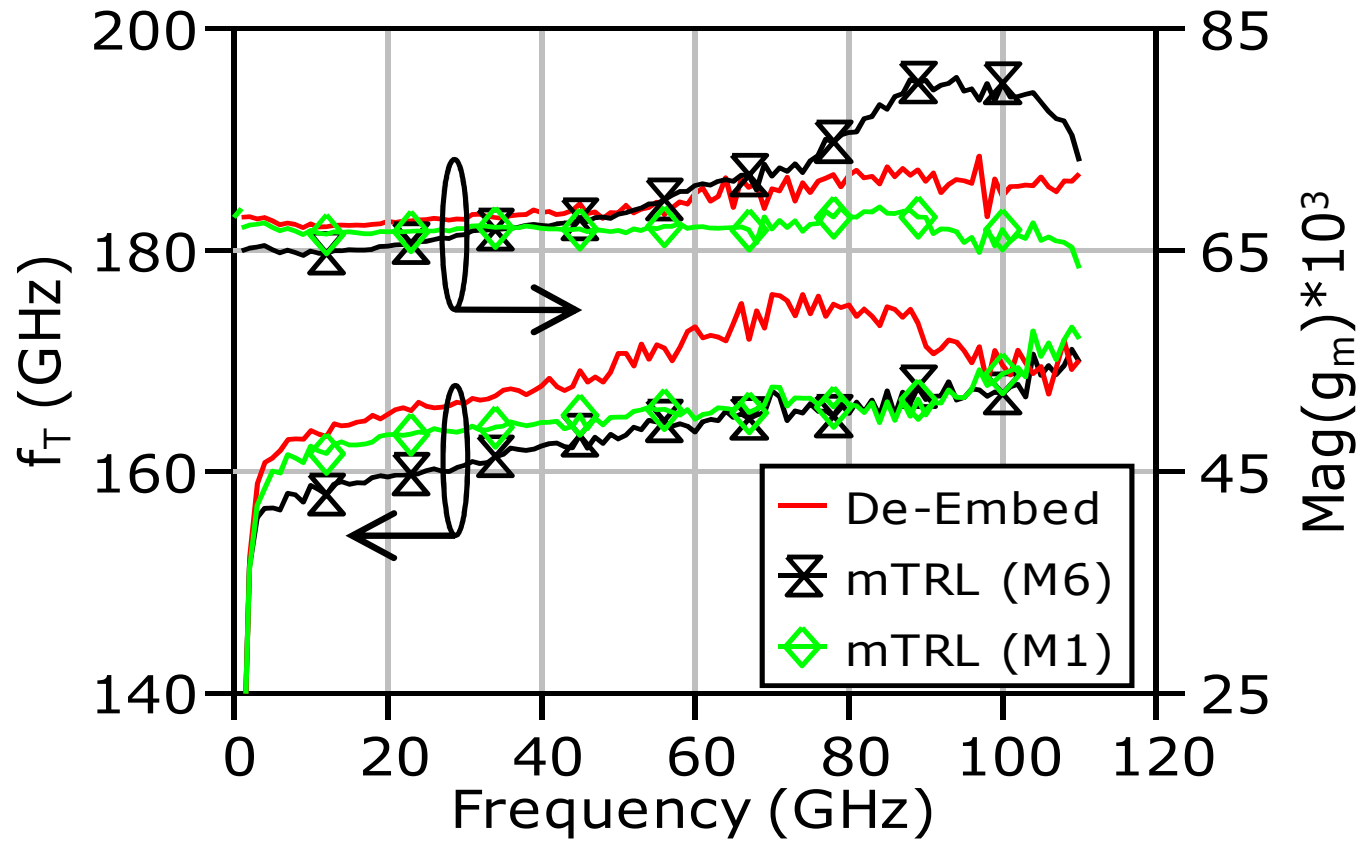
Equivalent inductance decreased down to < 5 pH

Comparison for DUT Parameters: CBC



Comparable results for CBC

Comparison for DUT Parameters: f_T and g_m



On-wafer calibration provided close to ideal results

■ Outline

- Motivation
- On-Wafer Calibration
- Design of Calibration Standards
- Comparison Results
- Conclusion

■ Conclusion

- Compared on-wafer calibration methods to the conventional pad de-embedding approach for an advanced BiCMOS process
- The proposed approach calibrates out the major part of the backend parasitics
- Possible distributed behavior of backend parasitics has no impact on calibration accuracy
- On-wafer calibrating is the most suitable approach for accurate characterization of high-speed silicon-based transistors

■ Acknowledgement

P. Chevalier, N. Derrier
from STMicroelectronics (France),

P. Sakalas from
Dresden University of Technology (Germany)

and

Agilent EESof division (USA)