Progress in Applying On-Wafer Calibration Techniques for Advanced High-Speed Silicon Technologies

Andrej Rumiantsev\textsuperscript{1)}, \textsuperscript{3)}, Franck Pourchon\textsuperscript{2)}

\textsuperscript{1)} Cascade Microtech Dresden GmbH, Suss-Strasse, 1, D-01561 Sacka, Germany

\textsuperscript{2)} STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles, France.

\textsuperscript{3)} Dresden University of Technology, CEDIC, D-01062 Dresden, Germany
Outline

- Motivation
- On-Wafer Calibration
- Design of Calibration Standards
- Comparison Results
- Conclusion
Transistor Measurement Challenges

- A transistor cannot be contacted (probed) directly:
  - Contact pads and interconnects are required
- Increase of measurement and operation frequency:
  - Impact of contact pads parasitics significantly increases

How to get rid of parasitics?
Conventional Method: Pad De-Embedding

- Complexity increases with an increase of frequency

One-Step (few GHz)

Five-Steps (<50GHz)

Alternative methods are required

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On-Wafer Calibration Goal

- To move the measurement reference plane close to the DUT terminals in just one step
Suitable Calibration Methods

- Multiline TRL:
  - Developed at NIST in early 90s
  - Original application: semi-insulating wafers (GaAs)
  - End of 90s: application techniques for Si

- LRM+:
  - First application: SiGe:C
  - Comparison vs. multiline TRL: GaAs, bulk Si
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Design of Calibration Standards

- Calibration reference plane tradeoff:
  - As close as possible to the DUT terminals
  - Locate standards as far as possible from Si (top metal)
Design of Calibration Standards: Load

mTRL Reference Plane

2 N+ salicided 50Ω Poly resistors
Characteristic Impedance of CPW

- **Lumped Load Method:**
  - Requires resistor (Load) embedded in the CPW launch
  - Load resistance $R$ can easily be measured
  - Difficulties:
    - Impact of Load reactance can decrease accuracy

- **Calibration Comparison Method:**
  - Requires initial reference calibration (probe tip, on ISS)
  - $Z_0$ of the test line is extracted from the second-tier cal
  - Difficulties:
    - Accurate reference calibration at mm-wave frequencies
    - Impact of the Si line launch can decrease accuracy
Standards: Measurement of Line $Z_0$

Lumped load method provided sufficient accuracy
Two-step de-embedding provided comparable results
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Calibration Verification Results

- Four calibration conditions:
  - Probe Tip
  - Probe Tip + De-embedding (conventional)
  - On-wafer mTRL, reference plane M6
  - On-wafer mTRL, reference plane M1

- Three elements: DUT Open, DUT Short, DUT
Capacitance of the Open Dummy

Equivalent capacitances decreased down to < 1fF
Inductance of the Short Dummy

Equivalent inductance decreased down to < 5 pH
Comparable results for CBC
Comparison for DUT Parameters: $f_T$ and $g_m$

On-wafer calibration provided close to ideal results
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Conclusion

- Compared on-wafer calibration methods to the conventional pad de-embedding approach for an advanced BiCMOS process
- The proposed approach calibrates out the major part of the backend parasitics
- Possible distributed behavior of backend parasitics has no impact on calibration accuracy
- On-wafer calibrating is the most suitable approach for accurate characterization of high-speed silicon-based transistors
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