Challenges in Modeling Layout Systematic Effects in Compact Device Models

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Electrical & Computer ENGINEERING

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Outline

- Motivation
- Variability sources and trends
- Analog/RF Modeling Challenges
- SOC Modeling Challenges
- pdBRIX™ for the 28/20nm technology node
- Conclusions

Technology scaling enablers

- **Strain and Substrate engineering remain major performance boosters after HK MG introduction (32 nm IBM Alliance and Intel)**
  - Process complexity continues to increase despite (or along with) the benefits from HK-MG

Performance booster	Impact on NMOS	Impact on PMOS
Dual Stress Liner (Gate First)	Mobility improvement from Tensile liner	Mobility improvement from Compressive liner
eSiGe	N/A	Mobility improvement from Compressive stress
Contact-induced strain	Bar contacts with recessed NMOS Active	N/A
Gate induced strain (Metal Gate Last)	N/A	Additional Strain allowed by Replacement Gate
SMT - Stress Memorization (Gate First)	Mobility improvement due to Strained Poly – induced stress	N/A
S/D emb SiC	Mobility improvement from longitudinal Tensile stress	N/A
Substrate orientation	(100) Beneficial across wide range of stress level	(110) better for hole mobility, gain deteriorate with stress level

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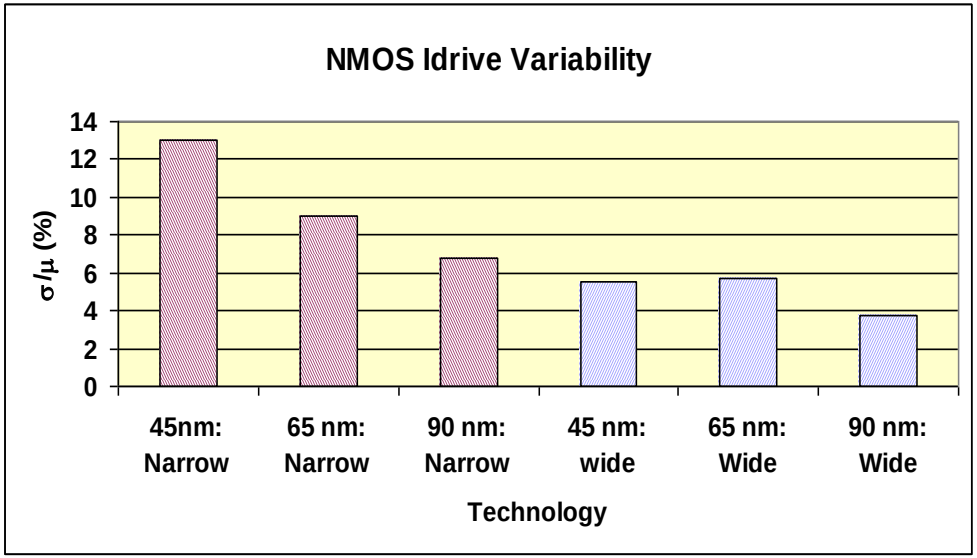
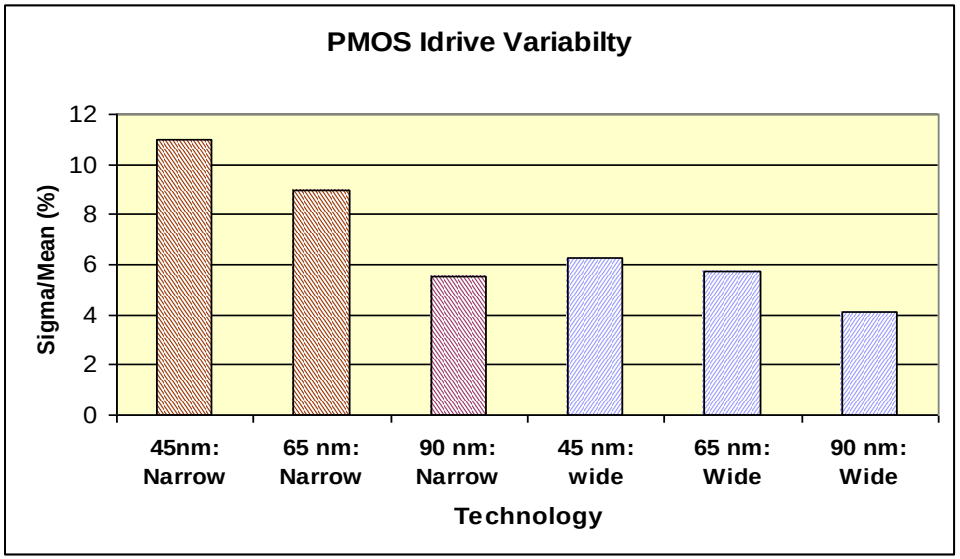
Variation Trends: Total Variation

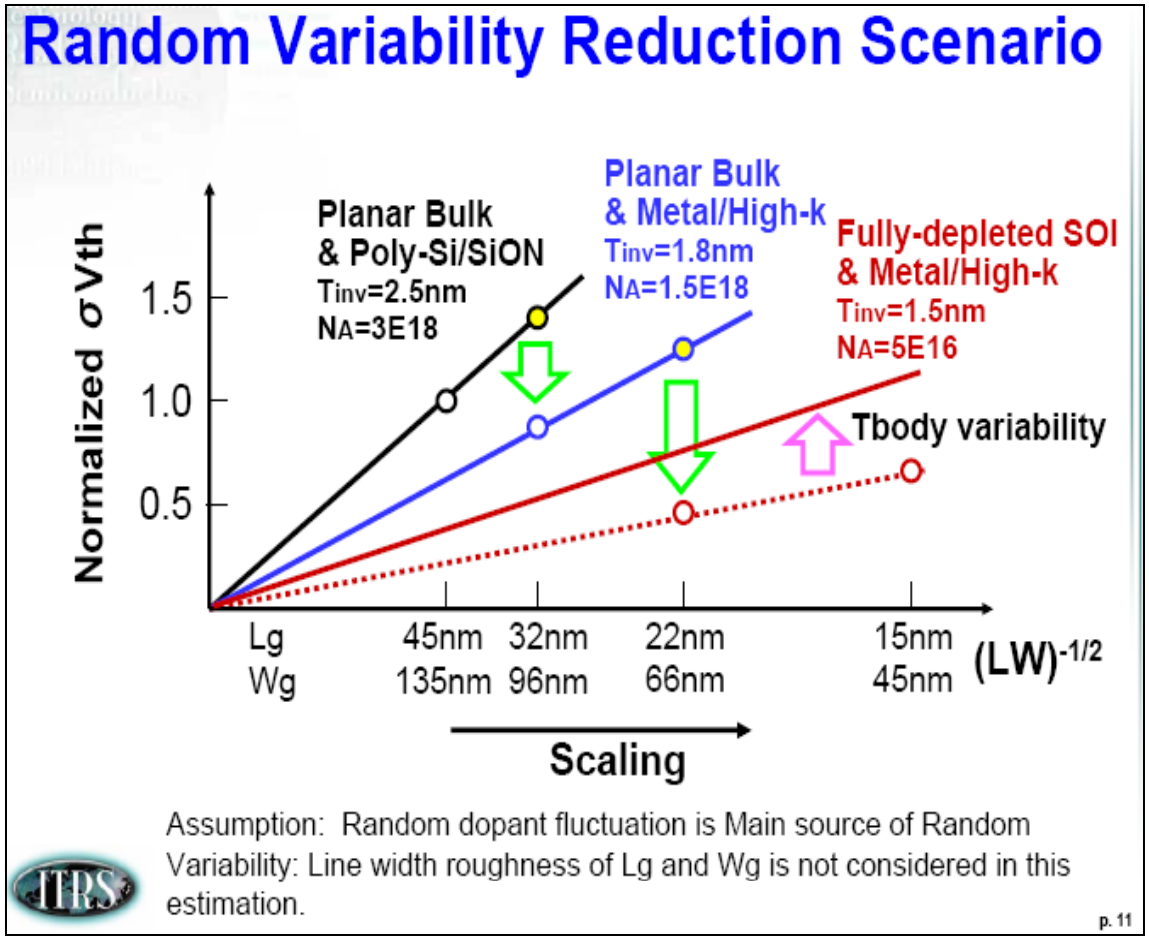




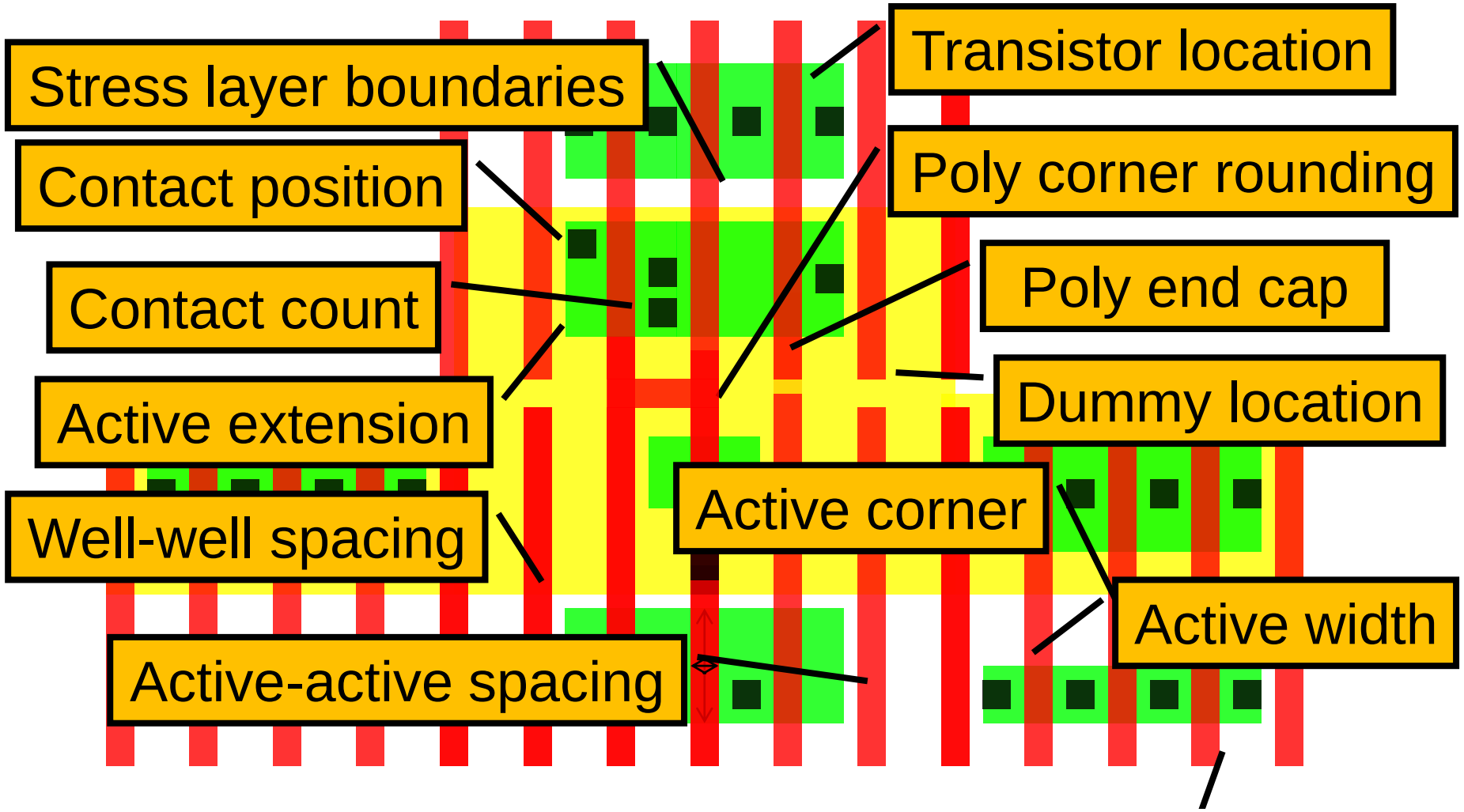
- Identical structure data presented here (no layout variability impact included)
- Total variation is increasing with scaling
- At 32 nm node, narrow transistors have 3σ variability > 45%, diminishing the benefits of scaling

Random Variability

- **Random variations play an important role**
  - Line edge roughness (LER)
  - Random dopant fluctuations (RDF)
- **Metal gate/High-K saves us for one generation only: 32nm/28nm**
- **RDF impact can be minimized by choosing different transistor architectures (FinFET, Ultra Thin Body or Fully Depleted SOI)**



Transistor Layout Effects



- 32/28nm logic has 2000+ unique transistors to characterize & model
- 45, 000+ DOE levels required to characterize transistor models
- Assuming 8 replicas and Kelvin/leakage arrays more than 400k transistors needed in a test chip for full characterization

Layout Effects in Nanometer Technologies

- **Printability and stress effects increase systematic layout variation**

Systematic variation (*)	Root causes	Impact at the 45/32nm technology node
Gate poly orientation	Poly lithography	N/A
Gate poly pitches	Poly OPC and lithography Stress Layers Loading effects from Etch and film deposition	3-5% - printability 15% - poly pitch related stress 5% - contact space related stress
Poly corner rounding	Poly OPC and lithography	15%
Transistor location in multi-gate transistor	Poly patterning and stress impacted by local neighborhood differences	15%
Active corner rounding	OPC and lithography, stress	7%
Un-modeled narrow width effects	Stress effects, poly step height	
Gate to active edge	STI stress, e-SiGe stress	10-20% for PMOS with e-SiGe
Well proximity	Implant scattering	
Nwell-Pwell separation	Gate counterdoping and misalignment	
Contact density and placement	Silicide sheet resistance and stress layers	

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Transistor Care-abouts vs Applications

	Digital		Baseband Analog	RF (< 5GHz)
	Logic	SRAM		
IDSAT	Critical			
IOFF	Critical		Somewhat critical (SNR degradation)	Not critical
VTSAT	Critical			
Igate	Critical		Impacts Ids matching, SNR	
Cgg (Covl+Cgb)	Critical			
Cj	Critical			
Gm at low Ids	Not critical		Critical	
Gds	Not critical		Critical	
Mismatch	For Clock trees etc	Show stopper	Critical	
Linearity (IP3)	Not Critical		Somewhat critical	Critical
f_T, f_{max}	Not critical			Critical
Noise (1/f, NFmin)	Not critical		Critical (SNR degradation)	Critical
Rsub	Low Rsub for latchup			High for Q

- Analog/RF designs have different/additional care-abouts from digital logic & SRAM technology drivers

Consequence of Transistor Scaling for Analog/RF

Care-about	45/40nm	32 nm MG/HiK	32nm Poly/SiON
Intrinsic gain (gm/gds) (Lmin, Vgs=Vds=Vdd/2)	~10	Similar or better due to gm ↑ and (potentially) gds ↓	Similar to or better than 40nm due to gm
Gate Leakage	~0.75 nA/um2	25-1000X lower	Same or higher than 45 nm
Mismatch	nMOS Avt ~ 3.0 mV/um	Significantly better than 40 nm & Poly/SiON	Avt same as 40 nm, min area matching worse
Linearity		Degraded, but potentially less compared to Poly/SiON	Degraded due to scaling
1/f noise	~1e-11 $V^2.um^2/hz$	Same as 45/40	Potentially degraded due to nitridation
f_T/f_{max}	~370/410 GHz	Higher than 45/40	Higher than 45/40
Layout dependence	Severe	Similar to Poly/SiON	Similar to 40nm HP
NF		Similar to Poly/SiON	Improved by scaling
Thermal Stability		Potentiality worse	Same as 40nm
Reliability (NBTI/HCI)	> 10 years	Same as Poly/SiON (>10 yrs) PBTI could be an issue	Potentially degraded due to nitridation
Process cost/other risks	Std CMOS cost	Double patterning Higher than Poly/SiON	Double patterning

Transistor Scaling Impact Summary

- **The 32/28 nm technology node has distinct technology choices, each with its advantages and risks**
  - In additional they share some common risks, like increased layout sensitivity
- **All the consequences of these choices on Analog/RF design are unclear**
  - The trade-off is more clear for digital logic design and SRAM
- **Poly/SiON**
  - Next generation of a proven technology; better understood trade-off in terms of performance and cost
  - In general devices will have worse electrostatics compared to MG/HiK, with its attendant impact on Analog/RF design (linearity, matching, leakage)
  - Reliability degradation as a consequence of Tox scaling
- **Metal Gate/Hi-K**
  - Benefits of devices with much better electrostatics (matching, linearity, leakage)
  - Improved reliability due to larger Tox(physical) ⇨ Lower E-field
  - However, new phenomena like Thermal stability, Resistor TC
  - Process cost
- **Accurate and comprehensive characterization will be essential for effective utilization of either of the technology choices for Analog/RF design**

Analog/RF Design in 40nm and 32nm Technology Nodes

- **40nm Process – the best analog/RF process since 130 nm [Klaas Bult - Broadcom Analog/RF CTO at 2009 ESSDERC Panel Discussion]**
- **All analog devices use minimum L (same as digital)**
- **Large area (equivalent width) devices used to average RDF effects**
- **Full dummification: very few layout patterns**
- **Mismatches modeled precisely based on Si characterization results**
  - Small number of patterns to characterize
- **Very aggressive shrink achieved**
- **No area penalty due to dummification**

- **32/28nm processes with MGHK:**
  - Improved transistor matching

- **Intel uses only 2 L values in their SOC's: one for digital and one of analog transistors [Mark Bohr - Intel at 2009 ESSDERC Panel Discussion]**

- **Full dummification to eliminate layout systematics**

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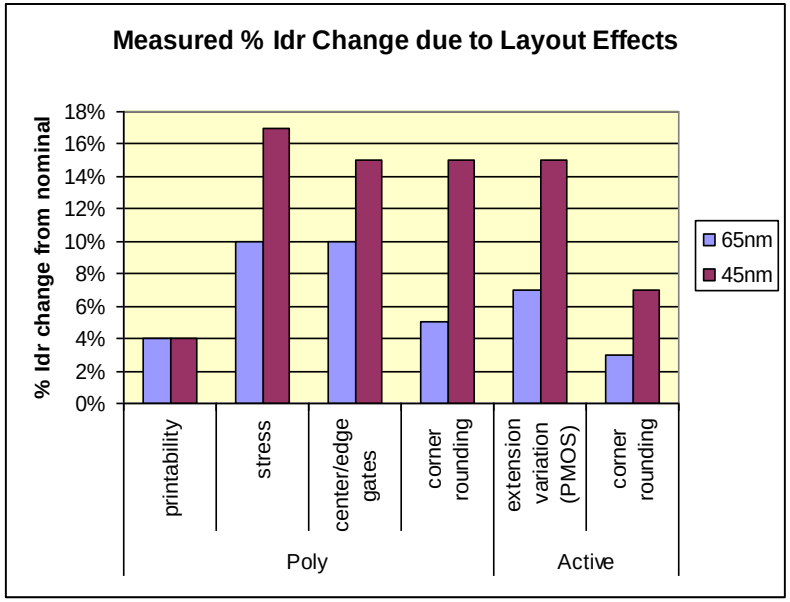
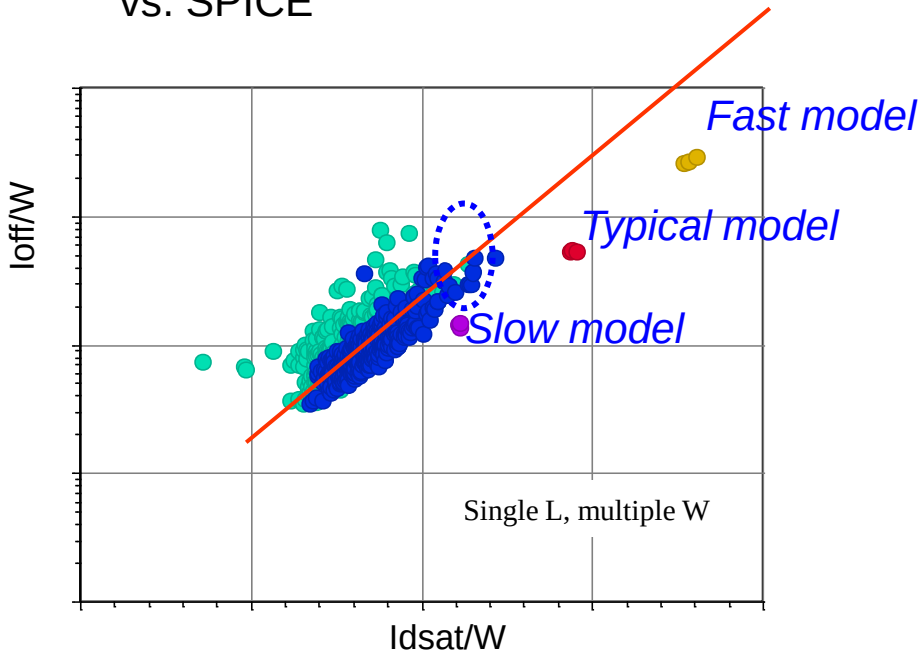
Layout Dependency Increasingly Important

45/40nm PMOS Measurement Layout Dependency



45/40nm PMOS Measurement vs. SPICE



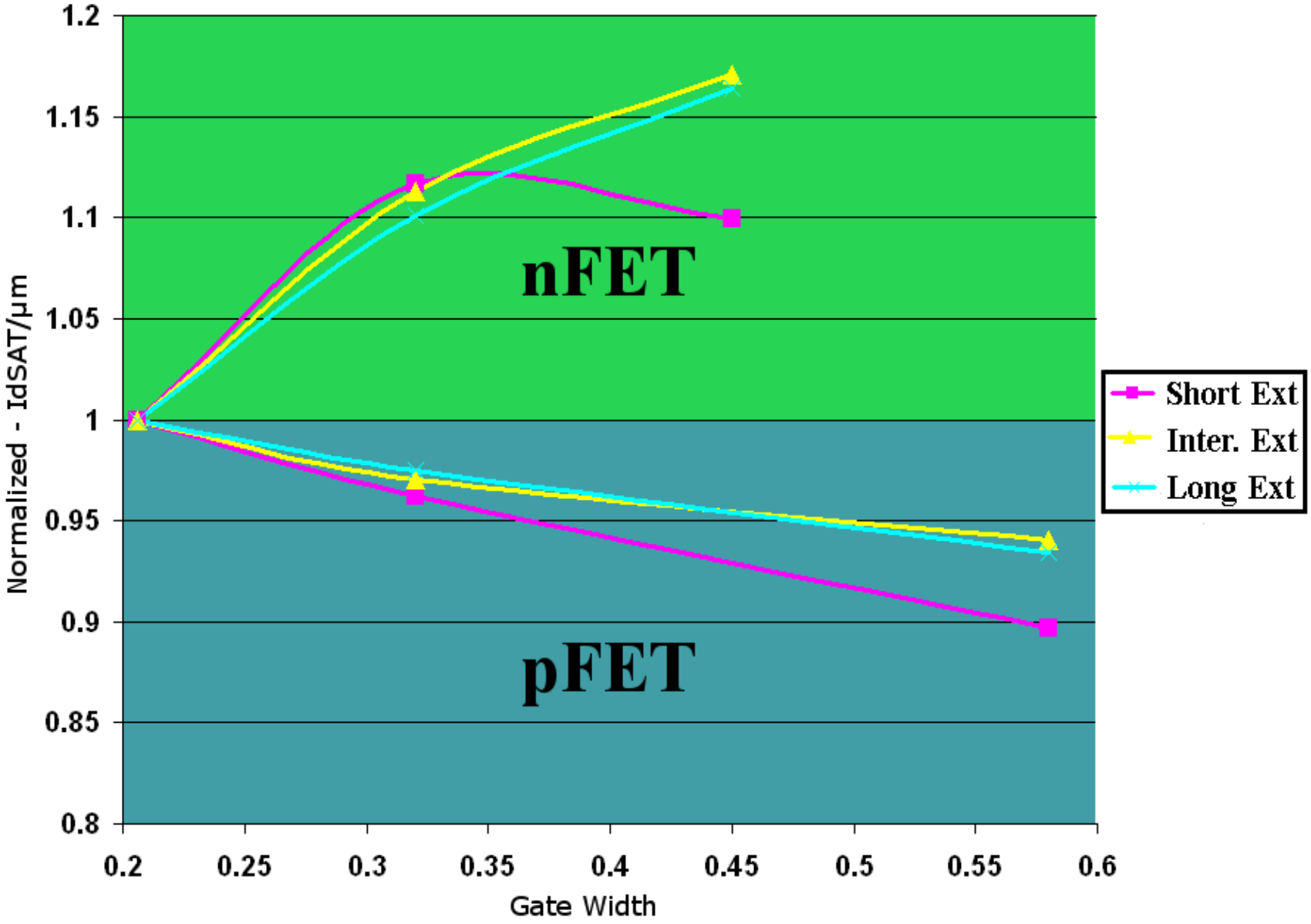
- Performance dependence on layout increasing
- Model accuracy decreasing

Key is to evaluate wide range of layout dependencies relevant to product

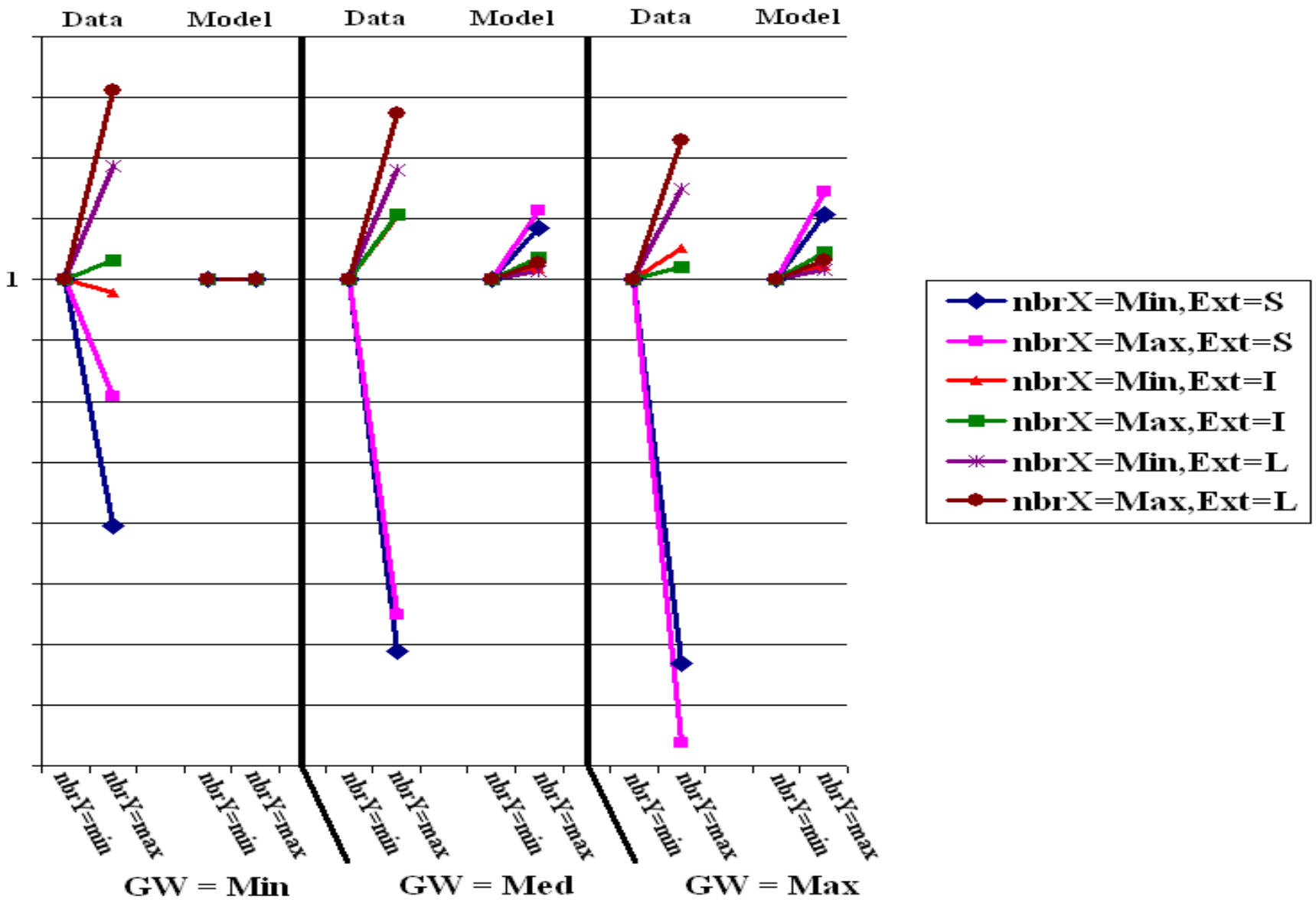
Device Modeling of Layout Interactions

- **Process advancements have made device behavior highly sensitive to the drawn geometry**
- **Modern day modeling methodology fails to accurately model entire design space**
- **Restricting the design space with regular fabrics can provide more accurate models**

Device Modeling of Layout Interactions



Device Modeling of Layout Interactions

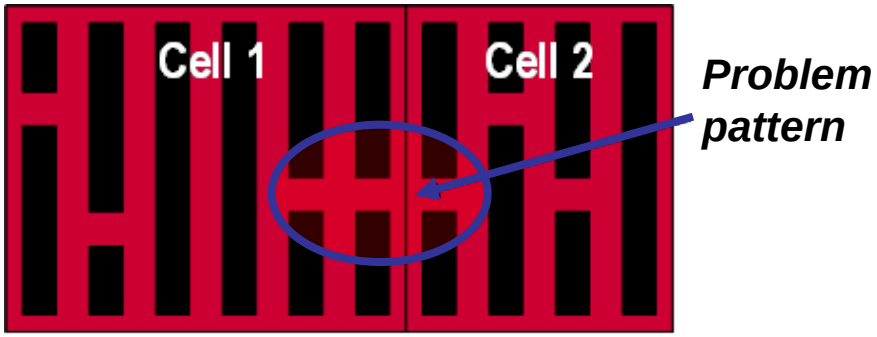


Variability: Is this a problem designers should be addressing?

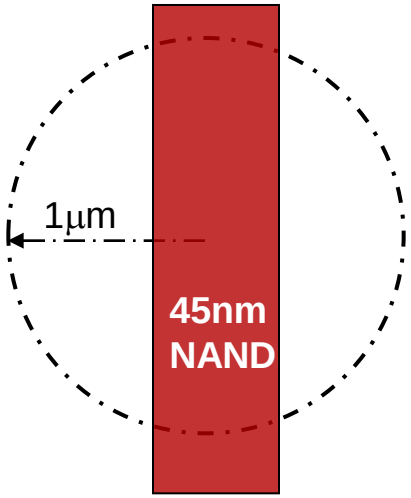
- **Designers' historical perspective:**
  - **"My world starts with SPICE models and Design Rules. It is up to the Foundry to get the SPICE models correct and the support the entire valid DR space"**
- **Current reality: silicon**
  - **Even typical gridded SOC designs can have >10,000 different transistor patterns**
  - **Complexity of interaction effects makes it hopeless for foundries to cure this problem**
  - **Physics won't change or improve as node matures – certain patterns will always have higher variability**
- **Let's restore designers freedom at advanced nodes**
  - **Selecting right set of low variability patterns**
  - **Validating SPICE models in silicon for those patterns**
  - **Ensuring manufacturability of metal patterns used in design**

Need for Limiting Number of Patterns

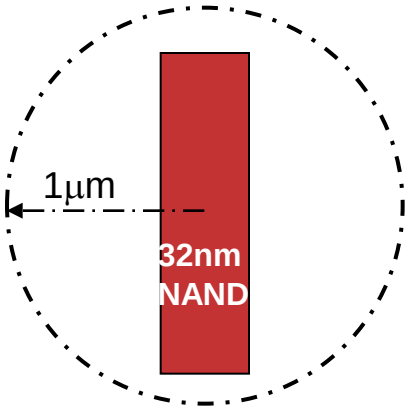
- **Improved predictability requires limiting the number of unique patterns**
- **New patterns are created from cell abutments**



- **Without wavelength scaling the optical interaction remains constant**
  - More cells fall within the same optical region of influence



Pattern influence range for 193nm lithography



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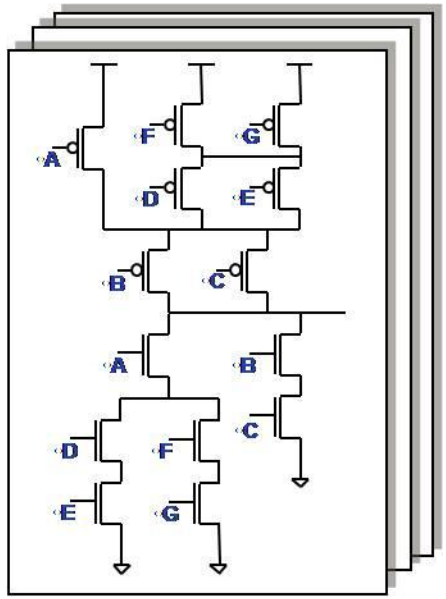
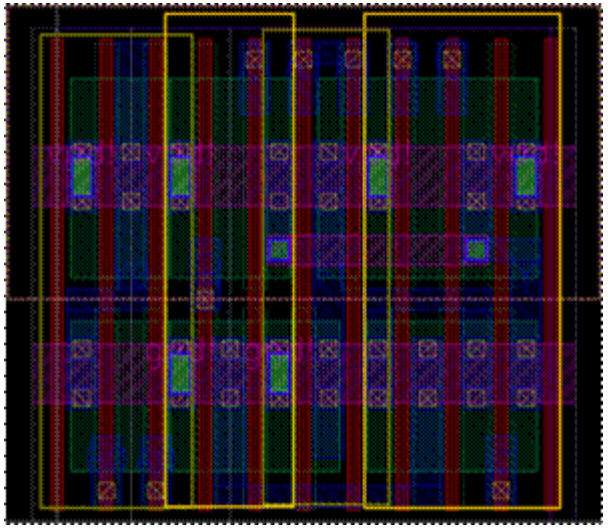
pdBRIX™ Logic Templates

- **Templates: Limited number of single-stage logic topologies (including all primitives: INV, NAND, etc.)**
  - We select approximately 70 of them that are most useful across wide application range given transistor stack height constraints

- **Choosing limited set of layout constructs to implement templates provides pattern predictability**
  - Well chosen layout constructs can facilitate exhaustive qualification of all possible patterns including neighborhoods

- **All logic cells and functions can be constructed as combinations of the qualified template layout set**



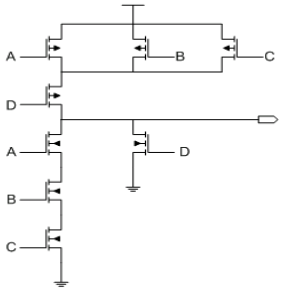


Reduce variability through pdBRIX™ design
Exhaustively characterize all patterns used

pdBRIX™ Library Creation Infrastructure

STANDARD CELL LIBRARIES:

Complete standard cell library assembled from templates

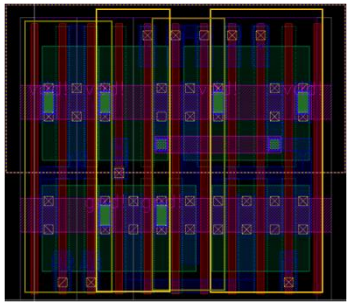


Silicon predictability achieved by:

- Merging, embedding, and abutting silicon qualified templates
- pdBRIX ensures zero new silicon layout patterns are created
- Tighter (simplified) SPICE models

TEMPLATES:

Small set of single stage logic functions built on Fabrics

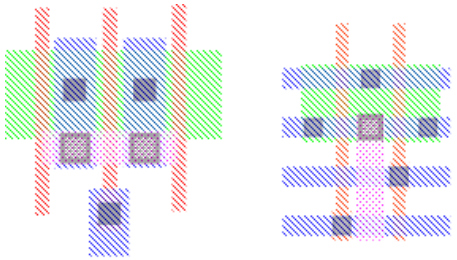


Co-optimized with fabrics and library:

- Functions selected for optimal library coverage
- Layouts co-optimized with fabrics for best area, power, and performance
- Minimize number of patterns created

FABRICS:

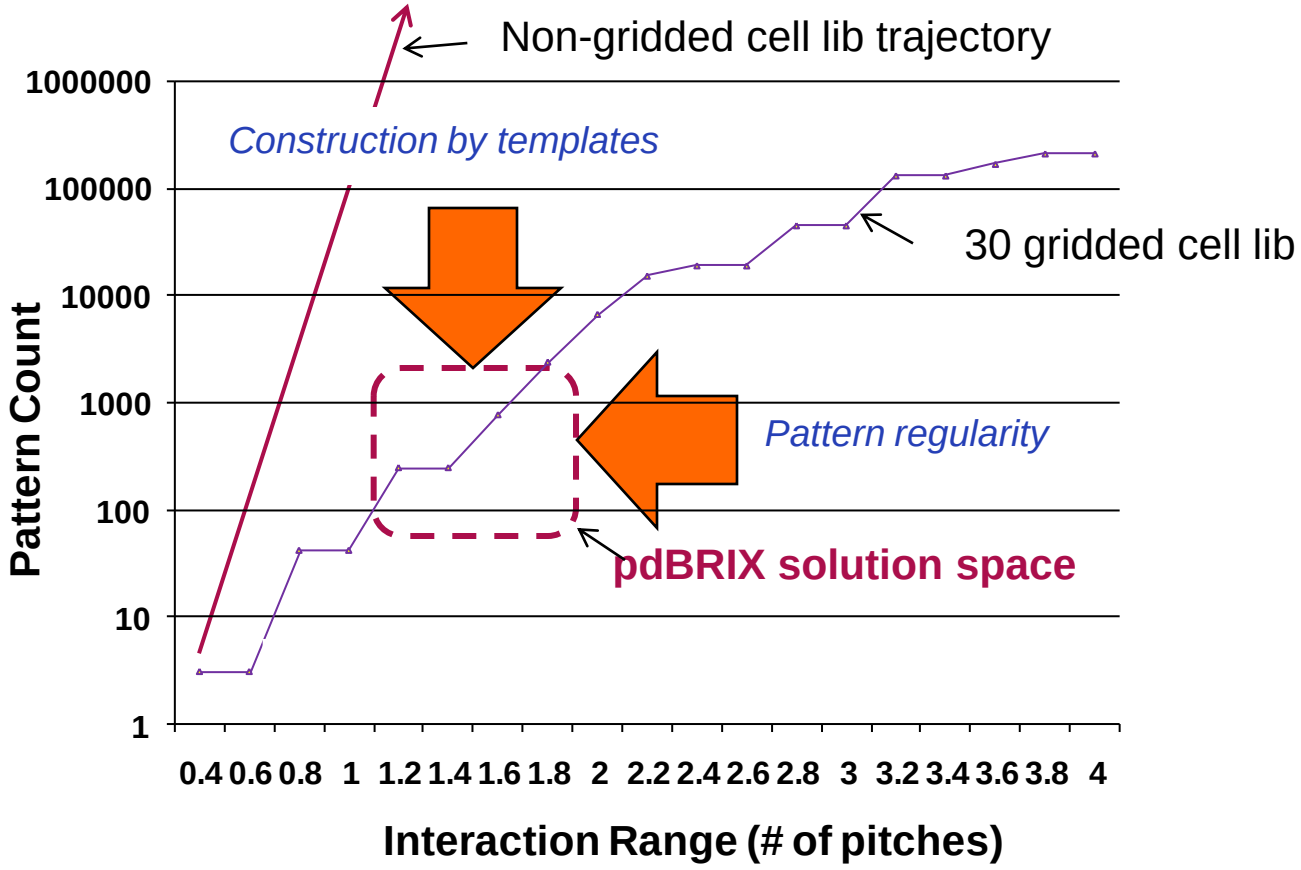
2-D grid environment defining allowed poly and metal shapes



Selected based on:

- Litho printability
- SRAM compatibility
- Yield optimization
- Product needs such as redundancy

Fewer Patterns → Better Predictability



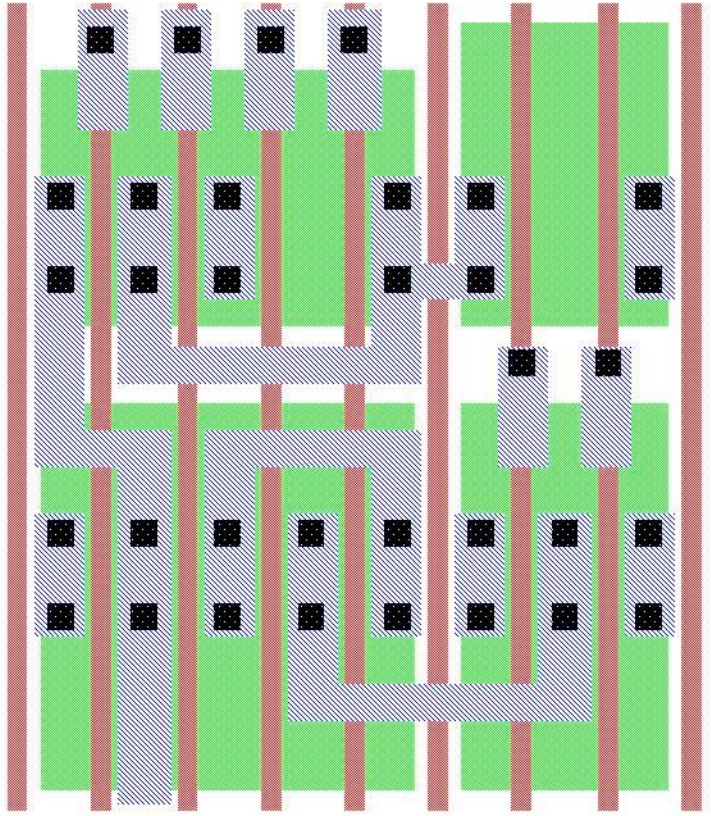
Controlling layout patterns enables exhaustive qualification of the layout space over the relevant interaction range

32/28nm Bulk Fabric Fabricated

- **Fabric chosen to accommodate manufacturing objectives and template requirements for design**

- **Fabric characteristics**
  - Fully gridded transistors
  - Limited diffusion jogs
  - Relaxed metal pitches
  - Limited “two-way” metal patterns
  - 100% active contact redundancy (9T+)
  - **Portable to 28nm**

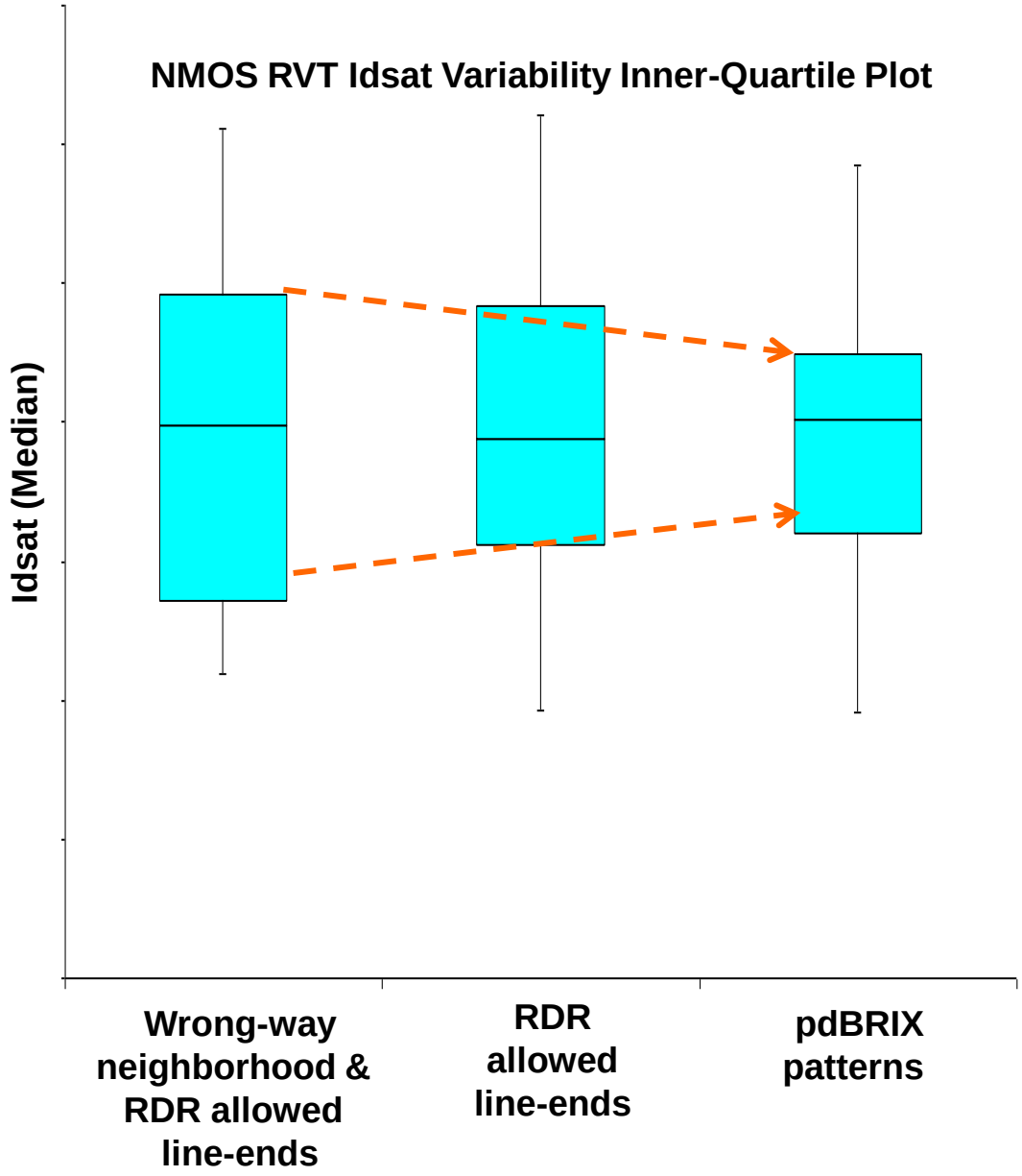
- **Qualifying layout constructs**
  - 8T, 10T and 13T silicon qualified
  - 9T, 11T, 12T and 14T+ available via virtual qualification



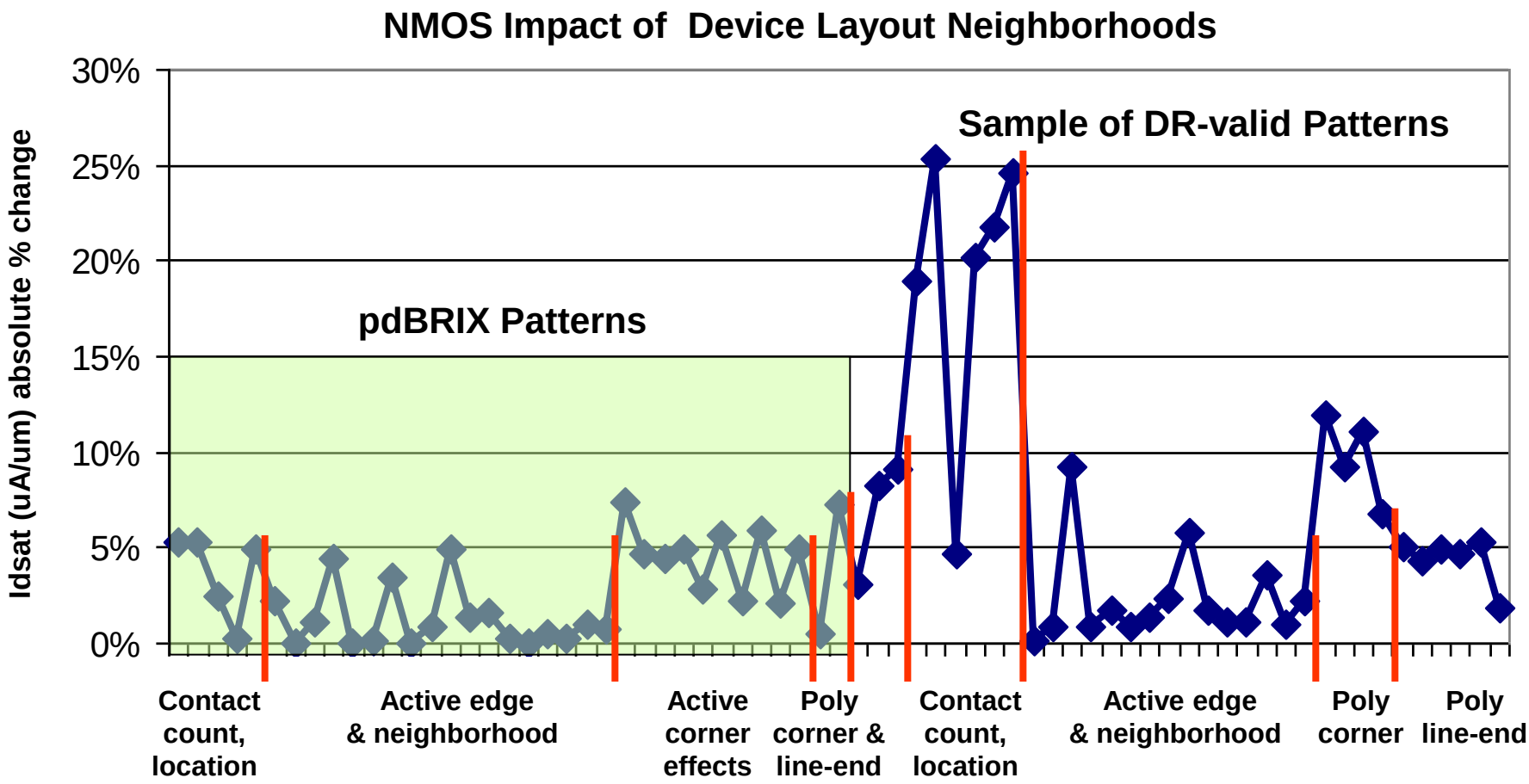
X = !(E(A+B)(C+D) + F)

Fabric Optimization: Parametric Variability Control

- Limited set of regular design can eliminate over half of NMOS Idsat variability due to poly effects
- More predictive transistor performance in std. cell & IP layout

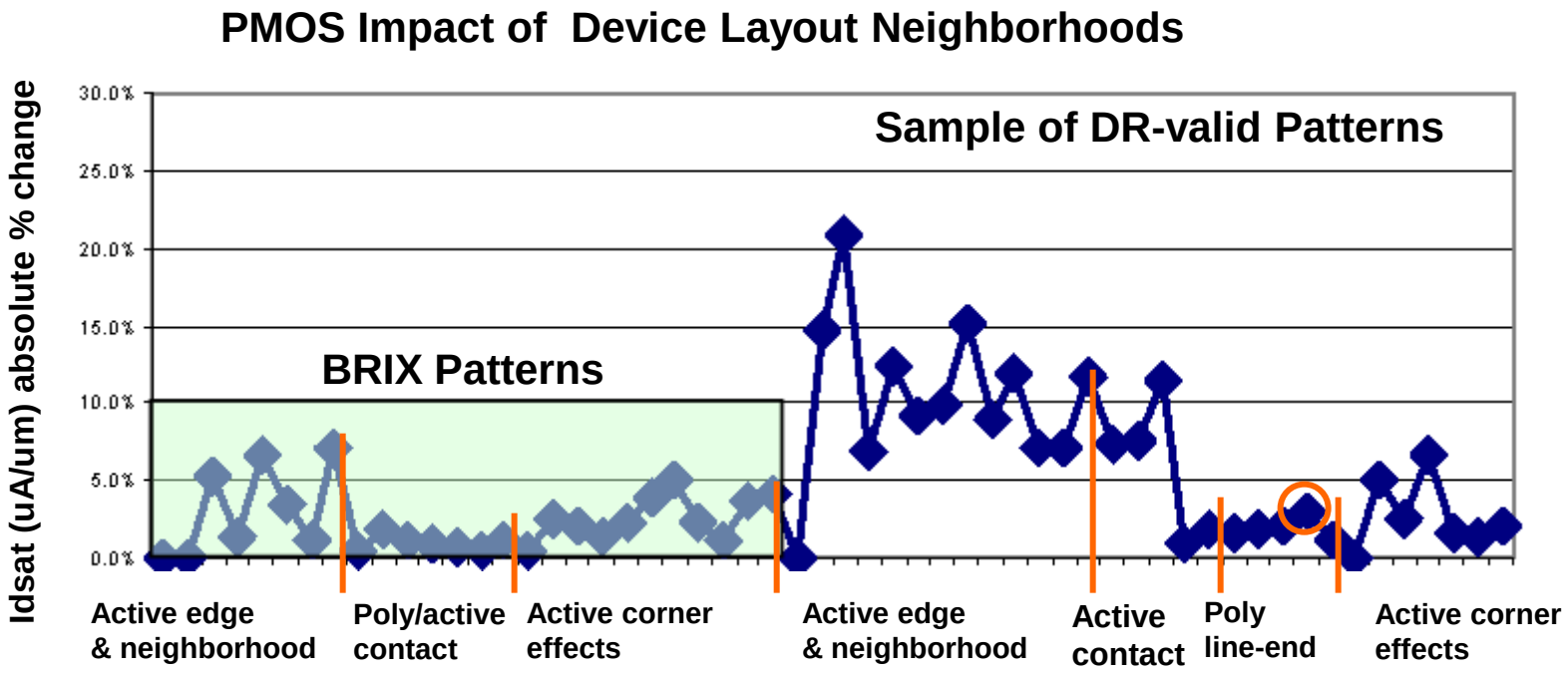


28LP NMOS Idsat Layout Dependency



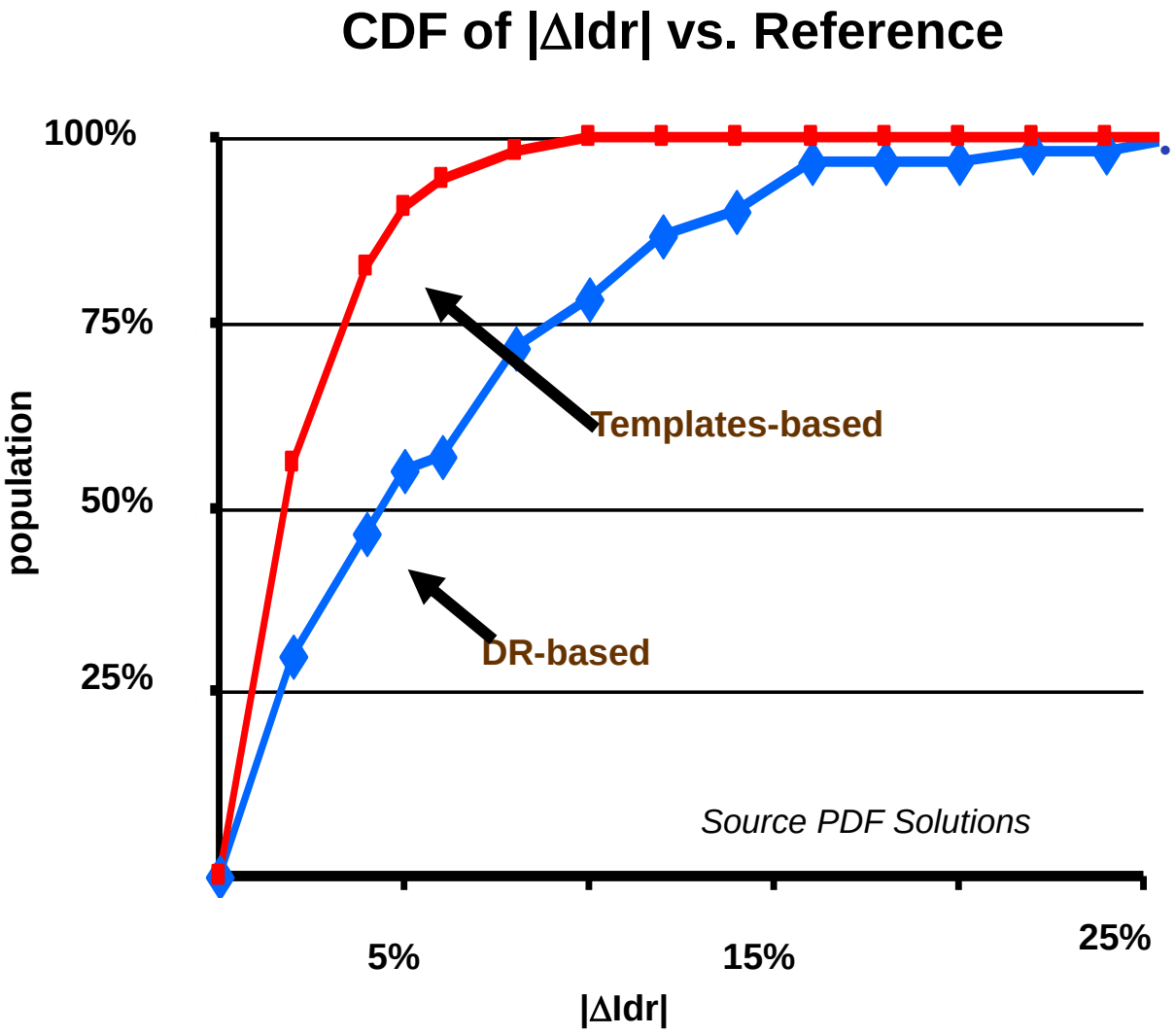
- **Transistor layout and layout neighborhood can significantly impact transistor performance**
- **~35% reduction in Idsat variability due to layout & neighborhood for pdBRIX NMOS transistors**
- **pdBRIX limits total number of transistor logic patterns**
  - Can avoid high variability patterns
  - Enables more accurate Si-to-SPICE matching of limited layout patterns

28LP NMOS Idsat Layout Dependency



- ~30% reduction in Idsat variability due to layout & neighborhood for pdBRIX PMOS transistors
- pdBRIX transistors can be qualified & modeled over all patterns. Cannot insure performance over all DR-compliant patterns in an SoC

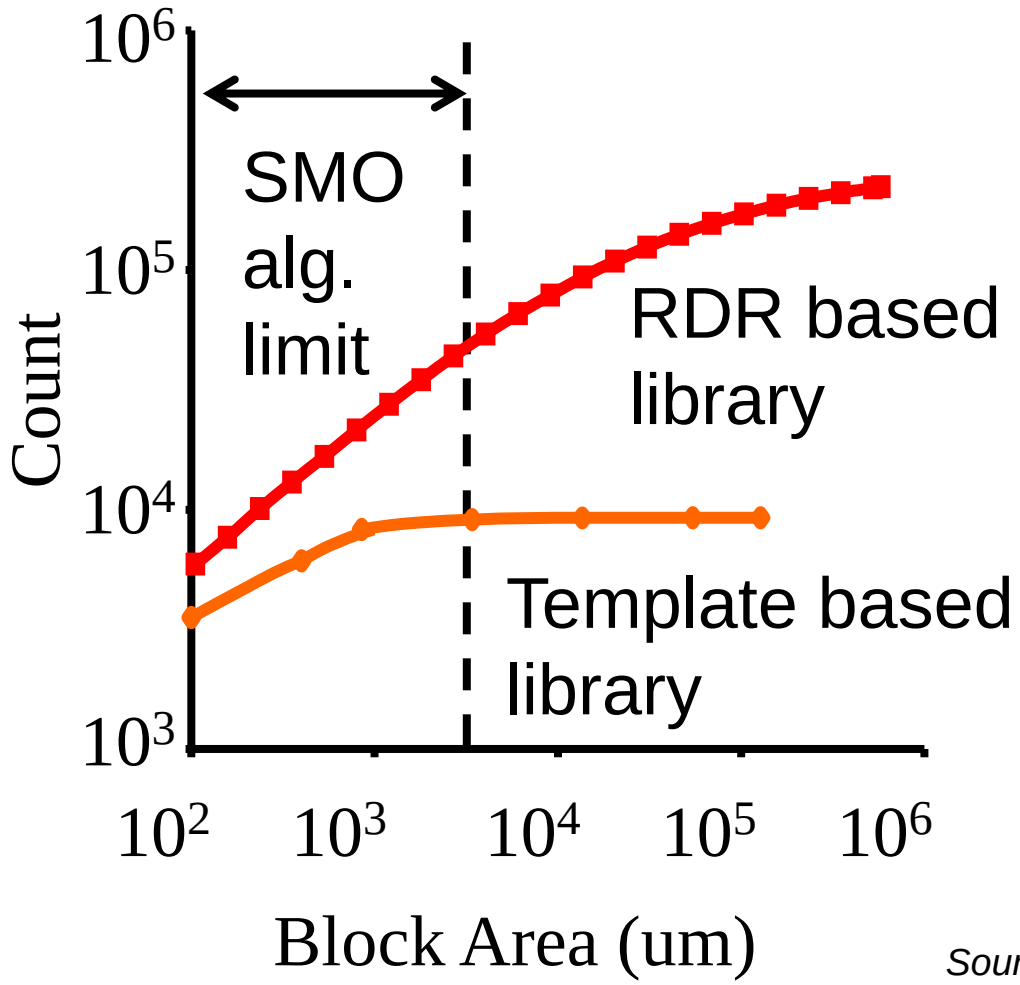
… Enabling Design With Low Variability



Significantly tighter transistor performance distribution possible from limiting transistor neighborhoods

Achieves 22/20nm Pattern Control

Pattern Count vs. Block Area
22/20nm node, 2 pitch interaction range



- **Templates provide pattern constraint beneficial for source-mask optimization algorithms**

Source PDF Solutions

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pdBRIX Templates Improve Model - Hardware Correlation

- **Templates: "Model = Hardware" → helps achieve working first silicon**
  - New simplified interface between foundry and std. cell / IP designers
  - Templates plus basic (process-integration driven) design rules replace increasing complex design rule manuals
  - Results in "correct by construction" IP
  - Enable compatibility across foundries

- **Templates achieve "Model = Hardware" from:**
  - Comprehensive Si verification enabling foundry to focus on specific patterns
  - Low layout pattern count compatible with SMO / DPT
  - Elimination of product-specific "hot spots" or yield loss mechanisms
  - Limited transistor patterns enable complete Si-to-SPICE validation

- **Templates have been validated:**
  - 40nm: adopted by Toshiba
  - 32/28nm: validated on IBM Alliance CV's
  - 22/20nm: validated with ASML/Brion Tachyon SMO (Si verification underway)
  - Fabless: adopted at 20nm

Conclusions

- **Variability crisis continues although MGHK architecture helps for one generation (32/28nm)**
- **Si-SPICE mismatch has become a key limiter**
- **Systematic layout effects must be eliminated**
- **Proposed comprehensive methodology for design-process co-optimization to reduce the cost per good die**
  - Extensively verified in silicon
- **Regular design methodology with limited number of patterns only viable means for advanced lithography solutions such as SMO and interference assisted lithography**
- **Current methodology can be used to concurrently determine the optimal lithography and design solutions for application domain**
  - Successfully Implemented in the 22/20nm technology node