Research progress of SOI devices and modeling in SIMIT

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Introduction of SOI Group

- Research results
  - DC Device Model
  - RF Device Model
  - Research of SOI Device
  - Fruits of international cooperation

Summary
Prof. Xi Wang  
Academician of the Chinese Academy of Sciences

Prof. Shichang Zou  
Academician of the Chinese Academy of Sciences

- Total 78 people
- 14 professors
- 10 associate Professors
- 38 graduate students
**Research field**

- SIMIT research teams are actively driving new SOI technology development, e.g. material, device, process, design services, products etc., help to build up SOI ecosystem.

### SOI Material
- SiGe, Strain SOI
- GaN, Graphene

### SOI Design Service
- Process, Device, Modeling
- PDK, Library, IP

### SOI Circuit
- ASIC, FPGA, ADC, Switch

### SOI Photonics
- AWG, MMI, High-end microprocessor
100+ papers published, 150+ patents applied (including 50+ international), within the last 5 years.

the Prize of National Science & Technology Advancement (1st grade)
SOI Roadmap in SIMIT

**Technology**
- 0.13um SOI Logic Process
- 0.2um SOI RF Process

**Substrates**
- Simox
- Smart cut

**Timeline**
- 1980s
- 2000s
- 2014s

*Shanghai Institute of Microsystem and Information Technology*
Laboratory has the ability to test DC, RF and flick noise.
Laboratory has a complete EDA solution for device modeling.

- **Sentaurus TCAD Tool**
  - Sentaurus PROCESS SIMULATION AND STRUCTURE
  - Sentaurus GRID GENERATION
  - Sentaurus DEVICE SIMULATION

- **Agilent Model Tool**

- **Cadence Tool**
  - Custom IC Design Tools
    - Virtuoso Front-to-Back Design Environment

Shanghai Institute of Microsystem and Information Technology
Outline

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  - RF Device Model
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- Summary
**DC Device Model**

- We have extracted a complete DC Device Model for 0.13 um SOI Technology.

<table>
<thead>
<tr>
<th>Device</th>
<th>MOS (FB, TB, HB), BJT, Resistor, Diode, MIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level</td>
<td>70 (BSIM4SOI)</td>
</tr>
<tr>
<td>Effects</td>
<td>FBE/GIFBE, SHE, Gate-leakage, GIDL</td>
</tr>
<tr>
<td>Geometry</td>
<td>L[0.13<del>10um], W[0.15</del>100um]</td>
</tr>
<tr>
<td>Geometry</td>
<td>IO: L[0.35<del>10um], W[0.3</del>100um]</td>
</tr>
<tr>
<td>Temp.</td>
<td>-55~125°C</td>
</tr>
<tr>
<td>Voltage</td>
<td>Gate: <a href="core">-1.32~1.32V</a> / <a href="IO">-3.63~3.63V</a></td>
</tr>
<tr>
<td>Voltage</td>
<td>Drain: <a href="core">0~1.32V</a> / <a href="IO">0~3.63V</a></td>
</tr>
<tr>
<td>Corner</td>
<td>TT, FF, SS, FS, SF</td>
</tr>
</tbody>
</table>

Golden Wafer for SOI Device modeling

The contents of 0.13 um SOI model library
Model QA

◆ All corner of model have correct trend, without warning and error. We have an detailed QA report of 0.13 um SOI Model.

Model Target:

Accuracy:  \( \Delta V_{tlin} < 5 \text{mV}, \quad \Delta I_{dsat} < 2\% \)

Physical:  Cover most physical effects (FBE/SHE)

Scalable:  Model QA pass from Wmax/Lmax to Wmin/Lmin

Convergence:  We have successfully simulated ring oscillator

<table>
<thead>
<tr>
<th>Device</th>
<th>( \Delta V_{tlin} )</th>
<th>( \Delta I_{dlin} )</th>
<th>( \Delta I_{dsat} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target</td>
<td>&lt;5mV</td>
<td>&lt;3%</td>
<td>&lt;3%</td>
</tr>
<tr>
<td>TB Core</td>
<td>&lt;5mV</td>
<td>&lt;1%</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>FB Core</td>
<td>&lt;5mV</td>
<td>&lt;1%</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>TB IO</td>
<td>&lt;5mV</td>
<td>&lt;2%</td>
<td>&lt;2%</td>
</tr>
<tr>
<td>FB IO</td>
<td>&lt;5mV</td>
<td>&lt;2%</td>
<td>&lt;2%</td>
</tr>
</tbody>
</table>
**Ring Oscillator Results**

- We have designed ring oscillator for the verification of SOI Model. As shown in the table, the simulation error is less than 10%.

<table>
<thead>
<tr>
<th>Ring Oscillator</th>
<th>Wp/Wn</th>
<th>Lp/Ln</th>
<th>FO</th>
<th>FF</th>
<th>Simulation Delay</th>
<th>Test Delay</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2V_FB_INV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.13/0.13</td>
<td>1  6</td>
<td>19.3</td>
<td>18.9</td>
<td>1.9%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2/1</td>
<td>0.13/0.13</td>
<td>1  6</td>
<td>21.7</td>
<td>21.8</td>
<td>-0.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.13/0.13</td>
<td>3  5</td>
<td>40.4</td>
<td>38.7</td>
<td>4.5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2V_TB_INV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.13/0.13</td>
<td>1  6</td>
<td>25.6</td>
<td>25.1</td>
<td>2.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2/1</td>
<td>0.13/0.13</td>
<td>1  6</td>
<td>29.2</td>
<td>29.7</td>
<td>-1.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.13/0.13</td>
<td>3  5</td>
<td>52.8</td>
<td>50.2</td>
<td>5.3%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.3V_FB_INV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.30/0.35</td>
<td>1  6</td>
<td>41.1</td>
<td>39.9</td>
<td>3.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2/1</td>
<td>0.30/0.35</td>
<td>1  6</td>
<td>45.2</td>
<td>44</td>
<td>2.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.30/0.35</td>
<td>3  5</td>
<td>88.8</td>
<td>86.3</td>
<td>2.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.3V_TB_INV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.30/0.35</td>
<td>1  6</td>
<td>41.9</td>
<td>44</td>
<td>-4.6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2/1</td>
<td>0.30/0.35</td>
<td>1  6</td>
<td>47.3</td>
<td>49.8</td>
<td>-4.9%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3/2</td>
<td>0.30/0.35</td>
<td>3  5</td>
<td>95.4</td>
<td>99.5</td>
<td>-4.1%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RF MOSFET

- We have designed RF test structure of SOI MOSFETs.
- The peak cutoff frequency \(f_T\) and maximum oscillation frequency \(f_{\text{MAX}}\) of TB Ncore are 87 and 75 GHz.

\[\text{Core: } \text{FB Ncore, FB Pcore, TB Ncore, TB Pcore; }\]
\[\text{IO: } \text{FB NIO, FB PIO, TB NIO, TB PIO; }\]
\[\text{Finger: } 4, 20, 60, 120;\]

\[W=5 \text{um}, L=0.13 \text{um}, nf=20\]

\(f_T\) characteristics of SOI Ncore device

\(f_{\text{MAX}}\) characteristics of SOI Ncore device
We have designed Inductor test structure.

The peak of Q factor is 16 in standard inductor with \( N=5.5, \ W=9\mu m, \ S=2\mu m, \ D=255\mu m \).

RF characteristics of 0.13\,\mu\text{m} SOI standard Inductor with \( N=5.5, \ W=9\mu m, \ S=2\mu m, \ D=255\mu m \).
We have extracted RF Device Model for 0.13 um SOI Technology.

**Device**
- MOS (TB, HB), Inductor, Resistor, Varactor, MIM, MOM

**Level**
- 70 (BSIM4SOI)

**Effects**
- FBE/GIFBE, SHE, Gate-leakage, GIDL

**Geometry**
- Core: L[0.13~0.75um], W[1.5~8um]
- IO: L[0.35~0.75um], W[1.5~8um]

**Temp.**
- -55~125°C

**Voltage**
- Gate: [-1.32~1.32V](core) / [-3.63~3.63V](IO)
- Drain: [0~1.32V](core) / [0~3.63V](IO)

**Corner**
- TT, FF, SS, FS, SF

Simulation result of RF NMOS
0.13 um SOI model was applied to SOI Library and ASIC circuit design.
The model has become an important part of 0.13 um SOI technology platform, which provides a powerful guarantee for the SOI high reliability circuit design.

ASIC Chip Verification

<table>
<thead>
<tr>
<th>Chip Parameters</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Working Frequency</td>
<td>50Mhz</td>
</tr>
<tr>
<td>Chip Scale</td>
<td>&gt; 2M gates</td>
</tr>
<tr>
<td>Chip Area</td>
<td>8mm x 9mm</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>250mA</td>
</tr>
</tbody>
</table>
**Novel Body Contact Structure**

- TDBC SOI devices without floating-body effects are successfully demonstrated, which represent an improvement of 10% for the $f_T$ and of 90% for the $f_{MAX}$ compared with conventional T-gate body-contact devices.

![Graph showing Drain Current vs Drain Voltage](image1)

- Drain Current, $I_D$ (mA)
- Drain Voltage, $V_D$ (V)
- $W/L=10\mu m/0.13\mu m$
- PD SOI nMOSFET

![Graph showing fT and fMAX vs VGS-VTH](image2)

- $f_T$ (GHz)
- $f_{MAX}$ (GHz)
- $V_{GS-VTH}$ (V)
- FB, TB, TDBC

Kink are perfectly suppressed in TDBC devices

Superior RF performance of TDBC devices

TDBC contact makes these SOI transistors strongly resistant to back channel radiation effects.

**Total Dose Effects of TDBC Device**

- Cooperated with E. X. Zhang and D. M. Fleetwood, Vanderbilt University, USA

**Jiexin Luo, Jing Chen et al.,** *IEEE Transaction on Nuclear Science,* 61(6), 11, 2014
We have experimentally demonstrated a novel capacitorless DRAM cell named FBGC on planar SOI CMOS technology.

FBGC has large noise margin and long retention time, also shows excellent endurance nondestructive read characteristics and low-power operation.

FBGC has large noise margin (26.5 \mu A/\mu m) and long retention time (560 ms)

Cooperated with Zhichao Lu and Jerry G. Fossum, University of Florida, USA

Qingqing Wu, Jing Chen et al., IEEE Electron Device Letters, 33 (6), 743, 2012
SOI LDMOS devices was successfully fabricated, the off-state breakdown voltage can reach to 750V.

Siemens Photonics

◆ It is expected to find applications in designing compact optical components to achieve the on-chip beam steering in photonic circuits.

Physical Review Letters (2011.5.20), Editor’s Suggestion

Sharp turn ahead for light beams

Optical Beam Steering Based on the Symmetry of Resonant Modes of Nanoparticles
Junjie Du, Zhifang Lin, S. T. Chui, Wanji Lu, Hao Li, Aimin Wu, Zhen Sheng, Jian Zi Xi, Wang Shichang Zou, and Fuwan Gan
Phys. Rev. Lett. 106, 203903 (Published May 20, 2011)

APS special reported

10Gbps transfer speed
High-K SiGe/SOI quantum well

- Epitaxial growth of strain silicon substrates was achieved via an Al interlayer mediated epitaxial. The hole mobility is 2.5X larger than Bulk channel.

- Coated with Juelich Research Center, Germany

- sSi/sSiGe/sSOI substrate
- Carries are confined in sSiGe
- 2.5X larger than Bulk channel

Cooperated with Juelich Research Center, Germany

- Bo Zhang et al., *Solid-State Electronics*, 62(1), 185, 2011
Nanowire on SOI

- SSRM has been used to characterize doping in silicon nanowire for the first time. The GAAC FinFET appears to be a good potential candidate for scaling down to sub-10 nm sizes.

- Perfect structure with gate all-rounded
- Easy to implement on SOI

SSRM (Scanning Spreading Resistance Microscopy)

- Nanowire on Hybrid orientation SOI

- Xin Ou et al., *Advanced Materials*, 22(36), 4020, 2010
- Xiao Deyuan et al., *Journal of Semiconductors*, 30(1), 2009
- Xin Ou et al., *Nano Letters*, 10(1), 171, 2010

Cooperated with Forschungszentrum Dresden-Rossendorf, Germany
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- Research results
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  - RF Device Model
  - Research of SOI Device
  - Fruits of international cooperation
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**Summary**

- **SOI Group**
  - The leading SOI research teams in China are actively driving new SOI technology development, help to build up SOI ecosystem.

- **Device Modeling**
  - We have extracted a complete Model for 0.13 um SOI technology, which was applied to SOI Library and ASIC circuit design.

- **Research of SOI Device**
  - We have designed TDBC SOI device, FBGC Cell, LDMOS, Nanowire, Silicon photonics integrated chip, and so on.

- **International cooperation**
  - We have fruits of international cooperation with some famous university in USA and Research Centers in Germany.
Thank you!