The Critical Role of Quantum Capacitance in Compact Modeling of Nano-Scaled and Nanoelectronic Devices

Zhiping Yu and Jinyu Zhang

Institute of Microelectronics
Tsinghua University, Beijing, China

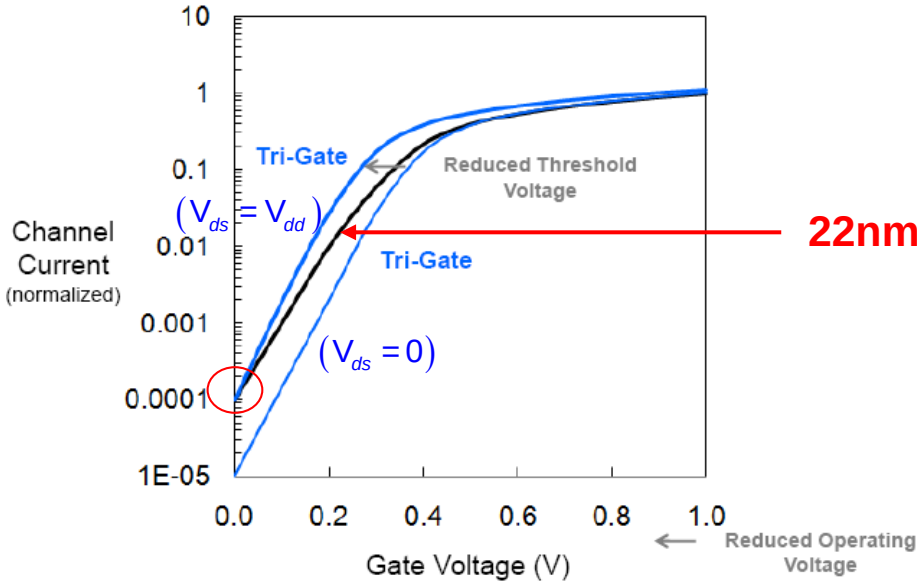
yuzhip@tsinghua.edu.cn

Outline

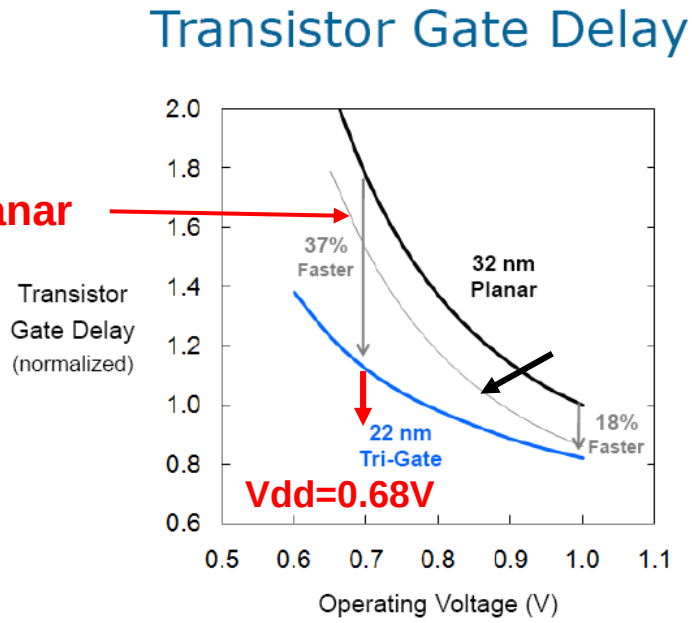
- The major concerns near the end of MOS scaling
- What is quantum capacitance (QC) and why has it mostly been ignored in FET compact modeling?
- Modeling and equivalent circuits for QC
- Carbon-NanoTube FET (CNT-FET), a classical Example for illustrating QC
- Compact model for Graphene FET (GFET) and its application in design of a distributed amplifier
- Conclusions

Driving Force for Further MOS Scaling

- It's low power, low voltage, and low gate delay (power-delay product)
- From planar to FinFET, and from tunneling FET to novel nano-electronic devices (new channel materials)

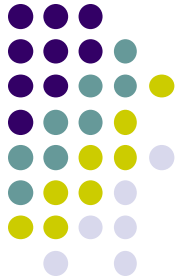


22nm planar



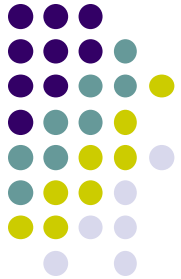
Source: Bohr/Mistry slides, May 2011

Important Means to Further MOS Scaling



- New device structures
  - Gate-All-Around Nanowire (GAA-NW) FETs
  - Tunneling FETs (tFETs)
  - Junctionless (JL) FETs
- New channel materials
  - III-V CMOS, e.g., InAs for nMOS and GaSb for pMOS on GaAs substrate
  - 2D materials, typical graphene, and emerging MoS_2, WSe_2, black phosphorous (BP), etc.
  - 1D materials, mainly carbon nanotube (CNT)

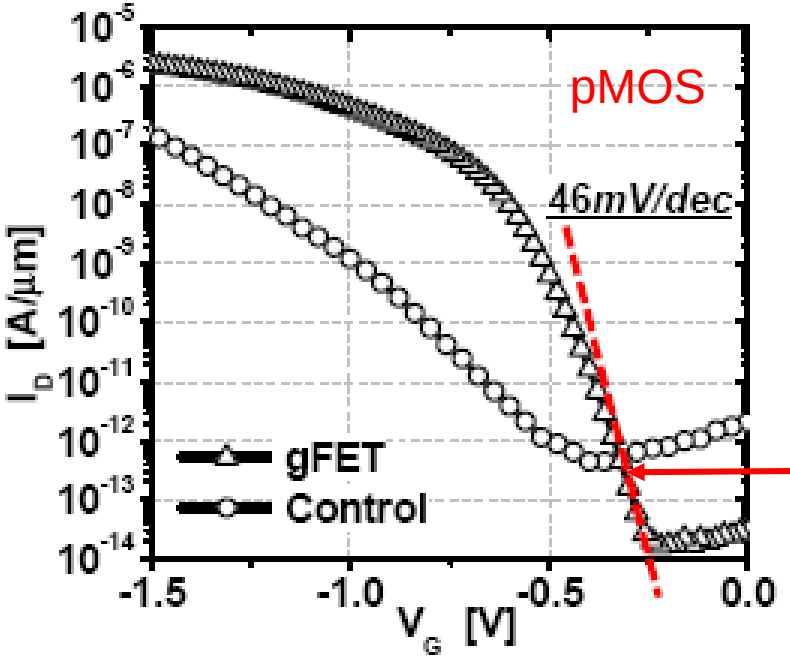
Critical Device/Material Parameters to Look At

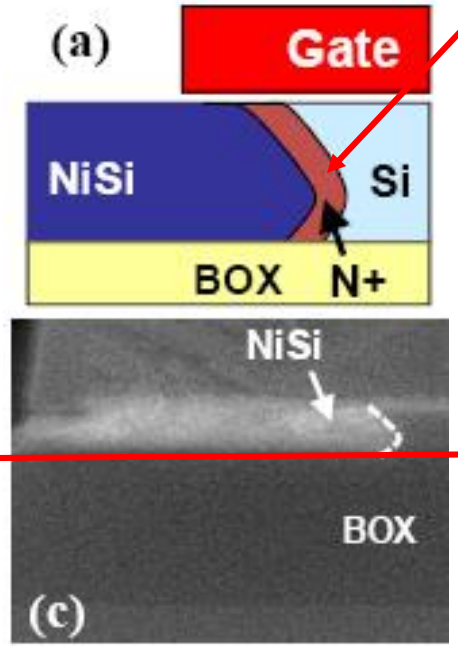


- Devices
  - Subthreshold swing (SS): break through the 60mV/dec limit
  - I_{on} and I_{on}/I_{off} ratio
  - Off-state leakage (drain controllability over gate)
- Channel materials
  - Mobility
  - Density of States (DOS)

Tunneling FETs and Small SS

- K. Jeon, SEMATECH/UCB, *VLSI* '10





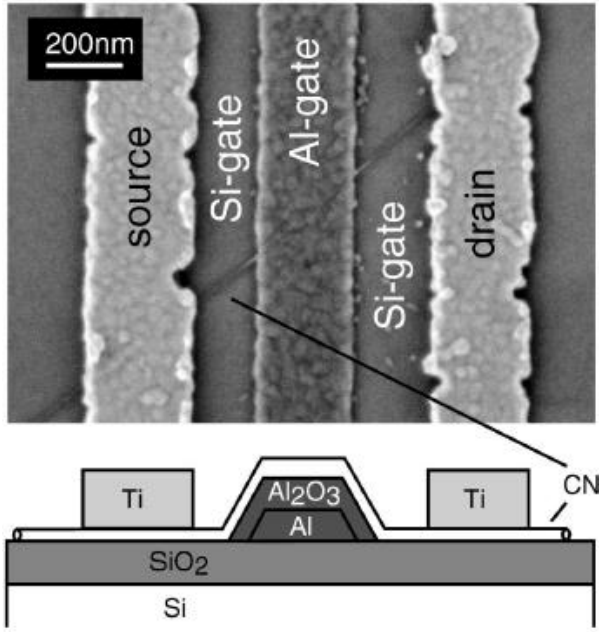
source side

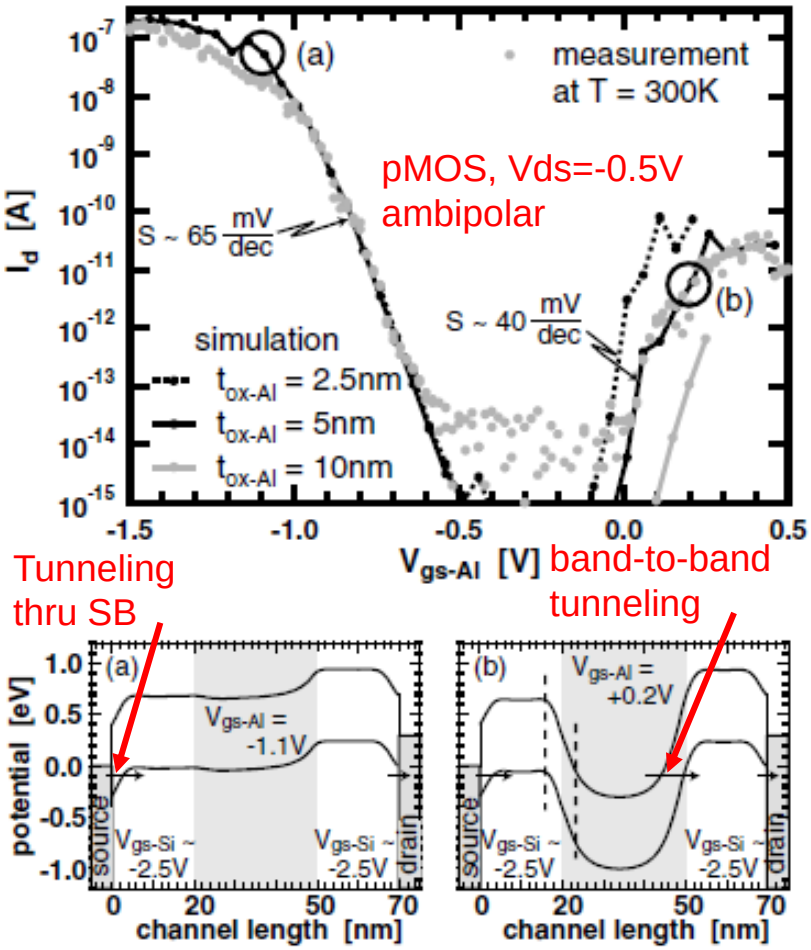
Features:

- **I_{on}/I_{off}: 10^8**
- **n-i-p on 40nm BOX**
- **NiSi source structure**
- **High field pocket**
- **Recessed source-side silicon**
- **SS<60 mV/dec for 3-decades of I_D**

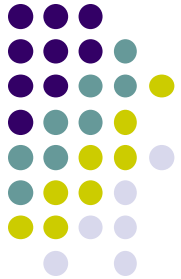
CNT-FET and Small Gate Delay

- J. Appenzeller, IBM, *PRL* '04





Why Need to Model Quantum Capacitance (QC)



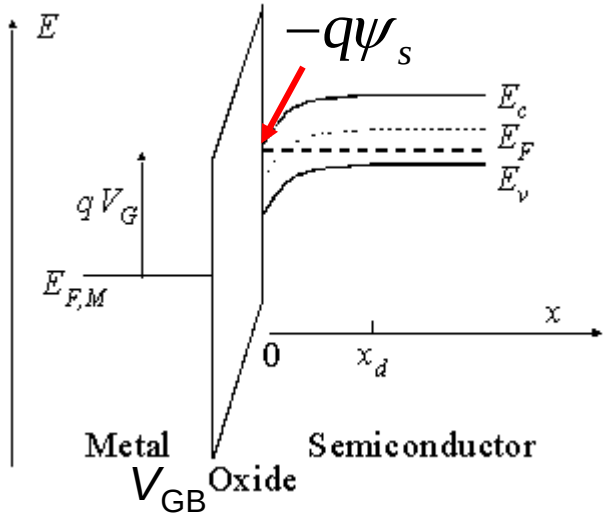
- An accurate total (and especially the intrinsic) gate capacitance is important in evaluating the transistor performance (gate delay, say)

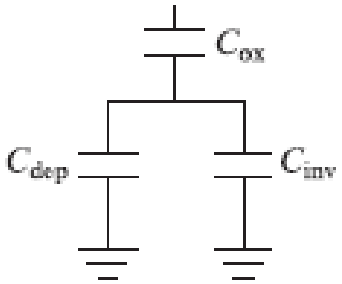
$$\tau_{\text{delay}} = C_{\text{gate}} V_{\text{dd}} / I_D$$

- Channel materials are assessed for both mobility and density-of-states (DOS), often there is a trade-off (high μ implies low DOS)
- Nano-electronic (and gate-all-around) devices don't have body contact to their channel.

QC Is Not New: MOS Capacitor Has DOS Capacitance

Having bulk contact to channel





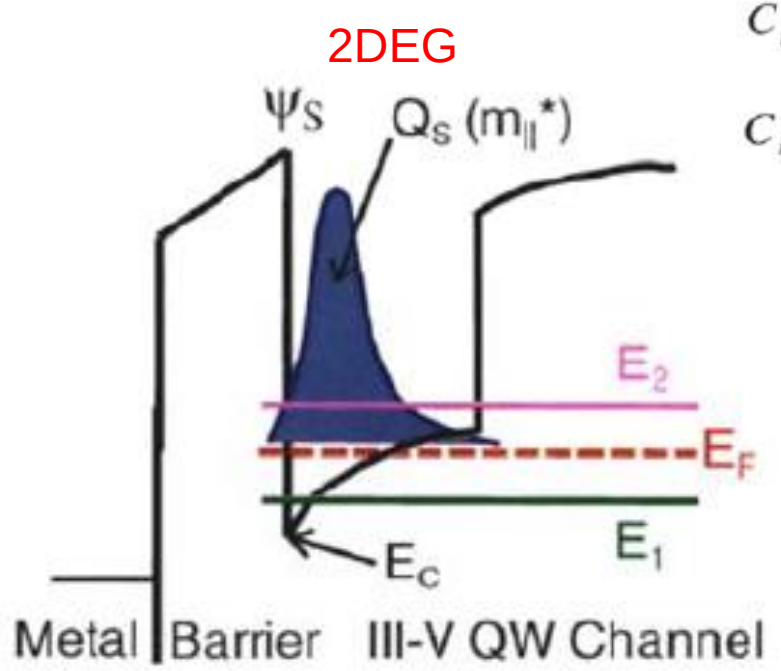
$$Q_{\text{inv}} = q\int n(x)\,dx,\ C_{\text{inv}} = \frac{\partial Q_{\text{inv}}}{\partial \psi_S}$$

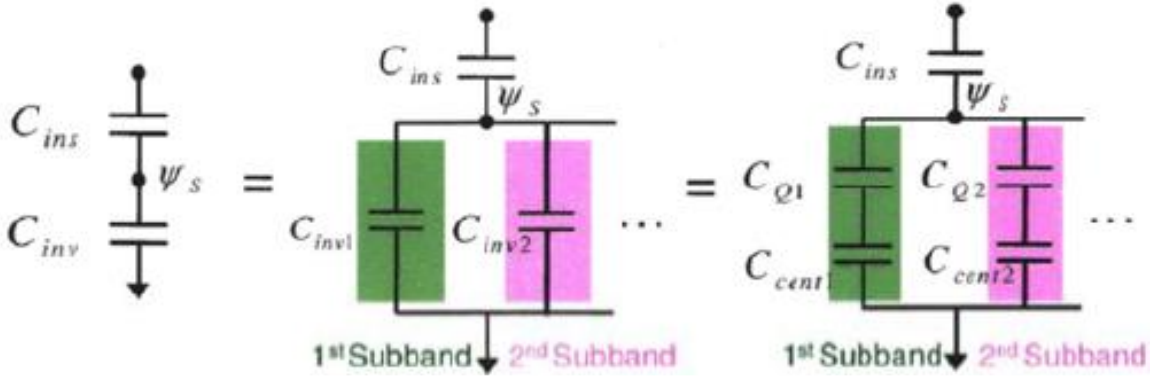
$$n = n_i e^{(\psi-\phi_F)/V_t} = N_C e^{(E_F-E_C)/k_BT}$$

$$n_i = \sqrt{N_C N_V}\, e^{-E_g/2k_BT}$$

Then, Why Quantum (Capacitance)?

- First coined by S. Luryi of Bell Labs, *APL* ’88 for 2DEG





$$C_{Qi} = \frac{q^2 m_{||}^* / (\pi\hbar^2)}{1 + e^{(E_i - E_F)/k_B T}}$$

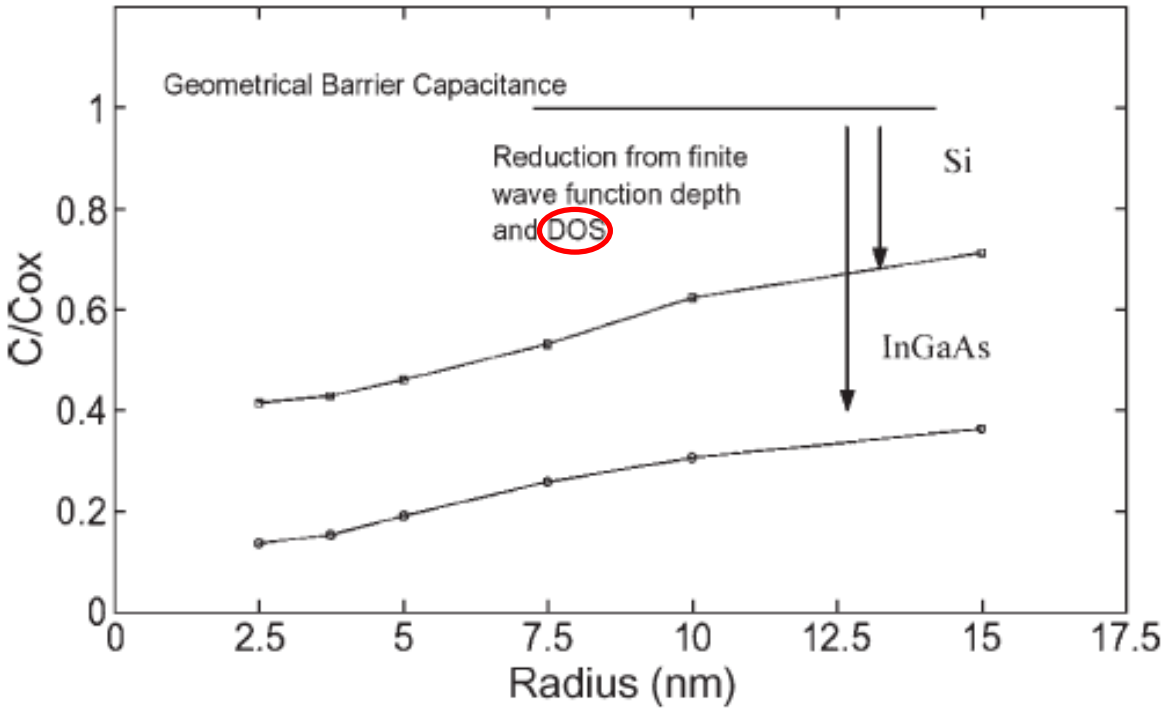
← 2D DOS

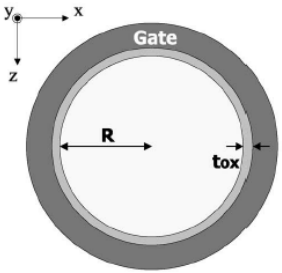
e.g., $m^*=0.98m_0$ for Si m_l

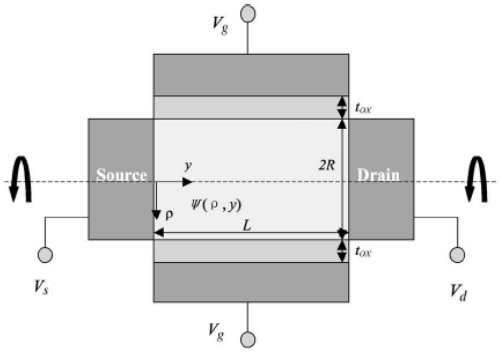
D. Jin, MS thesis, MIT, 2010

Impact of Quantum Capacitance

- B. Yu, UCSD, *T-ED*, '08



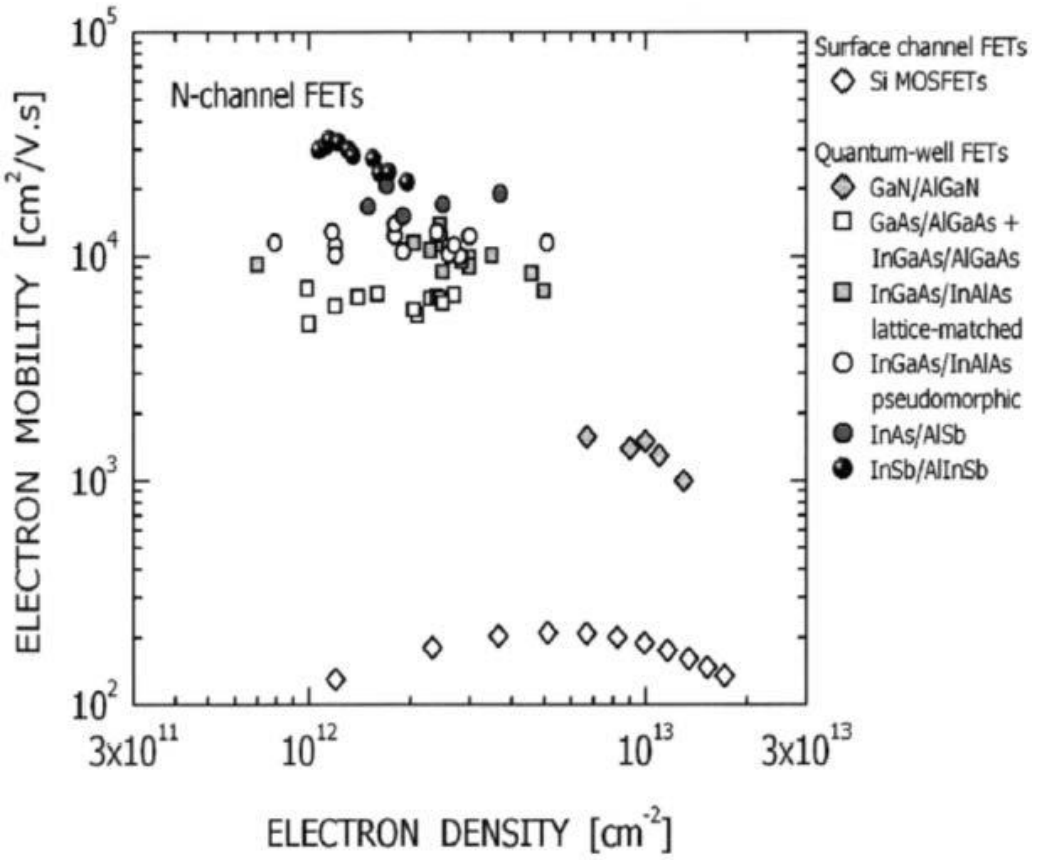




Effective Mass of DOS for Different Semiconductors

G. Jin, MIT, MS Thesis, ’10

- Si: 1.08 m_0
- GaAs: 0.067 m_0
- InAs: 0.026 m_0
- $In_{0.53}Ga_{0.47}As$: 0.04 m_0



DOS Dependence on Electronic Energy for 1/2/3D

$$D_1(E) = \frac{1}{\sqrt{c_k (E - E_0)}}$$

1D

$$D_2(E) = \frac{\pi}{c_k}$$

$$D_3(E) = 2\pi \sqrt{\frac{E - E_0}{c_k^3}}$$

2D

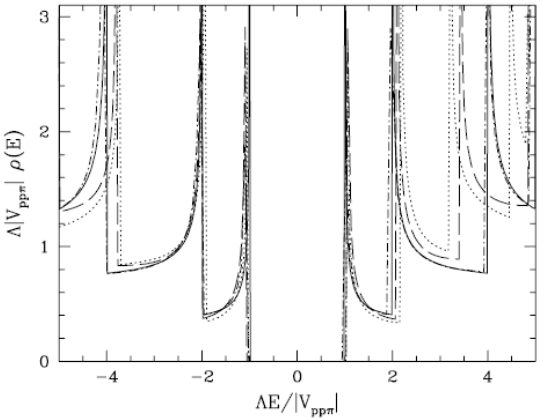
$$N_{3D}(E) = \frac{V}{2\pi^2} \left(\frac{2m^*}{\hbar^2} \right)^{3/2} \sqrt{E - E_0}$$

c_k in dispersion relation of $E = E_0 + c_k k^p$

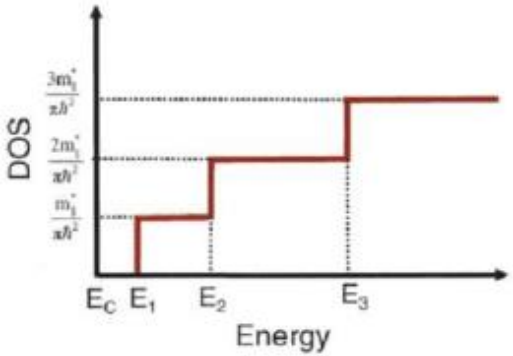
and p is the power of k,

e.g., $p = 2$ for parabolic

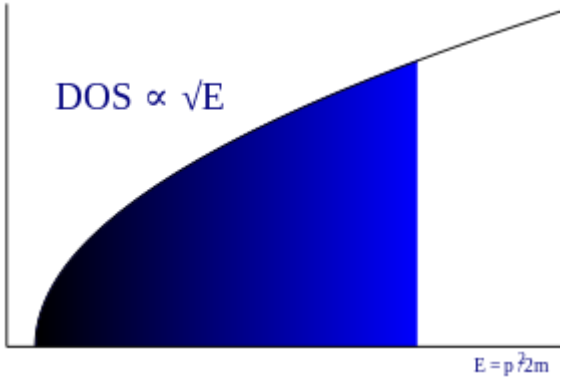
3D



J. Mintmire
PRL '98



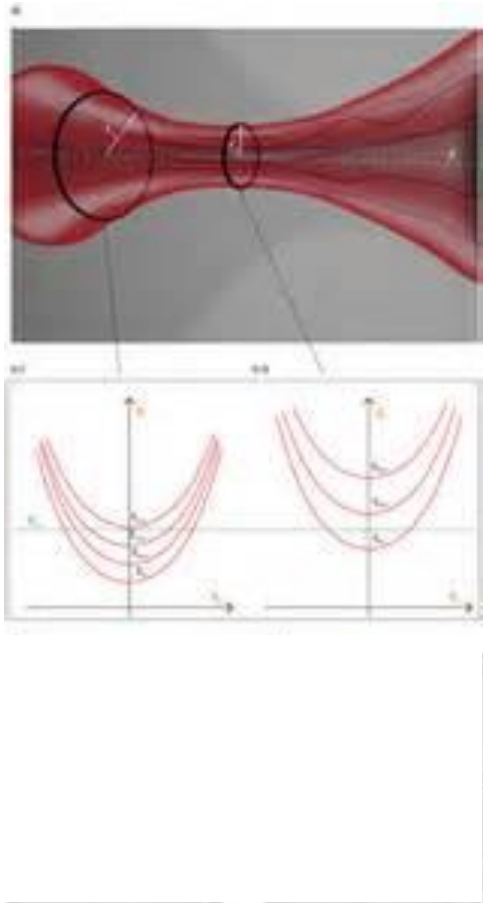
D. Jin
MIT MS
Thesis '10



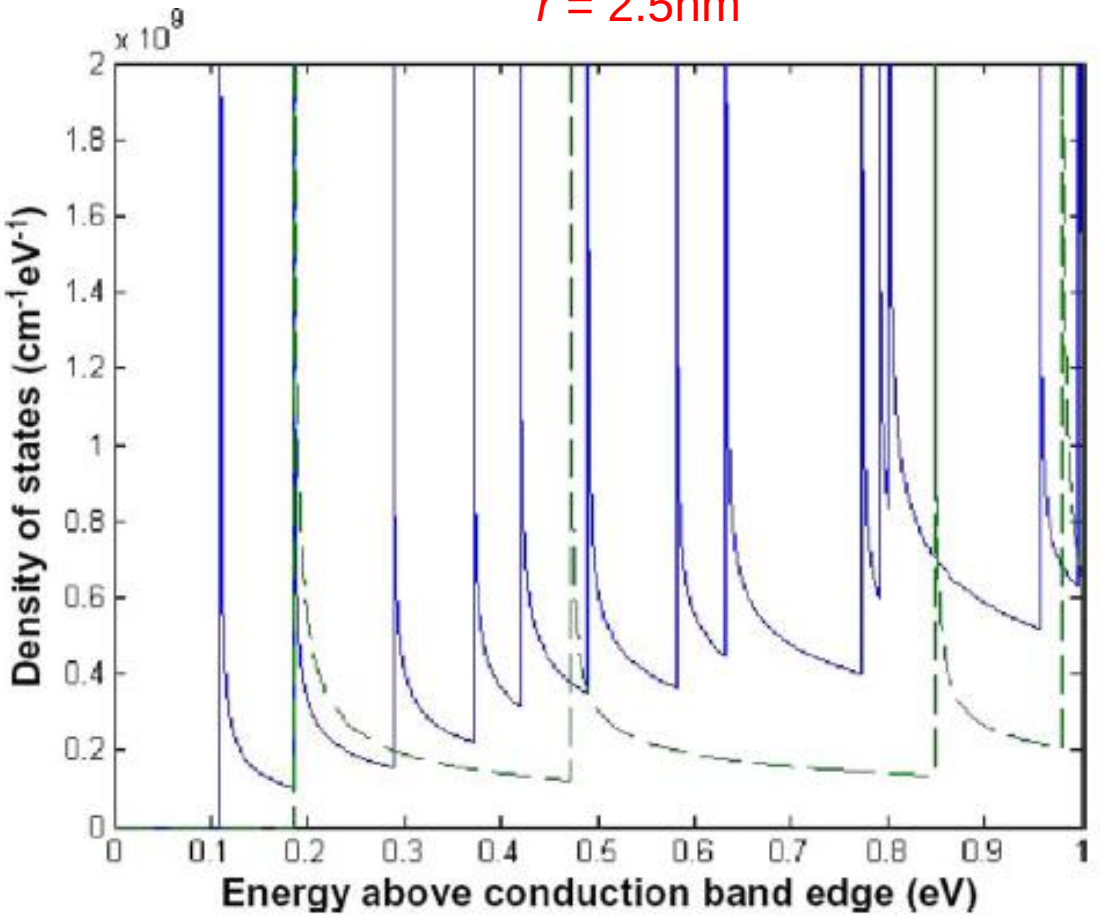
Wiki

DOS for Nanowire

- B. Yu, UCSD, *T-ED* ‘08

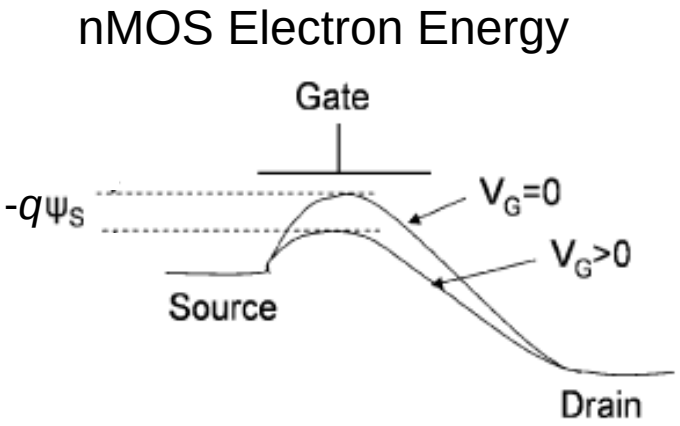


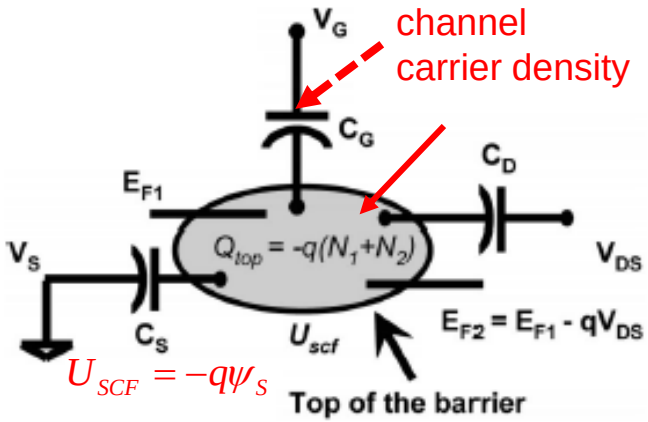
Si nanowire of
r = 2.5nm

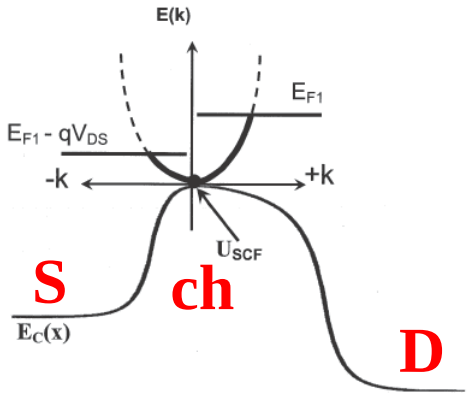


Quantum Capacitance (QC): Modeling Approach

Ballistic transport assumption: provide knowledge of Fermi level in channel





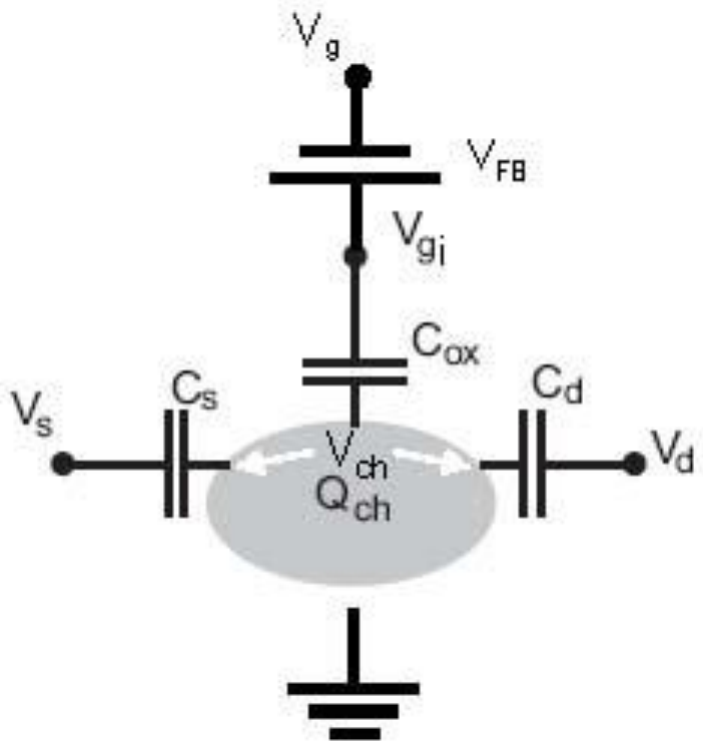


A. Raychowdhury, *T-ICCAD* '04

A. Rahman, *T-ED* '04

Definition of QC: C_q

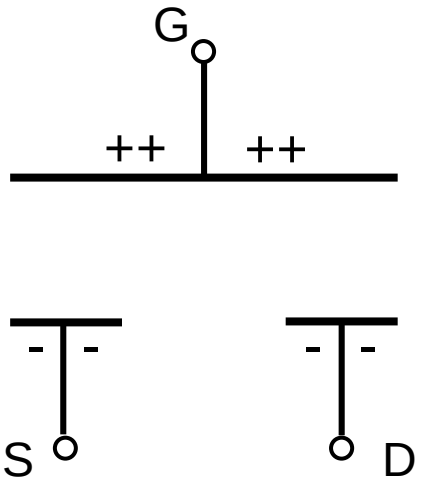
$$C_q = -\frac{dQ_{\mathrm{ch}}}{dV_{\mathrm{ch}}}$$



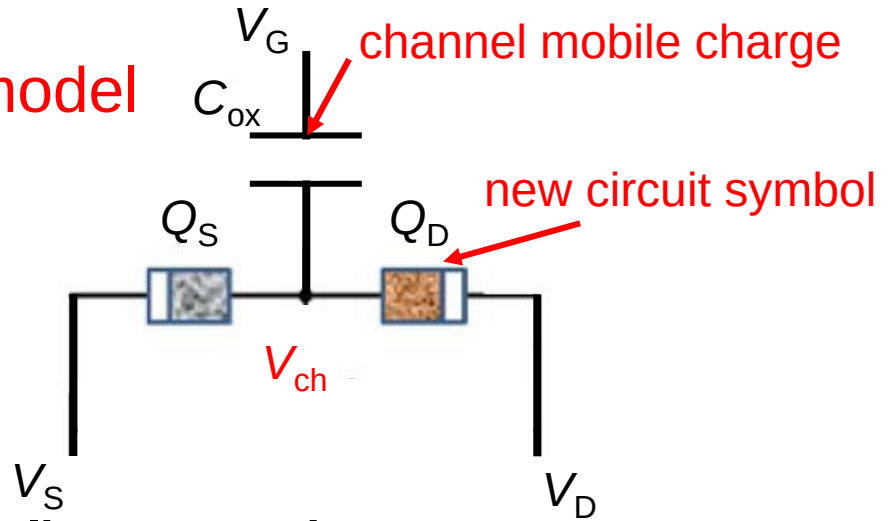
QC (cont'd): Equivalent Circuit

- Use charge balance principle to find V_{ch}:

$$-C_{ox} \times (V_G - V_{ch}) = Q_S (V_{ch} - V_S) + Q_D (V_{ch} - V_D)$$



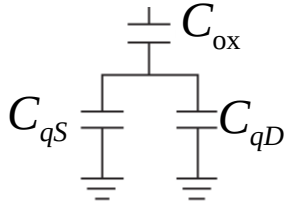
large signal model



- Incremental (small signal) capacitance network

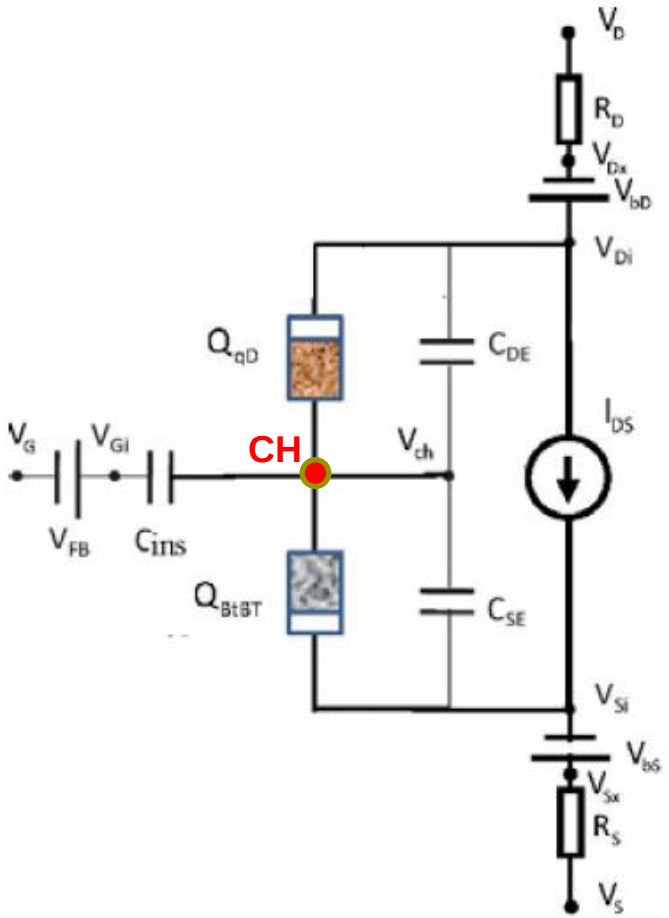
q for quantum

$$\delta V_{ch} = \frac{C_{ox}}{C_{ox} + C_{qS} + C_{qD}} \delta V_G, \; C_{qS} = \frac{\delta |Q_S|}{\delta V_{ch}}, \; C_{qD} = \frac{\delta |Q_D|}{\delta V_{ch}}$$

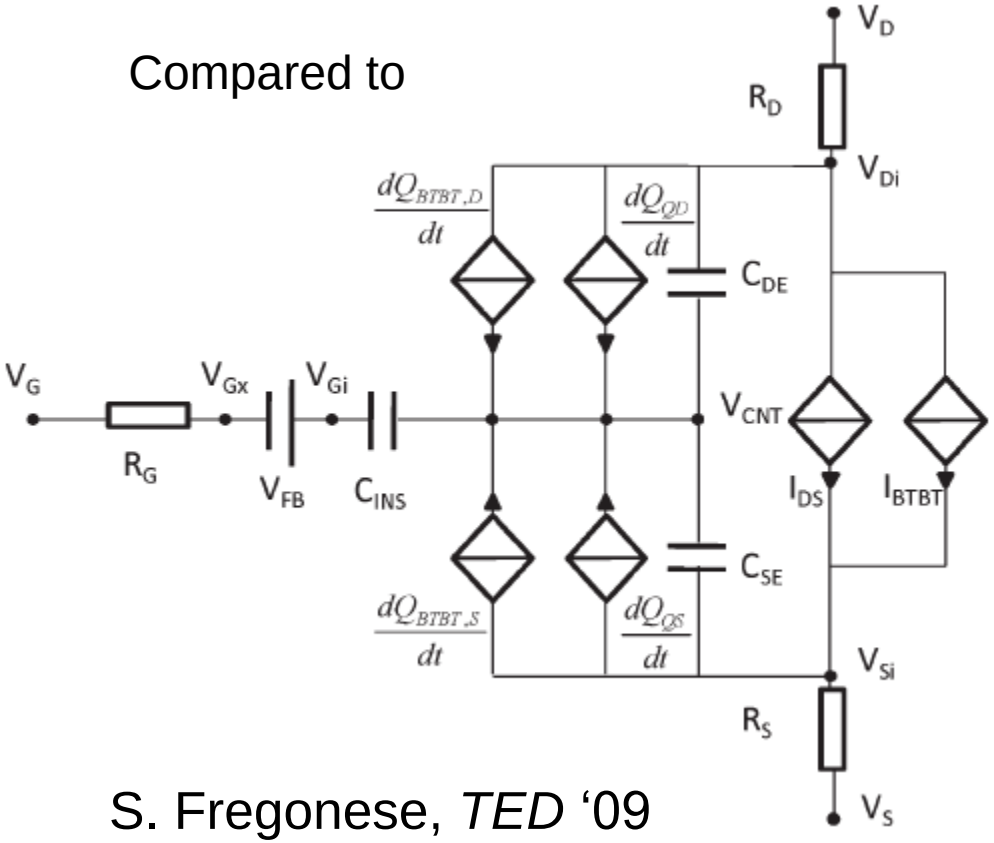


Application of QC to tFET

- Z. Yu, Tsinghua, *ICSICT* ‘12



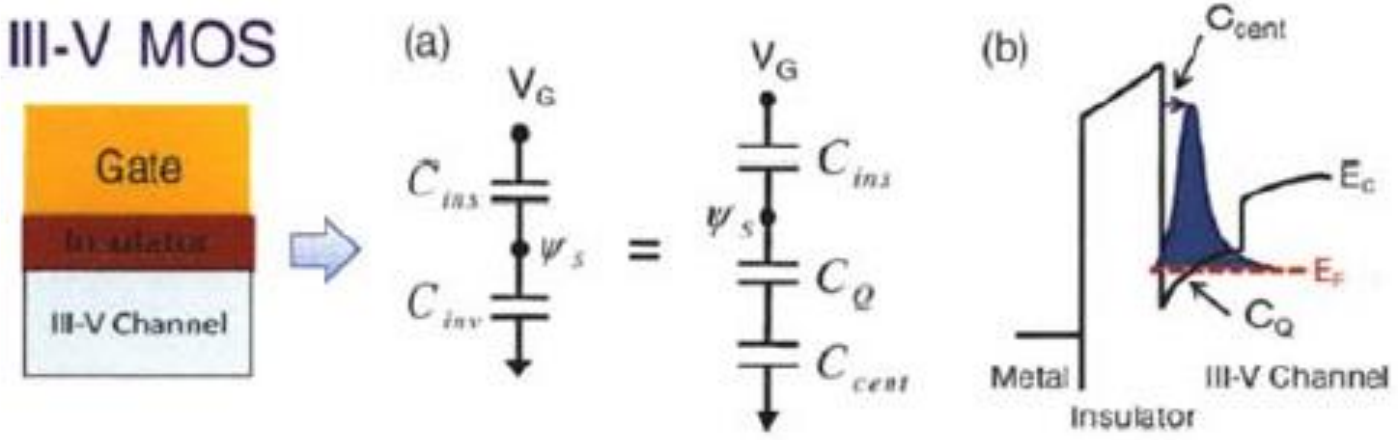
Compared to



S. Fregonese, *TED* ‘09

Quantum Capacitance in III-V FETs

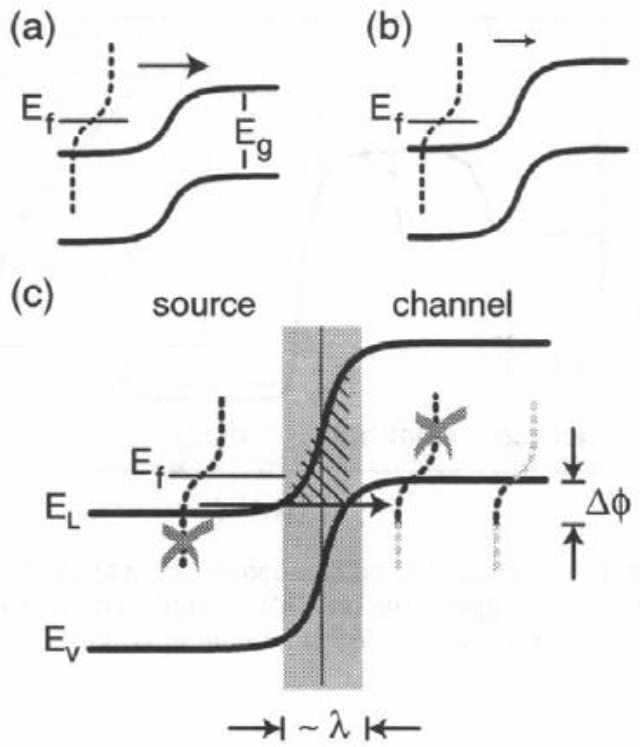
- D. Jin, MS thesis, MIT, 2010



$$\left[\frac{q\partial|Q_i|}{\partial(E_F-E_C)}\right]^{-1}=\left[\underbrace{\frac{q\partial|Q_i|}{\partial(E_F-E_i)}}_{C_{Qi}}\right]^{-1}+\left[\underbrace{\frac{q\partial|Q_i|}{\partial(E_i-E_C)}}_{C_{\text{cent},\,i}}\right]^{-1}$$

Thermal Emission vs. Band-to-Band Tunneling (BtBT): Band-Pass Filtering

- Now, consider using BtBT to improve SS



J. Knoch, IBM, *DRC* '05

$$T(E) = \text{const} = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar\mathrm{E}}\right)$$

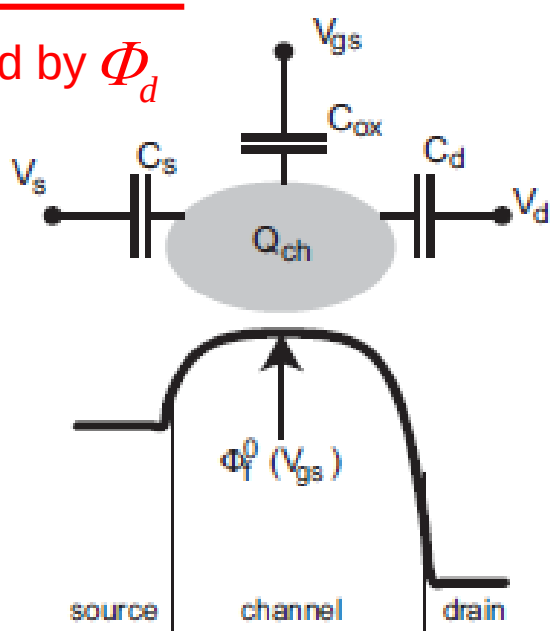
$$\mathrm{E} = \left(E_g + \Delta\phi\right)/\lambda,\ \lambda = \sqrt{\frac{\varepsilon_{\text{cnt}}}{\varepsilon_{\text{ox}}} t_{\text{ox}} t_{\text{cnt}}}$$

SCE: Short-Channel Effect

- J. Knoch, IBM Zurich Lab, *Phys. Stat. Sol.* ’08

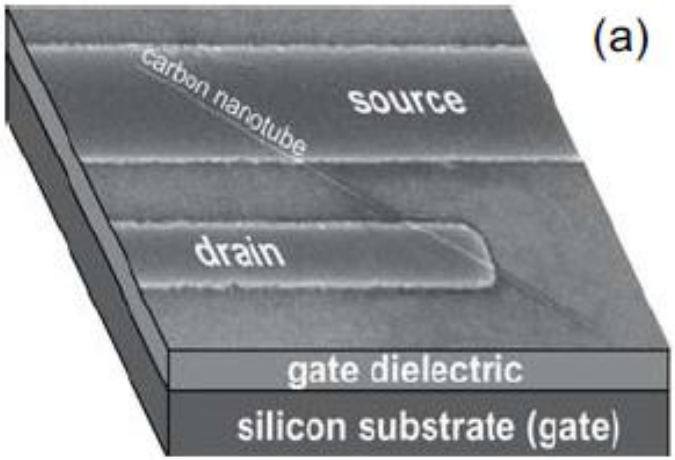
Φ_f^0 is influenced by Φ_d

- Look for
  - gate control
  - drain control (DIBL)
  - long channel or SCE: *L* vs. λ

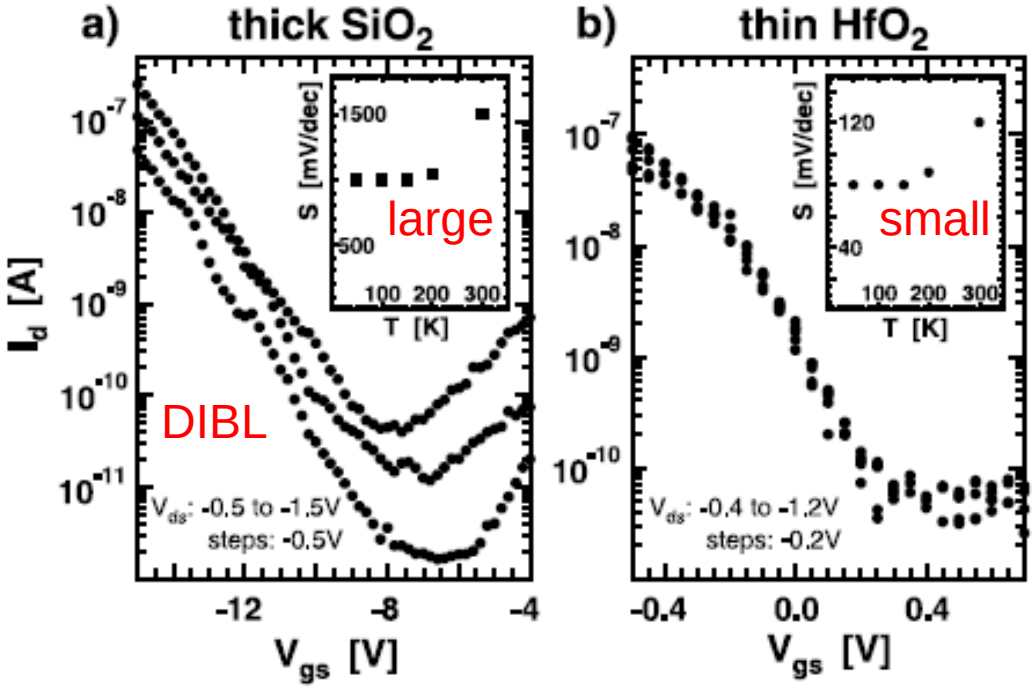


SS of CNT-FET as a Function of t_{ox}: a Measure of Gate Controllability

- J. Appenzeller, IBM, *PRL* '02 pMOS



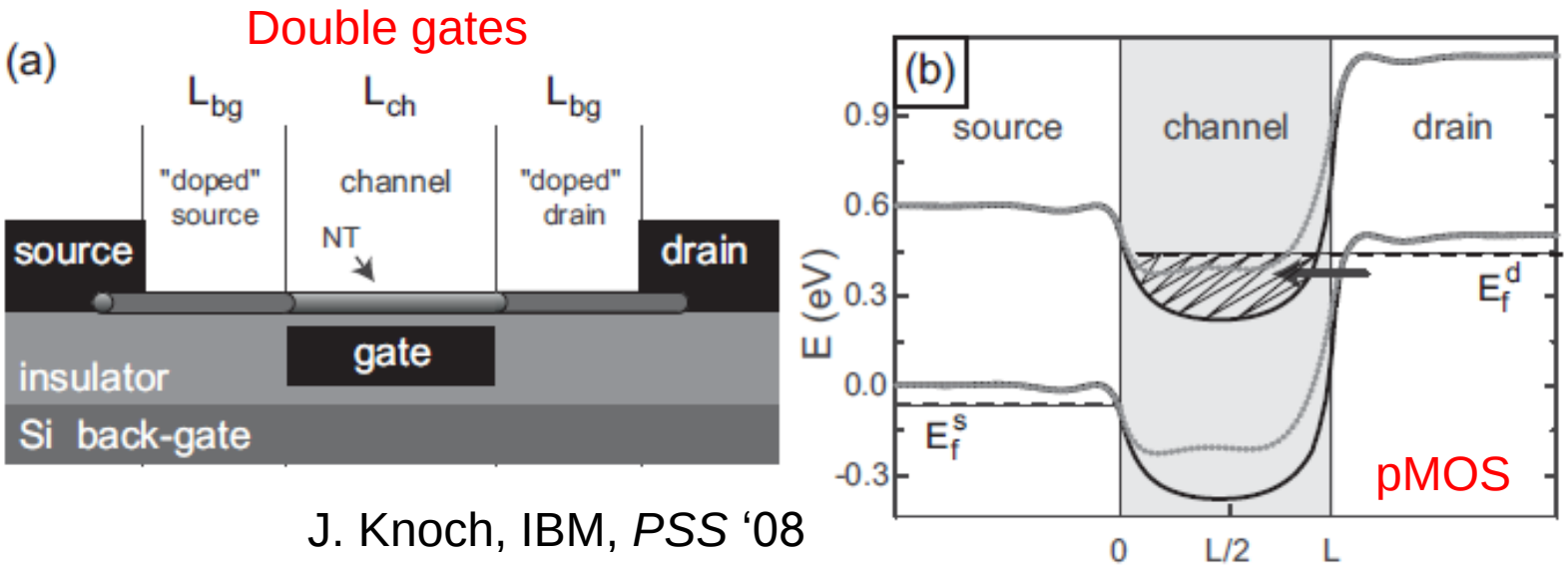
J. Knoch, IBM Zurich, *PSS* '08



120nm SiO_2 20nm HfO_2

Charge Pile-up in Channel of CNT-FET through BtBT

- J. Appenzeller, IBM, *PRL* ‘04 (both experiment and simulation by NEGF)
- S. Fregonese, U Bordeaux, *T-ED,* ‘09



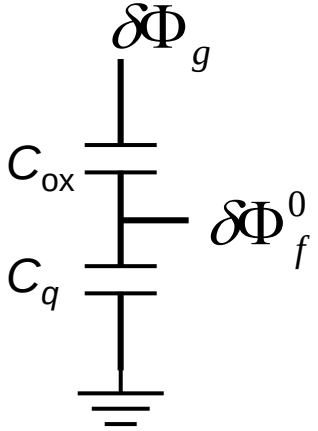
J. Knoch, IBM, *PSS* ‘08

Dual Forces in Controlling Channel Potential: from Gate and Drain Terminals

- J. Knoch, IBM, *PSS* '08

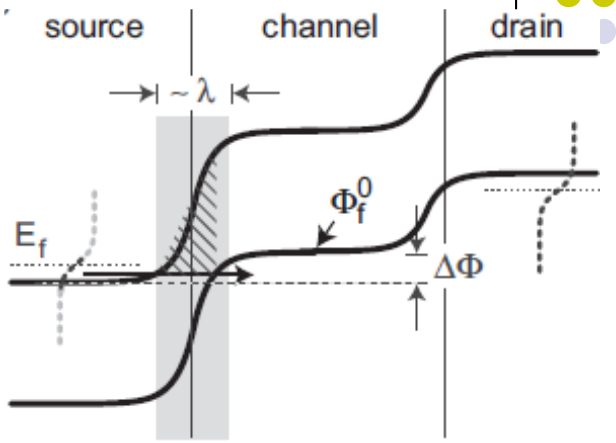
$$C_q = \frac{2}{h}\sqrt{\frac{8m^*}{\Phi_f^0 - E_f^d}}$$

$$\delta\Phi_f^0 = \frac{C_{\text{ox}}}{C_{\text{ox}} + C_q + C_d}\delta\Phi_g + \frac{C_q + C_d}{C_{\text{ox}} + C_q + C_d}\delta\Phi_d$$



- For an electrostatically well-designed device at off-state $C_{\text{ox}} \gg C_q,\ C_d$
- QCL: quantum capacitance limited $C_{\text{ox}} \gg C_q$

Advantage of 1D Transport for CNT-FET



- J. Knoch, IBM, *PSS* '08

$$C_{q,\,\mathrm{BtBT}} = \frac{\partial Q_{\mathrm{BtBT}}}{\partial \Phi_f^0} \approx$$

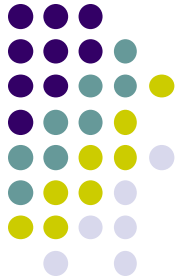
$$\frac{4\lambda\sqrt{2m^*}E_g^{3/2}}{3\hbar\left(E_g + \Delta\Phi\right)} T_{\mathrm{WKB}} \int dE\; D(E)\left[1 - f\left(E - E_f^S\right)\right]$$

$$+qT_{\mathrm{WKB}} \frac{\partial}{\partial \Phi_f^0} \int dE\; D(E)\left[1 - f\left(E - E_f^S\right)\right]$$

$C_{q,\,\mathrm{BtBT}} \propto T_{\mathrm{WKB}}$ and $I_D \propto T_{\mathrm{WKB}}$

resulting in τ_{delay} independent upon T_{WKB}

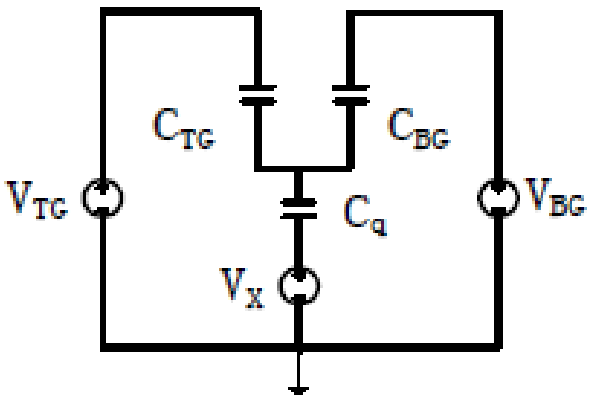
Dilemma of QCL Regime

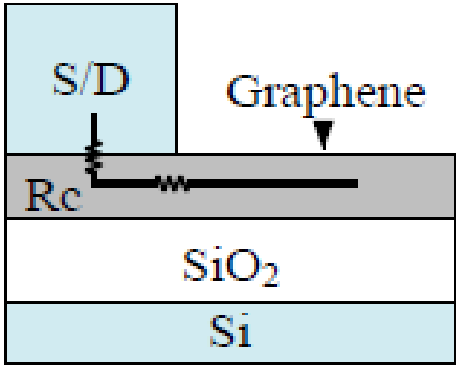


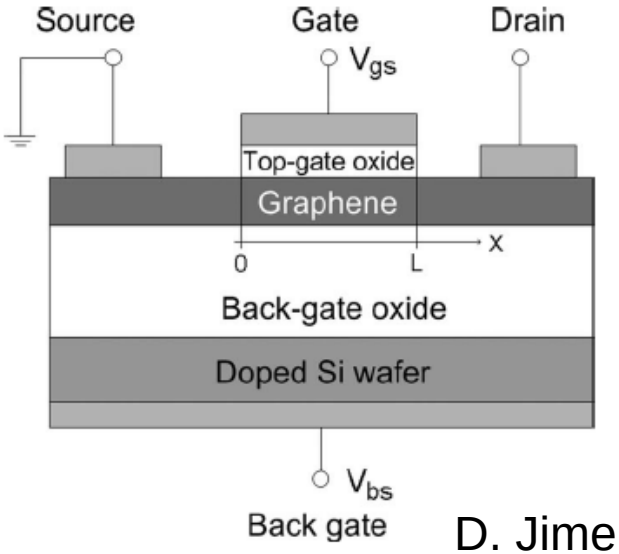
- Gate control is good (channel potential closely follow the gate bias), meaning small SS
- Yet, the total gate capacitance becomes small, which implies small on current
- There may be some optimization scheme for minimizing the gate delay
- Similar situation for JL-FETs

Compact Model for GFET

- W. Zhu, Tsinghua, *SISPAD* ’12





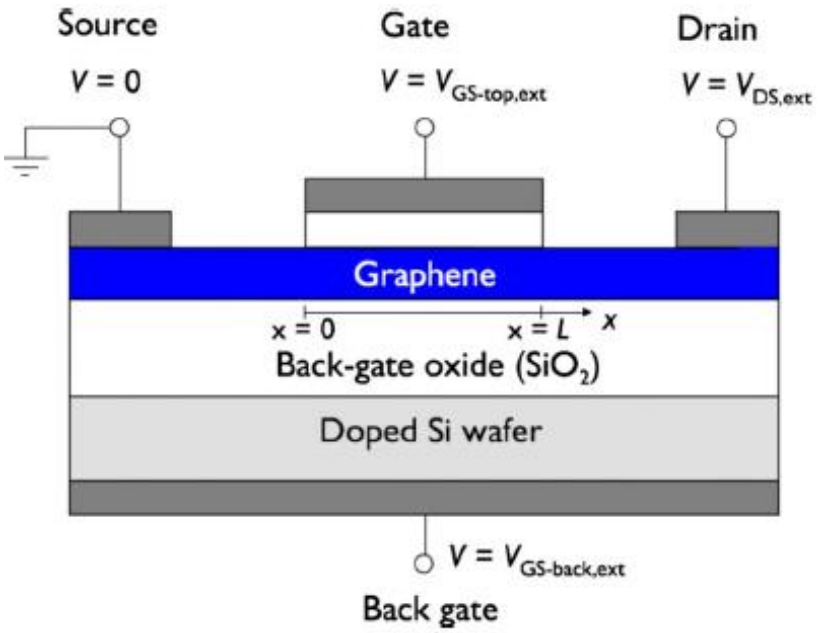


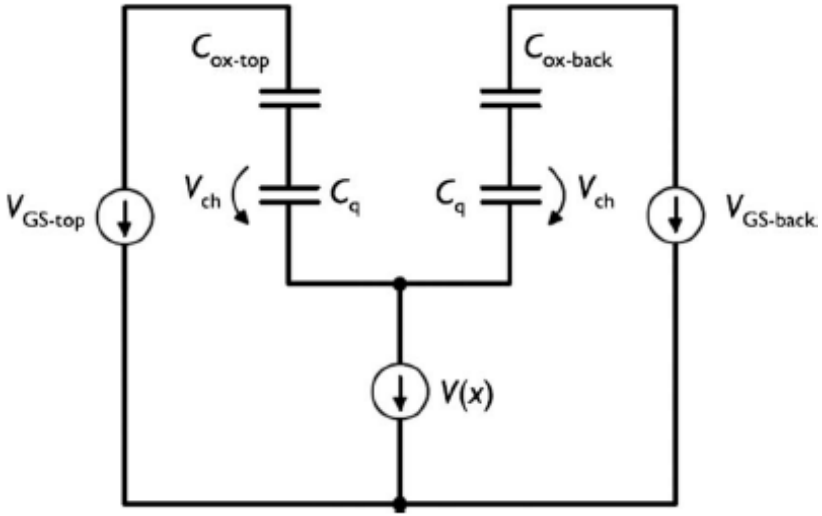
D. Jimenez, *TED* ‘11

- Features:
  - Back gate effect on the shift Dirac voltage
  - Reducing S/D resistance by using back gate

More on GET Model

- S. Thiele, U. Ilmenau, *JAP* '10

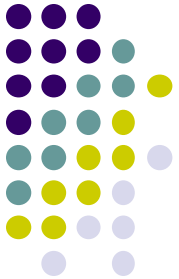




$$C_q = -\frac{dQ_{\mathrm{sh}}}{dV_{\mathrm{ch}}} = \frac{2q^2}{\pi}\frac{q|V_{\mathrm{ch}}|}{(\hbar v_F)^2}$$

Not a constant!

Central Ideal in GFET Modeling



- To each position x in the channel belongs a certain local potential $V(x)$

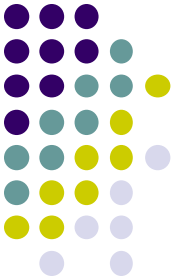
$$I_D = -qN_{\text{sheet}}(x)v(x)W = -qN_{\text{sheet}}\left[V(x)\right]v\left[V(x)\right]W$$

- The voltage across the quantum capacitance, C_q, is named as V_{ch}.
- Density of States (DOS) for graphene

$$D(E) = \frac{2}{\pi}\frac{|E - E_{CV}|}{(\hbar v_F)^2},\ v_F = 10^8\,\text{cm/s}$$

$$\text{Taking } E_{CV} = 0,\ E_F = qV_{\text{ch}}$$

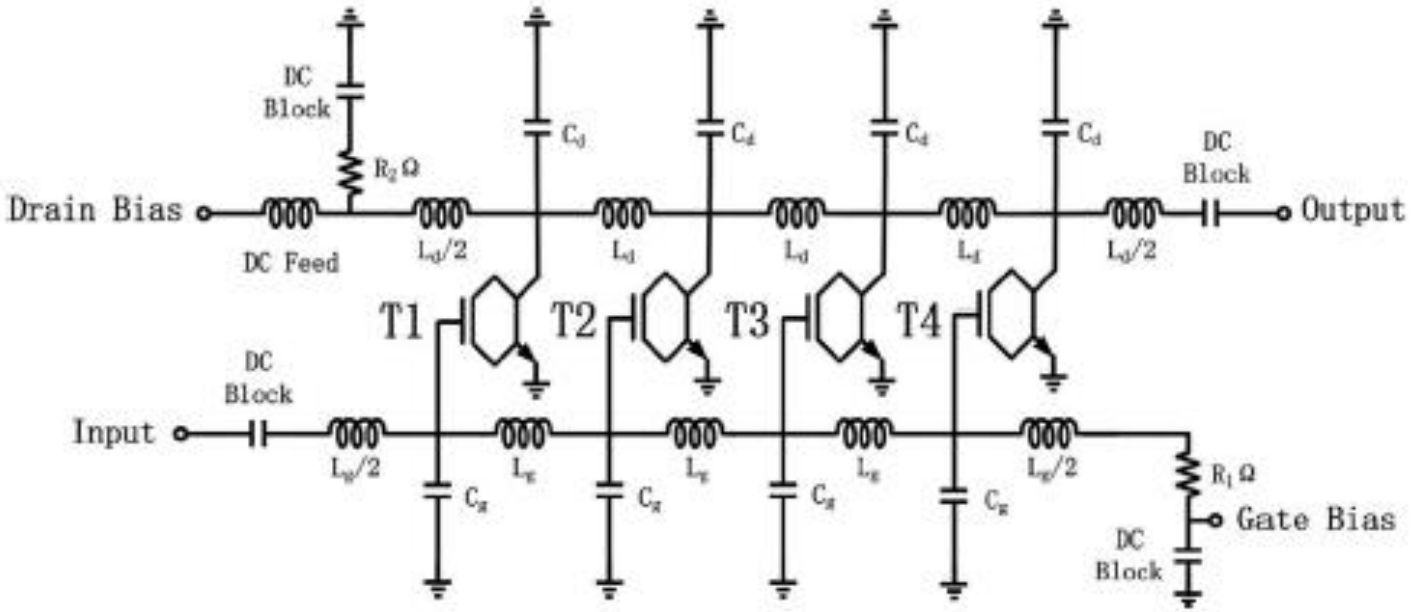
Self-Consistent Solution of V_{ch} and C_q



- J. Thielte

Four-Stage GFET Distributed Amplifier

- H Lyu, Tsinghua, *Scientific Report* '15



Conclusions

- Besides carrier transport, electrostatics (including quantum effects such as quantum confinement) still plays the most central role in device modeling.
- It is not certain towards the end of the MOS scaling, new (channel) materials and new device structures will emerge as the mainstream IC technology
- The case study of quantum capacitance prepares the modeling society for the new challenges.