The Critical Role of Quantum Capacitance in Compact Modeling of Nano-Scaled and Nanoelectronic Devices

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Outline

- The major concerns near the end of MOS scaling
- What is quantum capacitance (QC) and why has it mostly been ignored in FET compact modeling?
- Modeling and equivalent circuits for QC
- Carbon-NanoTube FET (CNT-FET), a classical Example for illustrating QC
- Compact model for Graphene FET (GFET) and its application in design of a distributed amplifier
- Conclusions
Driving Force for Further MOS Scaling

- It’s low power, low voltage, and low gate delay (power-delay product)
- From planar to FinFET, and from tunneling FET to novel nano-electronic devices (new channel materials)

Source: Bohr/Mistry slides, May 2011
Important Means to Further MOS Scaling

- New device structures
  - Gate-All-Around Nanowire (GAA-NW) FETs
  - Tunneling FETs (tFETs)
  - Junctionless (JL) FETs
- New channel materials
  - III-V CMOS, e.g., InAs for nMOS and GaSb for pMOS on GaAs substrate
  - 2D materials, typical graphene, and emerging MoS$_2$, WSe$_2$, black phosphorous (BP), etc.
  - 1D materials, mainly carbon nanotube (CNT)
Critical Device/Material Parameters to Look At

- **Devices**
  - Subthreshold swing (SS): break through the 60mV/dec limit
  - $I_{on}$ and $I_{on}/I_{off}$ ratio
  - Off-state leakage (drain controllability over gate)

- **Channel materials**
  - Mobility
  - Density of States (DOS)
Tunneling FETs and Small SS

K. Jeon, SEMATECH/UCB, VLSI ‘10

Features:

- $I_{on}/I_{off} : 10^8$
- n-i-p on 40nm BOX
- NiSi source structure
- High field pocket
- Recessed source-side silicon
- SS $\leq$ 60 mV/dec for 3-decades of $I_D$
CNT-FET and Small Gate Delay

- J. Appenzeller, IBM, *PRL* ‘04

![Diagram of CNT-FET structure](image)

- pMOS, $V_{ds}=-0.5V$

- Ambipolar band-to-band tunneling

- Tunneling thru SB

- Simulation at $T=300K$

- $S \sim 65 mV_{dec}$

- $S \sim 40 mV_{dec}$

- $t_{ox-Al} = 2.5nm$

- $t_{ox-Al} = 5nm$

- $t_{ox-Al} = 10nm$

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MOS-AK Shanghai, Jur
Why Need to Model Quantum Capacitance (QC)

- An accurate total (and especially the intrinsic) gate capacitance is important in evaluating the transistor performance (gate delay, say)
  \[
  \tau_{\text{delay}} = C_{\text{gate}} \frac{V_{\text{dd}}}{I_D}
  \]
- Channel materials are assessed for both mobility and density-of-states (DOS), often there is a trade-off (high \( \mu \) implies low DOS)
- Nano-electronic (and gate-all-around) devices don’t have body contact to their channel.
QC Is Not New: MOS Capacitor Has DOS Capacitance

Having bulk contact to channel

\[ Q_{\text{inv}} = q \int n(x) \, dx, \quad C_{\text{inv}} = \frac{\partial Q_{\text{inv}}}{\partial \psi_S} \]

\[ n = n_i e^{(\psi - \phi_F)/V_t} = N_C e^{(E_F - E_C)/k_BT} \]

\[ n_i = \sqrt{N_C N_V} e^{-E_g/2k_BT} \]
Then, Why Quantum (Capacitance)?

- First coined by S. Luryi of Bell Labs, *APL* ’88 for 2DEG

\[
2 \times 2 \quad 2 \text{DOS} \\
E_1 \quad E_2 \\
E_c \quad E_F
\]

\[
C_{Qi} = \frac{q^2 m^*_l / (\pi \hbar^2)}{1 + e^{(E_i - E_F)/k_BT}}
\]

D. Jin, MS thesis, MIT, 2010

E.g., \( m^* = 0.98 m_0 \) for Si \( m_l \)
Impact of Quantum Capacitance

- B. Yu, UCSD, T-ED, ‘08
Effective Mass of DOS for Different Semiconductors

G. Jin, MIT, MS Thesis, ’10

- Si: $1.08 \, m_0$
- GaAs: $0.067 \, m_0$
- InAs: $0.026 \, m_0$
- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$: $0.04 \, m_0$

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DOS Dependence on Electronic Energy for 1/2/3D

\[ D_1(E) = \frac{1}{\sqrt{c_k (E - E_0)}} \]

\[ D_2(E) = \frac{\pi}{c_k} \]

\[ D_3(E) = 2\pi \sqrt{\frac{E - E_0}{c_k^3}} \]

\[ N_{3D}(E) = \frac{V}{2\pi^2} \left( \frac{2m^*}{\hbar^2} \right)^{3/2} \sqrt{E - E_0} \]

\( c_k \) in dispersion relation of \( E = E_0 + c_k k^p \)

and \( p \) is the power of \( k \),
e.g., \( p = 2 \) for parabolic

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DOS for Nanowire

- B. Yu, UCSD, *T-ED ‘08*

Si nanowire of $r = 2.5$nm
Quantum Capacitance (QC): Modeling Approach

Ballistic transport assumption: provide knowledge of Fermi level in channel

nMOS Electron Energy

$U_{SCF} = -q\psi_s$

A. Raychowdhury, *T-ICCAD* ‘04

A. Rahman, *T-ED* ‘04
Definition of QC: $C_q$

\[ C_q = -\frac{dQ_{ch}}{dV_{ch}} \]
QC (cont’d): Equivalent Circuit

- Use charge balance principle to find $V_{ch}$:
  \[-C_{ox} \times (V_G - V_{ch}) = Q_S (V_{ch} - V_S) + Q_D (V_{ch} - V_D)\]

- Incremental (small signal) capacitance network

\[\delta V_{ch} = \frac{C_{ox}}{C_{ox} + C_{qs} + C_{qd}} \delta V_G, \quad C_{qs} = \frac{\delta |Q_S|}{\delta V_{ch}}, \quad C_{qd} = \frac{\delta |Q_D|}{\delta V_{ch}}\]
Application of QC to tFET

- Z. Yu, Tsinghua, *ICSICT* ‘12

Compared to

S. Fregonese, *TED* ‘09
Quantum Capacitance in III-V FETs

- D. Jin, MS thesis, MIT, 2010

\[
\frac{q}{\partial (E_F - E_C)} \left| Q_i \right| = \frac{q}{\partial (E_F - E_i)} \left| Q_i \right| + \frac{q}{\partial (E_i - E_C)} \left| Q_i \right|
\]
Thermal Emission vs. Band-to-Band Tunneling (BtBT): Band-Pass Filtering

- Now, consider using BtBT to improve SS

\[ T(E) = \text{const} = \exp \left( -\frac{4\sqrt{2m^*E_g^{3/2}}}{3q\hbar E} \right) \]

\[ E = \left( E_g + \Delta\phi \right)/\lambda, \quad \lambda = \sqrt{\frac{\varepsilon_{\text{cnt}}}{\varepsilon_{\text{ox}}}} t_{\text{ox}} t_{\text{cnt}} \]

J. Knoch, IBM, DRC '05
SCE: Short-Channel Effect


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**Φ₀** is influenced by **Φ₃**

- Look for
  - gate control
  - drain control (DIBL)
  - long channel or SCE: \( L \) vs. \( \lambda \)
SS of CNT-FET as a Function of $t_{\text{ox}}$: a Measure of Gate Controllability

- J. Appenzeller, IBM, *PRL* ‘02

J. Knoch, IBM Zurich, *PSS* ‘08

- J. Appenzeller, IBM, *PRL* ‘02

120nm SiO$_2$  
20nm HfO$_2$
Charge Pile-up in Channel of CNT-FET through BtBT

- J. Appenzeller, IBM, *PRL* ‘04 (both experiment and simulation by NEGF)
- S. Fregonese, U Bordeaux, *T-ED*, ‘09

![Diagram of Double gates]

J. Knoch, IBM, *PSS* ‘08
Dual Forces in Controlling Channel Potential: from Gate and Drain Terminals

- J. Knoch, IBM, PSS ’08

\[ C_q = \frac{2}{h} \sqrt{\frac{8m^*}{\Phi_f^0 - E_f^d}} \]

\[ \delta \Phi_f^0 = \frac{C_{ox}}{C_{ox} + C_q + C_d} \delta \Phi_g + \frac{C_q + C_d}{C_{ox} + C_q + C_d} \delta \Phi_d \]

- For an electrostatically well-designed device at off-state \( C_{ox} \gg C_q, C_d \)

- **QCL**: quantum capacitance limited \( C_{ox} \gg C_q \)

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MOS-AK Shanghai, June 26-28, 2016 24
Advantage of 1D Transport for CNT-FET

- J. Knoch, IBM, PSS ‘08

\[ C_{q, \text{BtBT}} = \frac{\partial Q_{\text{BtBT}}}{\partial \Phi^0_f} \approx \frac{4\lambda \sqrt{2m^*E_g^{3/2}}}{3\hbar (E_g + \Delta \Phi)} T_{\text{WKB}} \int dE \ D(E) \left[ 1 - f \left( E - E_f^S \right) \right] \]

\[ + qT_{\text{WKB}} \frac{\partial}{\partial \Phi^0_f} \int dE \ D(E) \left[ 1 - f \left( E - E_f^S \right) \right] \]

\[ C_{q, \text{BtBT}} \propto T_{\text{WKB}} \text{ and } I_D \propto T_{\text{WKB}} \]

resulting in \( \tau_{\text{delay}} \) independent upon \( T_{\text{WKB}} \)
Dilemma of QCL Regime

- Gate control is good (channel potential closely follow the gate bias), meaning small SS
- Yet, the total gate capacitance becomes small, which implies small on current
- There may be some optimization scheme for minimizing the gate delay
- Similar situation for JL-FETs
Compact Model for GFET

- W. Zhu, Tsinghua, SISPAD ’12

Features:
- Back gate effect on the shift Dirac voltage
- Reducing S/D resistance by using back gate

D. Jimenez, TED ‘11
More on GET Model

- S. Thiele, U. Ilmenau, *JAP* ‘10

\[
C_q = -\frac{dQ_{sh}}{dV_{ch}} = \frac{2q^2}{\pi} \frac{q|V_{ch}|}{(\hbar v_F)^2}
\]

Not a constant!
Central Ideal in GFET Modeling

- To each position $x$ in the channel belongs a certain local potential $V(x)$

$$I_D = -qN_{\text{sheet}}(x)v(x)W = -qN_{\text{sheet}}\left[V(x)\right]v\left[V(x)\right]W$$

- The voltage across the quantum capacitance, $C_q$, is named as $V_{\text{ch}}$.

- Density of States (DOS) for graphene

$$D(E) = \frac{2}{\pi} \left| \frac{E - E_{CV}}{\hbar v_F} \right|^2, \hspace{1cm} v_F = 10^8 \text{ cm/s}$$

Taking $E_{CV} = 0$, $E_F = qV_{\text{ch}}$
Self-Consistent Solution of $V_{ch}$ and $C_q$

- J. Thielte
Four-Stage GFET Distributed Amplifier

- H Lyu, Tsinghua, *Scientific Report ‘15*
Conclusions

- Besides carrier transport, electrostatics (including quantum effects such as quantum confinement) still plays the most central role in device modeling.
- It is not certain towards the end of the MOS scaling, new (channel) materials and new device structures will emerge as the mainstream IC technology.
- The case study of quantum capacitance prepares the modeling society for the new challenges.