Featured Circuit Simulation Using SMARTSPICE Compact Models and Verilog-AMS

MOS-AK - SILVACO

SANTA CLARA, 2017
SmartSpice Technology Models

**BIPOLAR**
- BJT
- VBIC
- HICUM
- HICUMUL0
- MEXTRAM
- PBJT
- MODELLA
- HBT
- HISIM-IGBT

**SOI**
- BSIMSOI3
- BSIMSOI4
- BSIM-IMG SOI
- HiSIM-SOI
- HiSIM-SOTB
- LETI-UTSOI

**TFT**
- RPIpSi
- RPIpSi
- UOTFT
- LUTFT
- MOTFT

**DIODE**
- DIO
- DIO-CMC
- HiSIMDIO
- Juncap
- Juncap2
- DIO500

**LASER**
- VCSEL

**MOS**
- MOS123
- BSIM1
- BSIM3
- BSIM4
- BSIM6
- BSIMBULK
- BSIM-CMG
- MOS9
- MOS11
- MOS20
- EKV
- EKV3
- PSP

**HiSIM**
- HiSIM
- HiSIM2
- HiSIMHV
- HiSIMHU
- HiSIMHUHV
- HSIMHUIGBT
- JFET
- MOSVAR
SmartSpice Advanced Nodes Technologies

Designer Features
TSMC TMI 7nm

- Aging analysis
- Self heating
- TSMC TMI model format compatibility
- Monte Carlo local and global variation
- High sigma Monte Carlo
SmartSpice for DISPLAY

- Flexible display
- OLED display
- TFT strain model
- Amorphous TFT model
- Reliability model
- Pixel analysis
- INVAR
Extending conventional uniaxial bending model by using the Kirchhoff thin plate element model to define flexible substrate mechanical deformation in the proximity of a thin-film transistor.

- It is possible to handle pure banding (uniaxial, biaxial), pure twisting and combined deformation
- Requires only 3 instance parameters which could be defined from mechanical deformation measurement setups or from mechanical co-simulation output.

uniaxial deformation  biaxial deformation  wist deformation
Mechanical Deformation Induced Variations in TFT Electrical Characteristics

\[
\epsilon = [\epsilon_L, \epsilon_W, \epsilon_{LW}]
\]

\[
\epsilon_L = CL \cdot \frac{d_{sub}}{2}
\]

\[
\epsilon_W = CW \cdot \frac{d_{sub}}{2}
\]

\[
\epsilon_{LW} = LW \cdot d_{sub}
\]
### Instance Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL</td>
<td>Channel length bending curvature</td>
<td>1/m</td>
<td>0.0</td>
</tr>
<tr>
<td>CW</td>
<td>Channel width bending curvature</td>
<td>1/m</td>
<td>0.0</td>
</tr>
<tr>
<td>CLW</td>
<td>Channel twisting curvature</td>
<td>1/m</td>
<td>0.0</td>
</tr>
</tbody>
</table>

### Model Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Units</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLMU, CWMU, CLWMU</td>
<td>Mobility strain sensitivity parameters</td>
<td>m³/Vs</td>
<td>0.0</td>
</tr>
<tr>
<td>CLVT, CWVT, CLWVT</td>
<td>Threshold voltage strain sensitivity parameters</td>
<td>Vm</td>
<td>0.0</td>
</tr>
</tbody>
</table>
SmartSpice for memory design

New models and features

\[
\frac{\partial}{\partial x} \left( K_x \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left( K_y \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left( K_z \frac{\partial T}{\partial z} \right) = -Q_y + \rho C_p \frac{\partial T}{\partial t}
\]

**Q** (x,y,z,t) Power density of heat sources (W/m^3)

**\rho** (x,y,z) Density of the material (Kg/m^3)

**K** (x,y,z) Thermal conductivity of the material (W/m*C)

**C** (x,y,z) Heat capacity (J/Kg*C)

**T** (x,y,z,t) Temperature distribution

**STT-MTJ, magnetic element**

**PCM, phase change memory**

**RRAM, resistive element**

**Aging simulation**

**Device reliability**

**PCM electro thermal reliability**

**Verilog-A models enhancements**
SmartSpice for DISPLAY

Reliability

Aging analysis

- Time – dependent degradation
- Intrinsic device reliability model
- Extreme operating conditions
- Negative Bias temperature Instability (NBTI)
- Hot Carrier Injection (HCI)
- Time dependent dielectric breakdown (TDDB)
- Gate oxide integrity (GOI)
Comprehensive Radiation Hardening Tool Flow

PROCESS & DEVICE

DESIGN & VERIFICATION
• The two major tools are
  • **SmartSpice RadHard** – Circuit Level Radiation Simulation
  • **Victory Radiation Effects Module** – Device Level Radiation Simulation

Victory

SmartSpice & Gateway

AccuCore

InVar (Thermal, Power, EM/IR, 3D)
RADIATION ANALYSIS

- Provides accurate Dose Rate (DR), SEE, analysis using the .RAD statement for transient and DC analysis.

- Built as an extension to the industry-proven SmartSpice Analog Circuit Simulator allowing for the use of foundry supplied models.

- Analyzes Dose Rate with modified Wirth & Rogers' models and with optional customer-defined models.

- Analyzes Single Event Upsets (SEU’s) and Multi-Bit Upsets (MBU’s) with modified Messenger’s models and with optional customer-defined models.

- Advanced circuit optimization improves the radiation tolerance of the design and enables complex analysis of design trade offs necessary to meet system specifications.

- Supports standard foundry-supplied HSPICE®, PSPICE® and SmartSpice models for bulk CMOS, SOI, bipolar, and BiCMOS processes.

SILVACO
SmartSpice Signal Integrity Package

W element  Field Solver

W element statements

.MATERIAL

.SHAPE

.LAYERSTACK

.FSOPTIONS

.MODEL MODELTYPE=FieldSolver
Proximity effect induced by surrounding electrical field

- B-field from 1-st conductor
- Reduced current density back here
- Eddy currents
- Second conductor
- By conductor 1 Influenced current

Rs Matrix

<table>
<thead>
<tr>
<th></th>
<th>R11</th>
<th>R12</th>
<th>R22</th>
</tr>
</thead>
<tbody>
<tr>
<td>R11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R12</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Increased current density
B-field generating current

First conductor

By conductor 1 Influenced current
Dynamic Model Development

- **Stress Model for TFT devices (A-Si/OxideTFT application)**
  - Consider Bias, Temp, and Duty dependence
  - Symmetric Vth shift and recovery Modeling
  - Asymmetric Vth shift and recovery Modeling
  - Constant Vth Recovery Modeling
  - Interface traps and Oxide traps induced Vth shift and Recovery reproduced by Semi-Physical Models
  - Gate Driver Simulation with Stress Models
  - Find the major failure root cause due to stress condition
  - Estimate the life time with TFT circuits

- **Hysteresis Model for TFT devices (OxideTFT/LTPS for AMOLED application)**
  - Consider Bias, Temp, and Duty dependence
  - Symmetric Vth shift and recovery Modeling
  - Asymmetric Vth shift and recovery Modeling
  - Consider Floating condition as Vth constant
  - 6T1C AMOLED pixel circuit simulation
SmartSpice: Verilog-A API

- Verilog-AMS is essential part of SMARTSPICE
- Verilog-AMS API is a new mechanism to connect SPICE dialects: Fast Spice, RF, traditional SPICE
- Verilog-AMS API allows to integrate modeling tool UTMOST with SMARTSPICE
- New custom features are emerging and must be supported by Verilog-AMS simulator
  - Radiation
  - Mechanical strain
  - Fast Spice (model look up and model latency)
  - Integration with partitioning and multithreading
  - OMI CMC
  - TMI TSMC
  - Reliability
  - Integration with field solvers
  - TFT hysteresis
  - Integration with Fast Monte Carlo
  - Integration with runtime thermal analysis
- ADMS replacement by Verilog-AMS
- Challenging qualification for TSMC TMI FINFET and GF SOI.
• Fast and accurate SPICE model generation and validation
• User-friendly GUI and powerful script mode
  • Silvaco TCAD flow integration
• Relational database to store and manage datasets and projects
UTMOST IV Optimization

- Full SPICE simulator supports all compact, macro-model, Verilog-A and TMI models
- Powered by high-speed SmartSpice interface
  - Hundreds of simulations per second
  - No speed slowdown with macro-models
  - Also support for third party simulators
- Any combination of data
  - Multiple temperatures, wafers, die, devices
  - Mixture of DC, Capacitance, S-parameter and extracted data (Vt, Idsat, etc)
- Any combination of device model parameters and netlist parameters
SOI Modeling Using Verilog-A

- FDSOI device characterization using Verilog-A BSIMSOI 4.5 module
Generic Macromodel Support

- Netlist of any complexity can be defined for macro-model
- All macro-model parameters available for simultaneous optimization and rubberbanding
• Proprietary approach to creating models
• Fast modeling for novel devices
Novel Device Modeling: OTFT

- OTFT model created using TechModeler
Novel Device Modeling: OLED

- OLED model
  - I-V model created with TechModeler
  - C-V macromodel extracted using Utmost
  - Models combined in UTMOST IV using Verilog-A
Thank you!