A Normally-on MOSFET Compact Model based on Surface Potential Description

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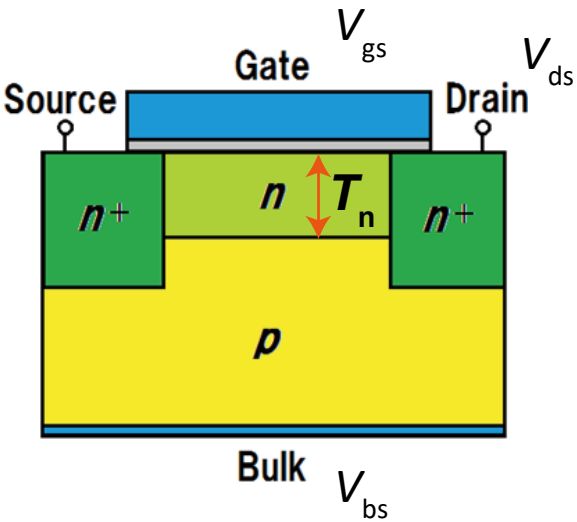
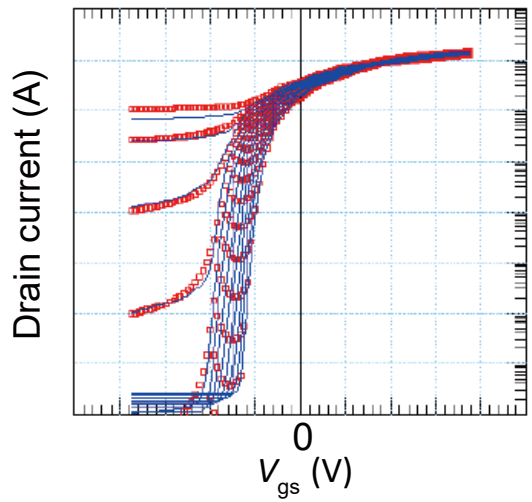
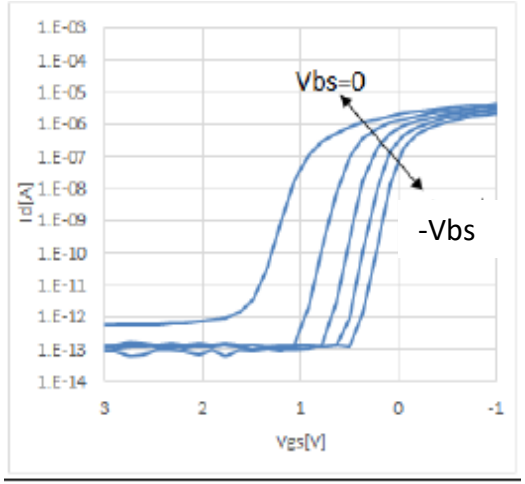
Normally-on MOSFET

- Normally-on (depletion-type) MOSFET is one descendant of MOSFET used for low-power analog circuits.



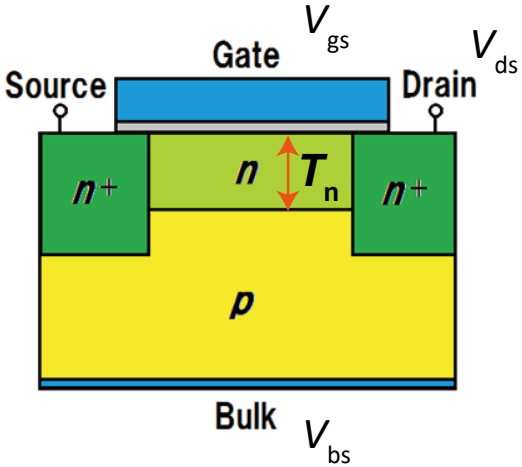


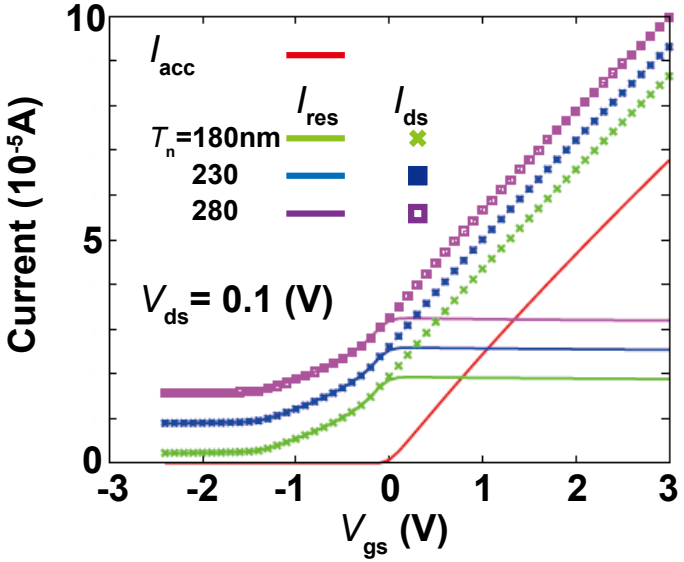


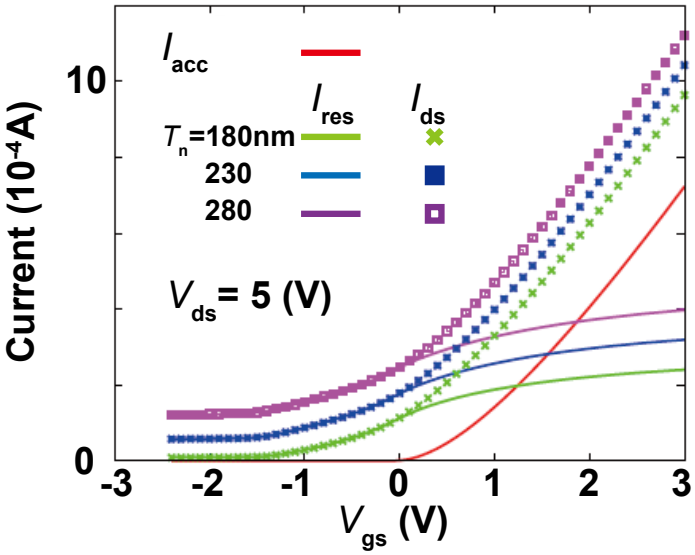
- A prominent feature is the large leakage current at V_{bs}= 0 that creates the normally-on condition.

Normally-on MOSFET Characteristics

- Accumulation-mode current (I_{acc}) at the surface
- Resistor current (I_{res}) within the neutral region beneath the surface

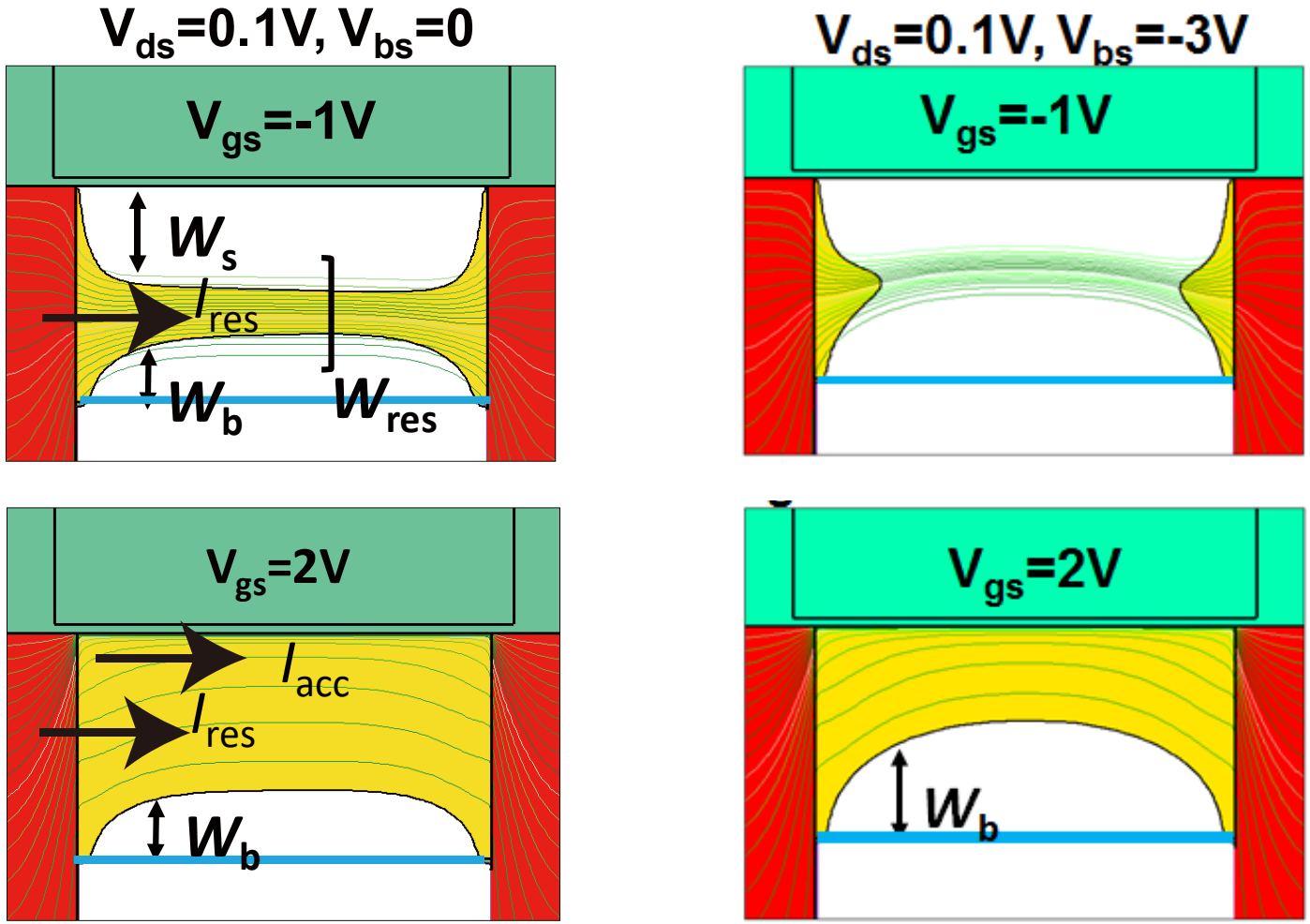






Composite description of current.

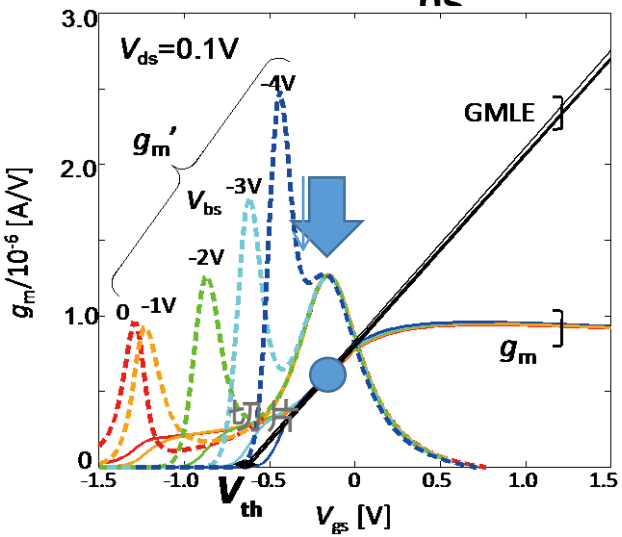
Buried Layer Dynamics at Low V_{ds}



Neutral region has a complex bias dependency.

Threshold Voltage Characteristics

Low V_{ds}

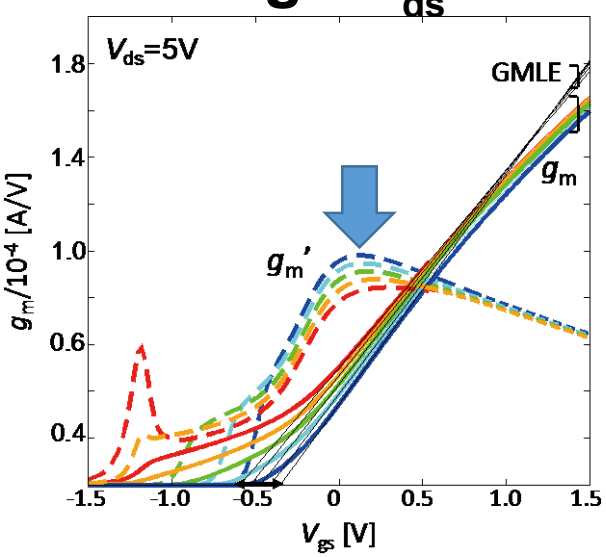


V_{bs}	V_{th}
0	-0.626
-1V	-0.630
-2V	-0.638
-3V	-0.651
-4V	-0.656

No dependence on V_{bs} at accumulation.

I_{acc} and I_{res} can be separated.

High V_{ds}



V_{bs}	V_{th}
0	-0.592
-1V	-0.532
-2V	-0.471
-3V	-0.410
-4V	-0.351

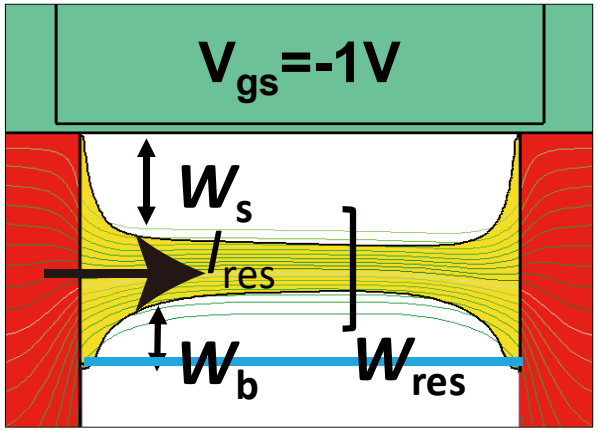
With V_{bs} dependence.

I_{acc} and I_{res} cannot be separated.

Short-channel Effects

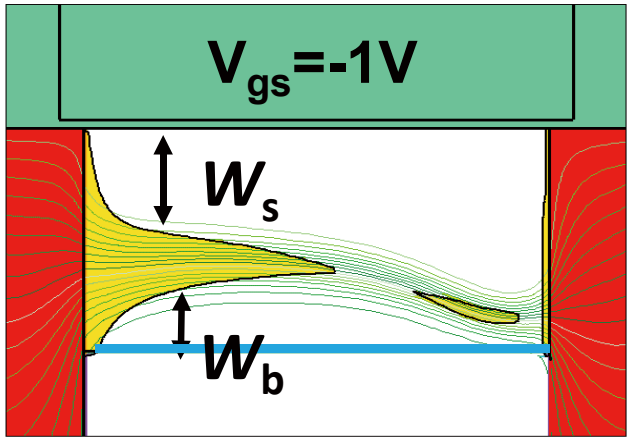
Low V_{ds}

V_{ds}=0.1V, V_{bs}=0



High V_{ds}

V_{ds}=5V, V_{bs}=0



Pinch-off occurs.

Modeling of Normally-on MOSFET

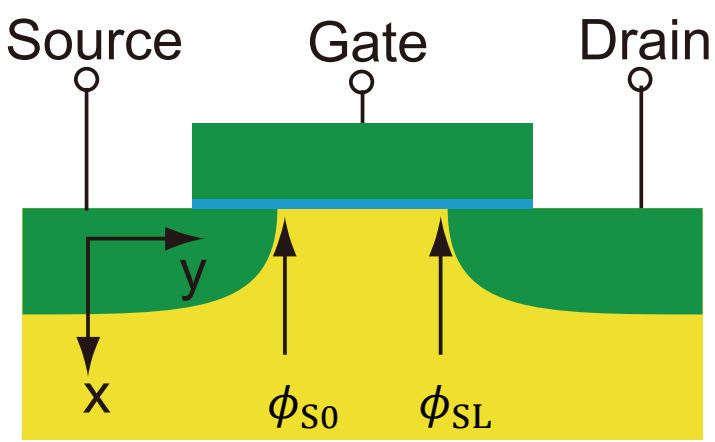
- Composite currents:
  Accumulation-mode current(I_{acc}) and Resistor current (I_{res})
- Bias-dependence of the neutral region within the buried layer

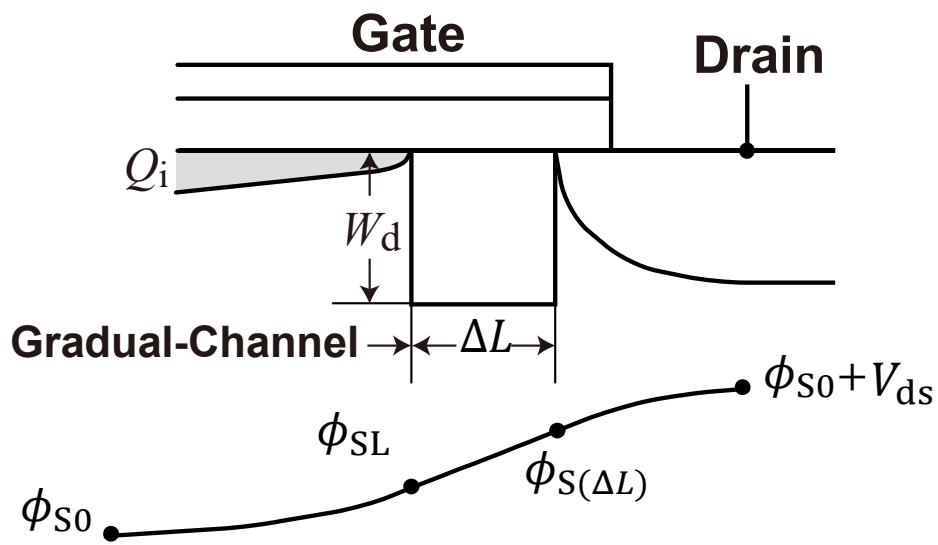
Surface-potential-based modeling

Compact Model: HiSIM

- Hiroshima University STARC IGFET Model (HiSIM. HiSIM_HV, HiSIM_SOI, HiSIM_SOTB)
- Surface-Potential-Based Compact Model

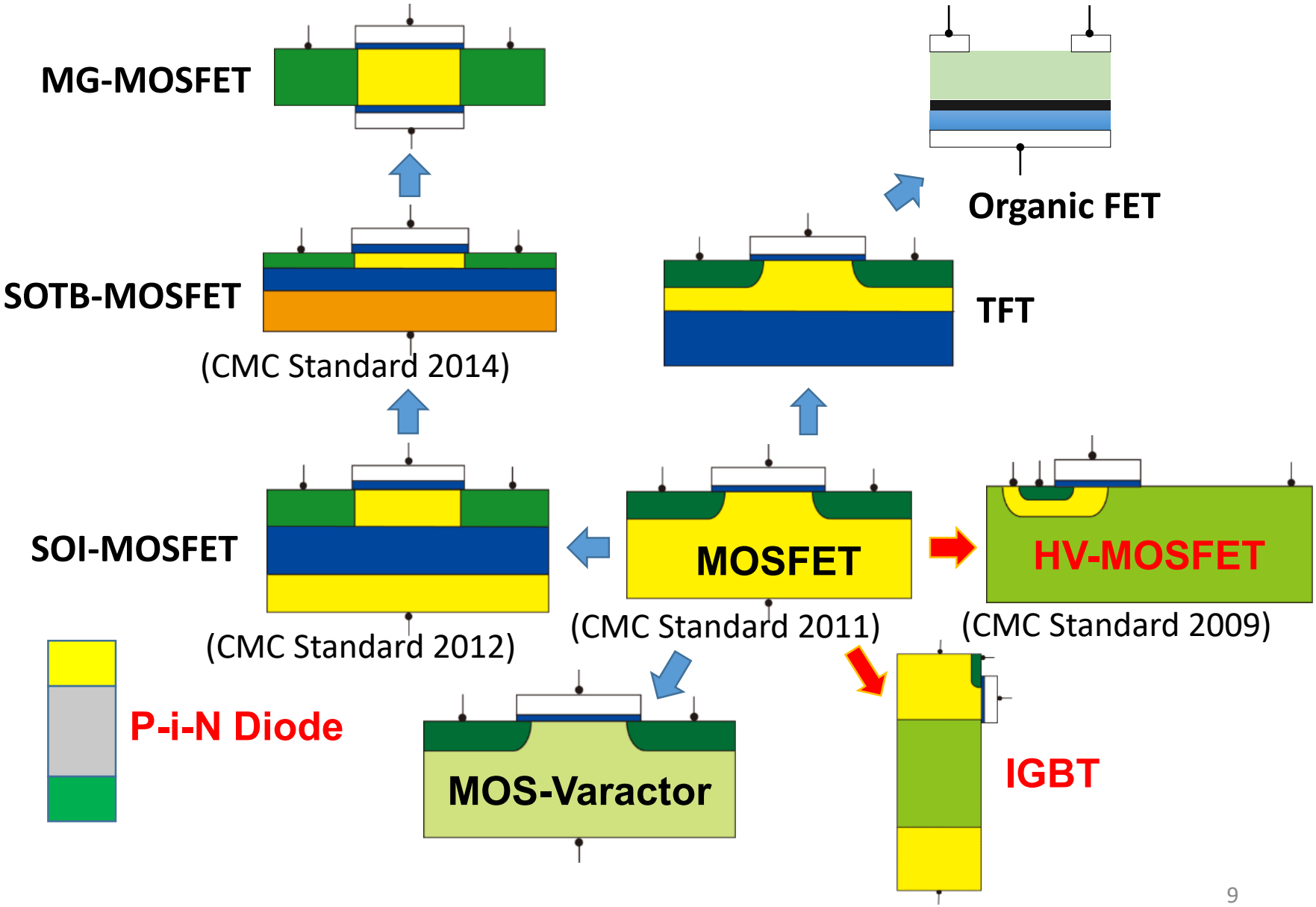
HiSIM



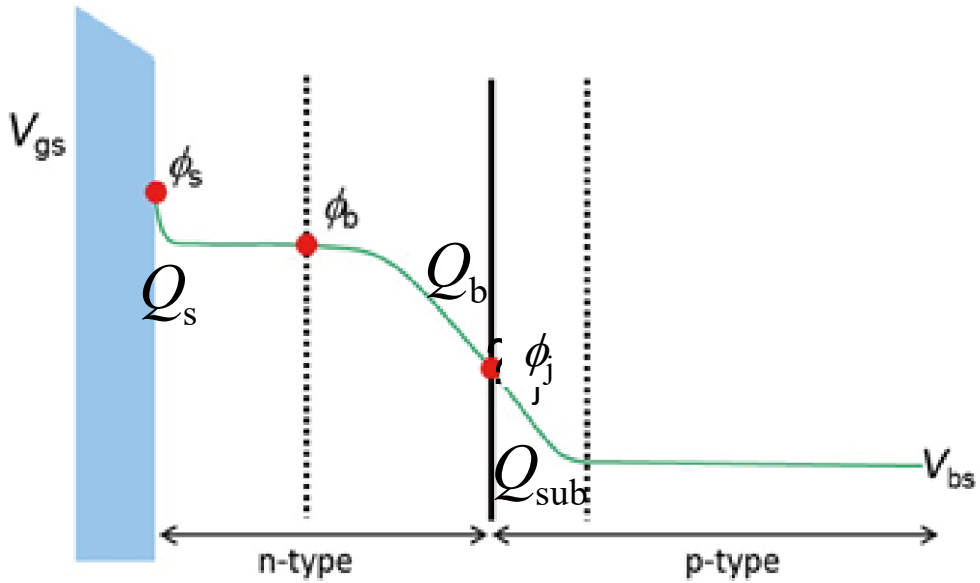


Potentials at important locations are solved.

HiSIM Family of Models



Modeling of Potential Distribution



$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\varepsilon_s}$$

$$\rho = Q_s + Q_b + Q_{sub}$$

$$Q_s = \pm cnst0\sqrt{exp(\Phi) - 1 - \Phi + CNT}$$

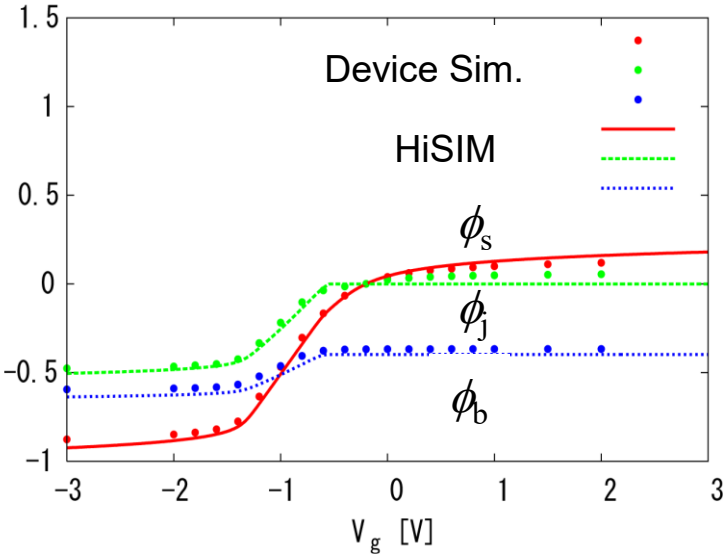
$$\Phi = \phi_s - \phi_b \qquad CNT = cnst1\big(exp(-\beta\phi_s) - exp(-\beta\phi_b)\big)$$

$$Q_b = qN_{dep}\sqrt{\frac{2\varepsilon_s}{qN_{dep}}(\phi_b - \phi_j)} \qquad Q_{sub} = qN_{dep}\sqrt{\frac{2\varepsilon_s}{qN_{sub}}(\phi_j - V_{bs} + V_{bi})}$$

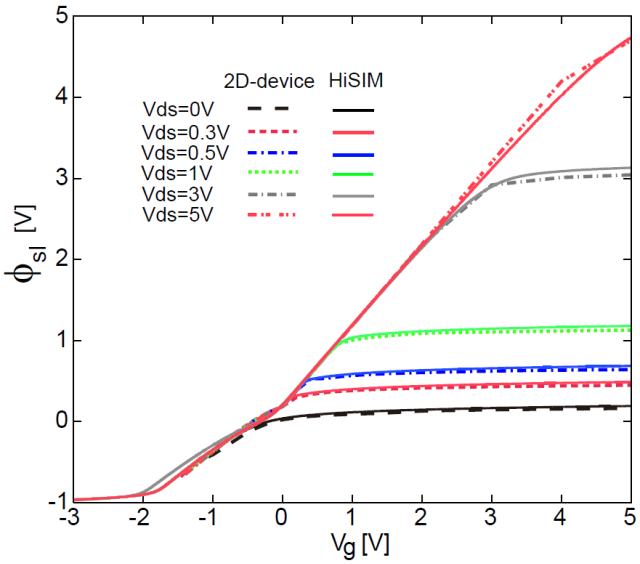
$$cnst0 = \sqrt{2\varepsilon_s \cdot q \cdot N_{dep}/\beta} \qquad cnst1 = {n_i}^2/{N_{dep}}^2$$

Modeling Results

Potential Distribution



source



drain

Potential distribution is verified using 2D device simulation.

Current Components

$$I_{\mathrm{ds}} = I_{\mathrm{acc}} + I_{\mathrm{res}}$$

Accumulation Current (I_{acc})

- governed by conventional MOSFET physics.

$$I_{\mathrm{acc}} = \frac{W_{\mathrm{eff,nf}}}{L_{\mathrm{ch}}} \cdot \frac{1}{\beta}(\mu \cdot I_{\mathrm{dd}})$$

$$I_{dd} = -\beta \frac{(Q_{\mathrm{n0}} + Q_{\mathrm{nl}})}{2} \cdot \phi_{\mathrm{ds}} - Q_{\mathrm{n0}} + Q_{\mathrm{nl}}$$

Universal Mobility

$$\mu_0 = \frac{1}{\mu_{\mathrm{CB}}} + \frac{1}{\mu_{\mathrm{PH}}} + \frac{1}{\mu_{\mathrm{SR}}}$$

$$\mu_{\mathrm{CB}} = \mathrm{MUECB0} + \mathrm{MUECB1} \cdot \frac{-Q_{\mathrm{n0}}}{q \cdot 10^{11}}$$

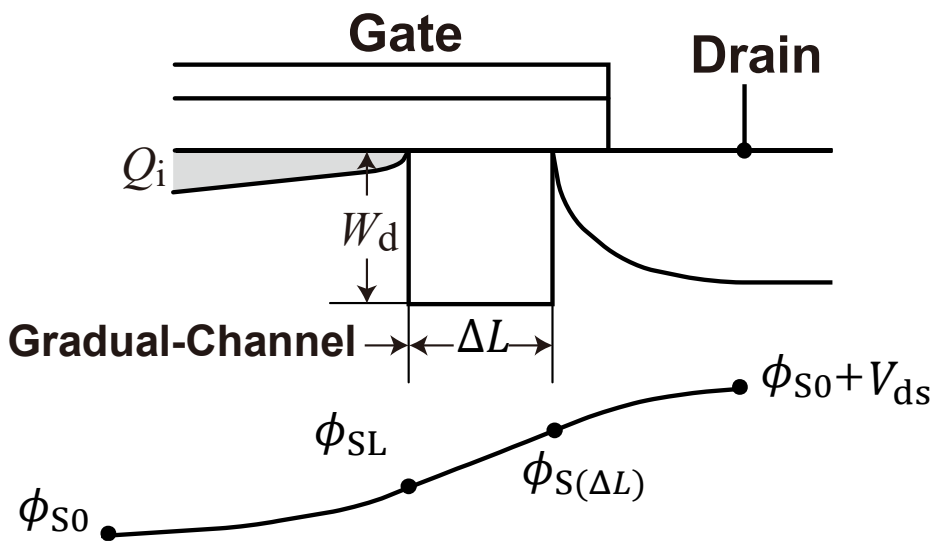
$$\mu_{\mathrm{PH}} = \frac{M_{\mathrm{uephonon}}}{E_{\mathrm{eff}}^{\mathrm{MUEPH0}}} \qquad \mu_{\mathrm{SR}} = \frac{\mathrm{MUESR1}}{E_{\mathrm{eff}}^{M_{\mathrm{uesurface}}}}$$

High-field mobility

$$E_{\mathrm{eff}} = \frac{\left(\frac{\mathrm{NINV}}{\varepsilon_{\mathrm{Si}}}\right) \cdot (-Q_{\mathrm{n0}})}{1 + (\phi_{\mathrm{SL}} - \phi_{\mathrm{S0}}) \cdot N_{\mathrm{invde}}}$$

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 E_{\mathrm{y}}}{V_{\mathrm{max}}}\right)^{\mathrm{BB}}\right)^{\frac{1}{\mathrm{BB}}}}$$

Short-Channel Effect



$$\phi_S(\Delta L) = (1-\mathrm{CLM1})\cdot\phi_{SL} + \mathrm{CLM1}\cdot(\phi_{S0}+V_{ds})$$

$$\Delta L = \frac{1}{2}\left[-\frac{1}{L_{eff}}\left(2\frac{I_{dd}}{\beta Q_i}z + 2\frac{N_{sub}}{\varepsilon_{Si}}\left(\phi_S(\Delta L)-\phi_{SL}\right)z^2 + E_0 z^2\right) + \sqrt{\frac{1}{L_{eff}^{\ 2}}\left(2\frac{I_{dd}}{\beta Q_i}z + 2\frac{N_{sub}}{\varepsilon_{Si}}\left(\phi_S(\Delta L)-\phi_{SL}\right)z^2 + E_0 z^2\right)^2 + 4\left(2\frac{N_{sub}}{\varepsilon_{Si}}\left(\phi_S(\Delta L)-\phi_{SL}\right)z^2 + E_0 z^2\right)}\right]$$

$$\Delta L = \Delta L\left(1+\mathrm{CLM6}\cdot\left(L_{gate}\cdot 10^6\right)^{\mathrm{CLM5}}\right)$$

Effect of lateral field is considered.

Resistive Current (I_{res})

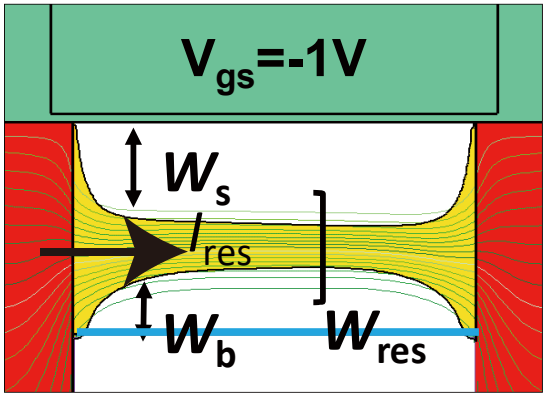
- governed by potential difference between source and drain.

$$I_{\mathrm{res}} = q \cdot N_{\mathrm{res}} \cdot \mu_{\mathrm{res}} \cdot \frac{W_{\mathrm{res}} \cdot W_{\mathrm{eff}}}{L_{\mathrm{eff}}} V_{\mathrm{ds}}$$

$$W_{\mathrm{res}} = T_{\mathrm{n}} - W_{\mathrm{s}} - W_{\mathrm{b}}$$

$$W_{\mathrm{b}} = \sqrt{\frac{2\varepsilon_{\mathrm{Si}}\varepsilon_0 N_{\mathrm{sub}}}{qN_{\mathrm{n}}\left(N_{\mathrm{n}} + N_{\mathrm{sub}}\right)} \cdot \left(\phi_{\mathrm{bi}} - V_{\mathrm{bs}}\right)}$$

$$W_{\mathrm{s}} = \sqrt{\frac{2\varepsilon_{\mathrm{Si}}\varepsilon_0}{q \cdot N_{\mathrm{n}}}\left(-\phi_{\mathrm{res}}\right)}$$

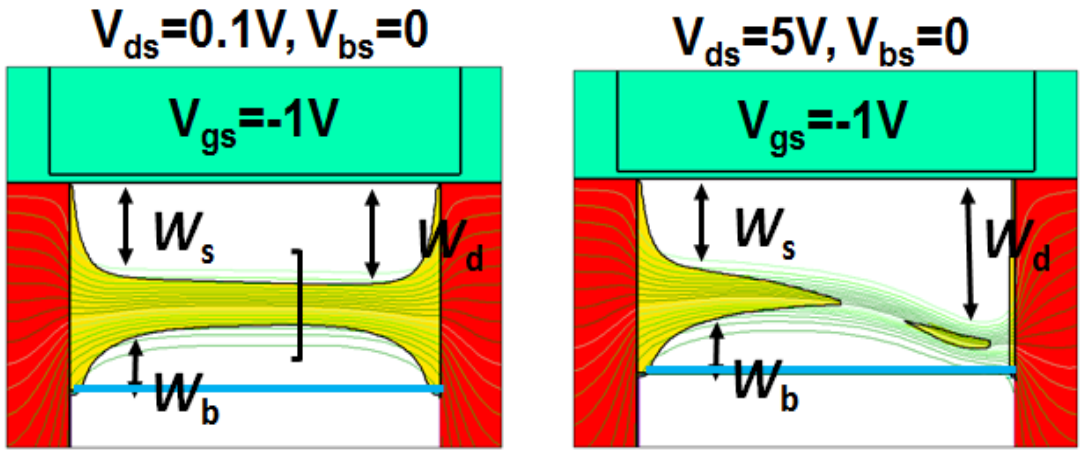


$$\mu_{\mathrm{leak,res}} = \frac{\mu_{0\mathrm{leak,res}}}{\left(1 + \left(\frac{\mu_{0\mathrm{leak,res}} \cdot E_{\mathrm{y}}}{DEP_{\mathrm{vmax}}}\right)^{\mathrm{DEPBB}}\right)^{\frac{1}{\mathrm{DEPBB}}}}$$

$$\mu_{0\mathrm{leak,res}} = DEP_{\mathrm{mue0}}$$

$$E_{\mathrm{y}} = \frac{V_{\mathrm{ds,res}}}{L_{\mathrm{ch}} - \mathrm{DEPRDRDL2}}$$

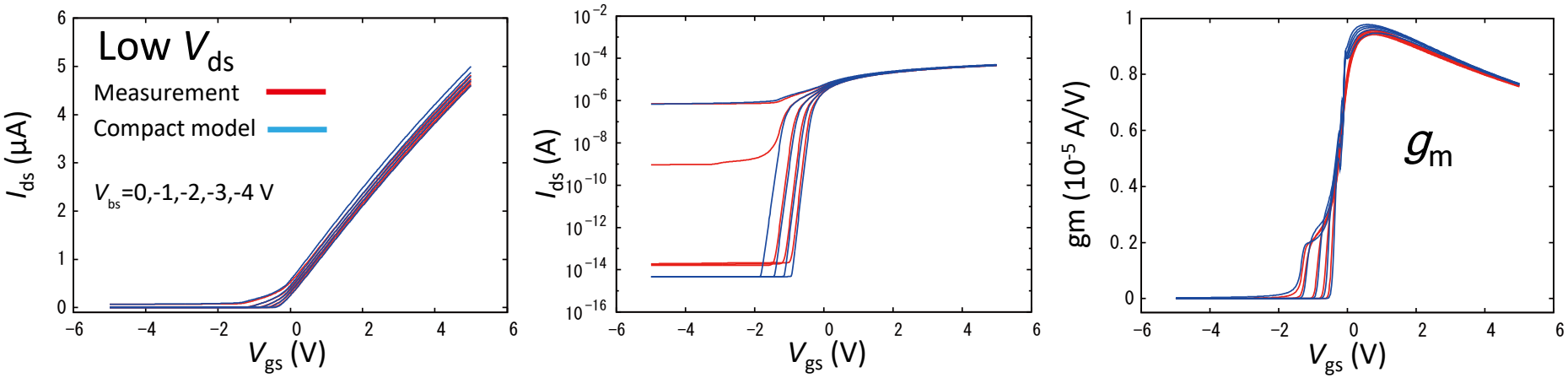
Resistive Current (I_{res}) at High V_{ds}



Potential at the pinch-off point

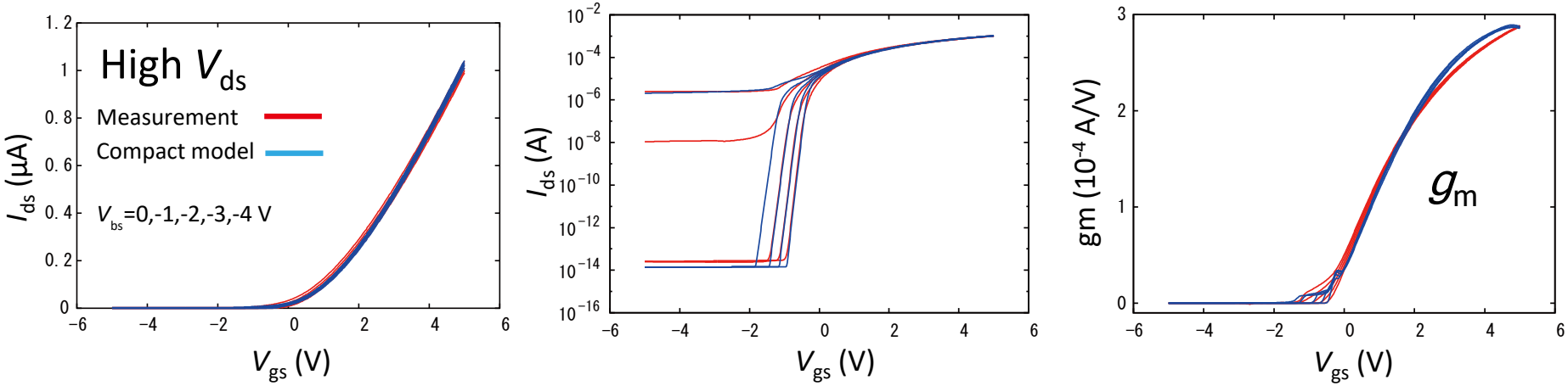
$$\phi_{\mathrm{f\,max}} = V_{\mathrm{gp}} + \frac{qN_{\mathrm{n}}\varepsilon_{\mathrm{Si}}}{C_{\mathrm{ox}}^2}\left\{1 - \sqrt{1 + 2\frac{C_{\mathrm{ox}}^2}{qN_{\mathrm{n}}\varepsilon_{\mathrm{Si}}}V_{\mathrm{gp}}}\right\}$$

I_{ds}-V_{gs} characteristics at low V_{ds}



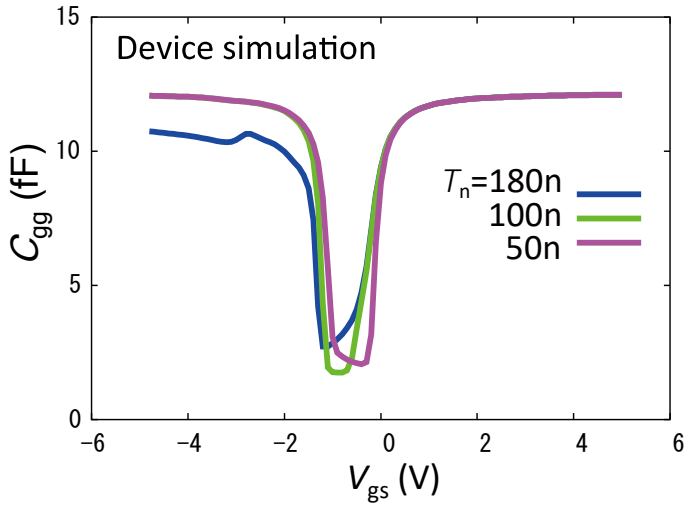
Good agreement with measurements is verified.

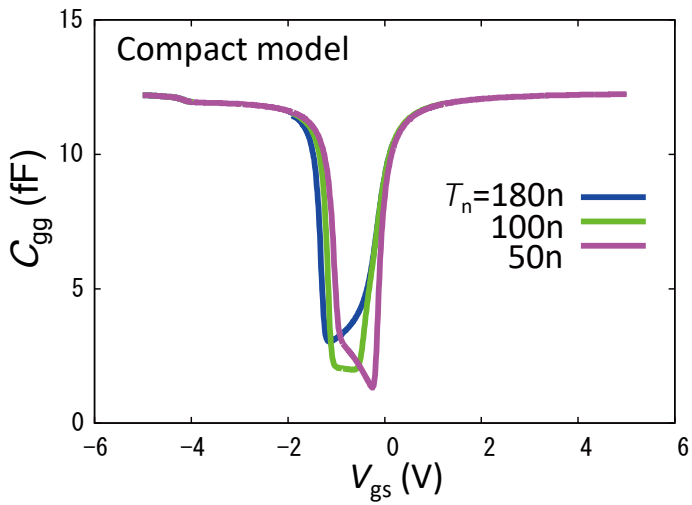
I_{ds}-V_{gs} characteristics at high V_{ds}



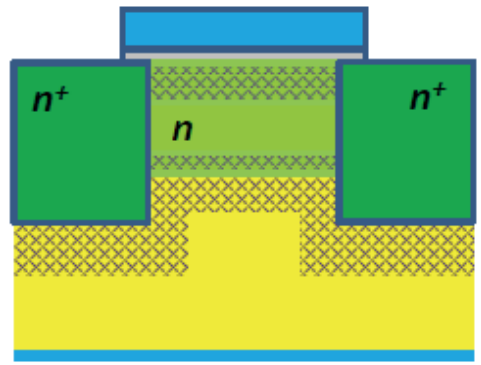
Good agreement with measurements is verified.

Capacitance Characteristics





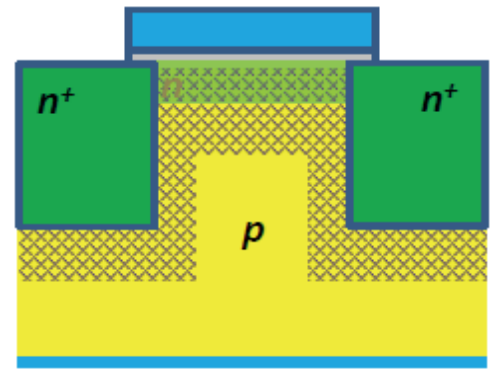
Thick surface layer



Partial depletion in the surface layer.

Capacitive coupling between gate and surface layer (n-type).

Thin surface layer



Full depletion in the surface layer.

Capacitive coupling between gate and substrate (p-type).

Summary

- A compact model for normally-on MOSFET is developed.
- Surface-potential-based approach to model the device captures device behavior consistently. The current and capacitance characteristics are verified against measurements and device simulation.
- The modeling approach is a viable solution for all technology generations.