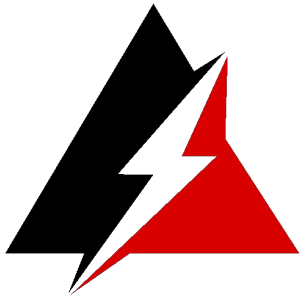

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11th International MOS-AK Workshop
(co-located with the IEDM and CMC Meetings)
Silicon Valley, December 5, 2018

Impact of Basal Plane Dislocations and Ruggedness of 10 kV 4H-SiC Transistors

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PowerAmerica is a U.S. Department of Energy WBG Semiconductor Manufacturing Institute

- The U.S Department of Energy launched the PowerAmerica Institute to Accelerate Adoption of Wide Band Gap (WBG) power electronics.
- PowerAmerica started operations in 2015 with $140M funds over 5 years, and is managed by North Carolina State University in Raleigh, NC USA.
- PowerAmerica addresses gaps in WBG power technology to enable U.S. manufacturing job creation and energy savings.

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PowerAmerica is a Member Led Manufacturing Institute Active in **All Areas** of the Power GaN/SiC Supply Chain

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SUNY Polytechnic Institute

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Naval Research Laboratory Washington, DC

Argonne National Laboratory

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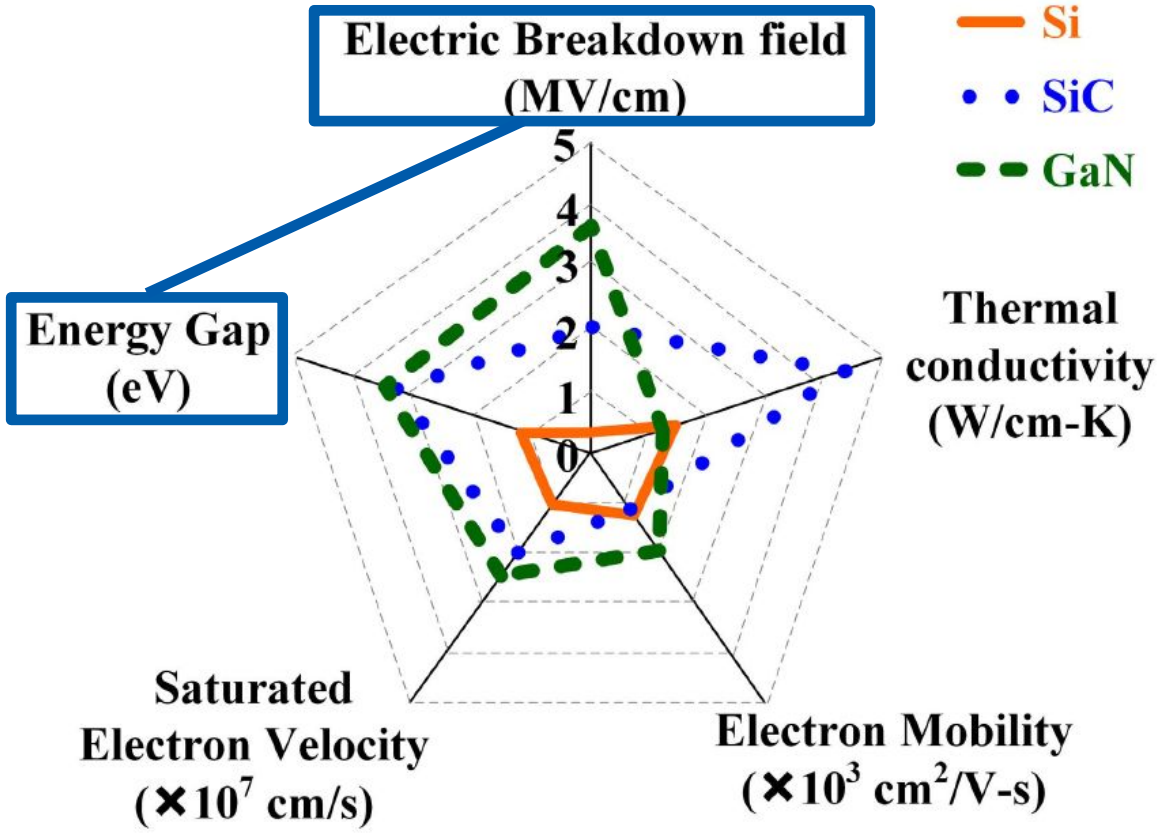
PEIC Power Electronics Industry Collaborative

iNEMI Advancing manufacturing technology

SiC and GaN Power Devices Allow for More Efficient and Novel Power Electronics



Device Thickness

$$W_N = \left(\frac{3}{2}\right)\left(\frac{V_B}{E_C}\right)$$

Device Resistance

$$R_{ON,SP} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_N \varepsilon_S E_C^3}$$

Large Bandgap and Critical Electric Field allow for high voltage devices with thinner layers: lower resistance and associated conduction losses

Thinner layer and low specific on-resistance allow for smaller form factor that reduces capacitance: higher frequency operation, reduced size passives

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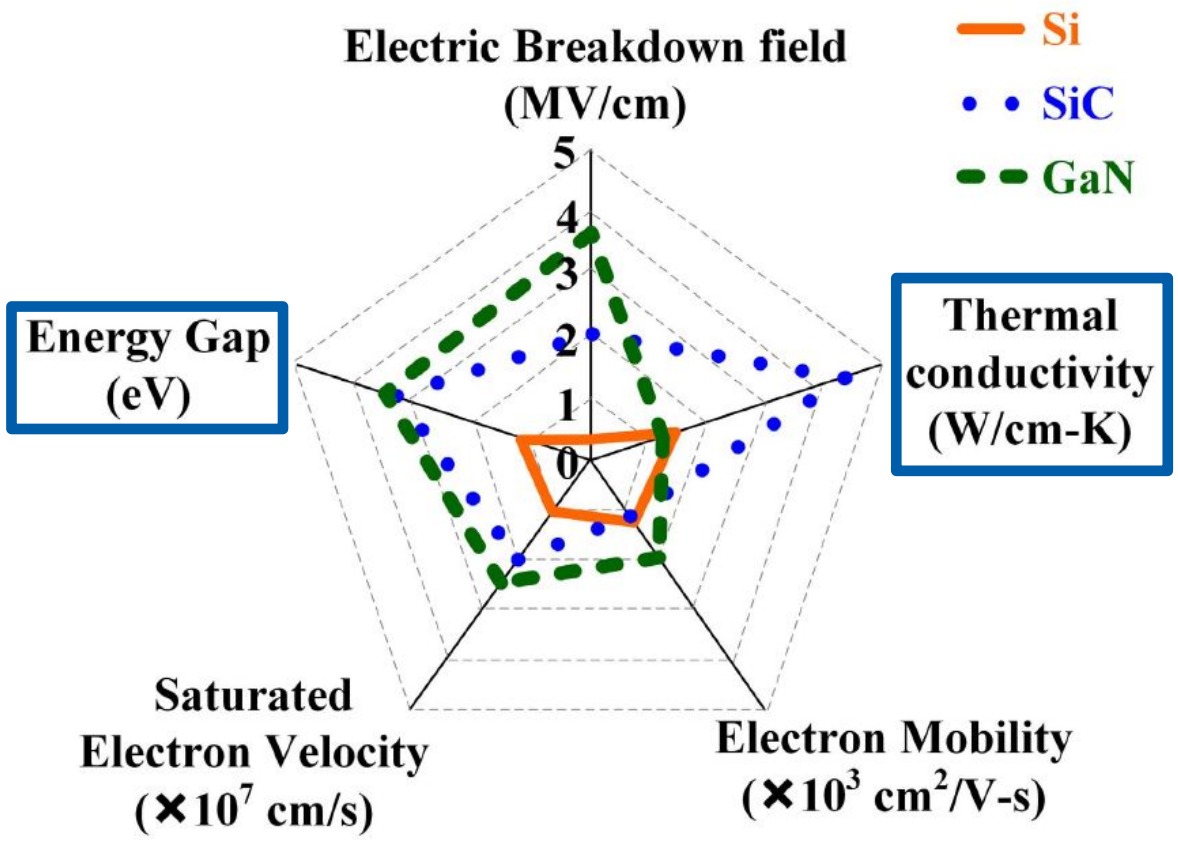
Large SiC Bandgap and Thermal Conductivity Enable Robust High Temperature Operation with Reduced Cooling



SiC/GaN devices enable **more efficient, lighter, smaller form factor** power electronics operating at high frequencies, and at elevated temperatures with reduced cooling.

Large Bandgap results in relatively low intrinsic carrier concentration: low leakage and robust high temperature operation

Large Thermal Conductivity: high power operation with reduced cooling requirements

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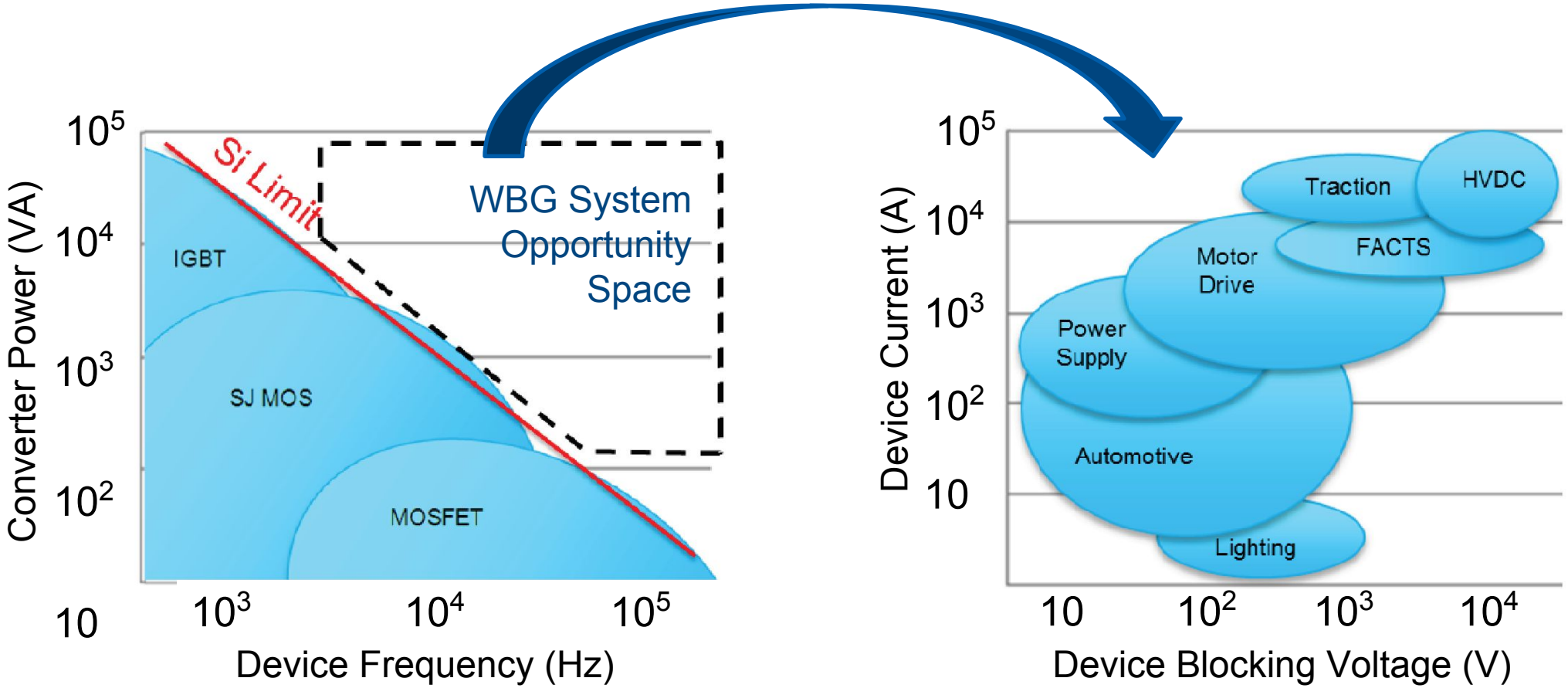
WBG Devices Are Uniquely Positioned to Enable Next Generation Power Electronics Growth



Graphs: Isic C. Kizilyalli *et al.*, ARPA-e Report 2018
https://arpa-e.energy.gov/sites/default/files/documents/files/ARPA-E_Power_Electronics_Paper-April2018.pdf

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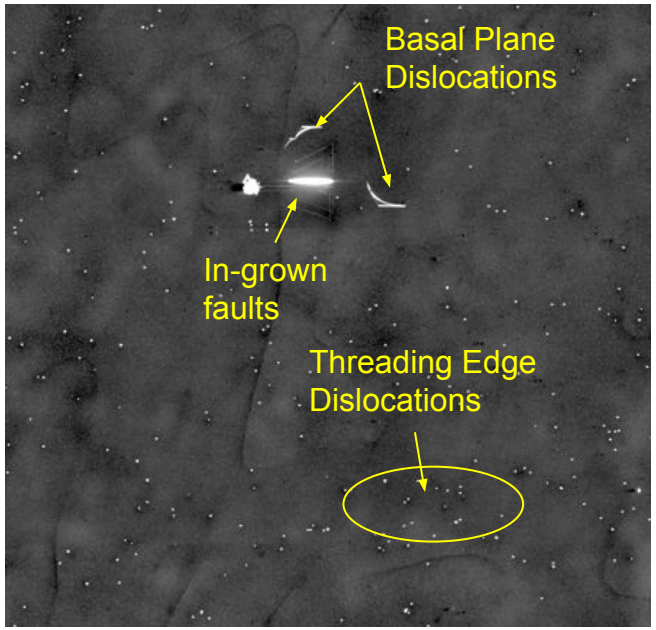
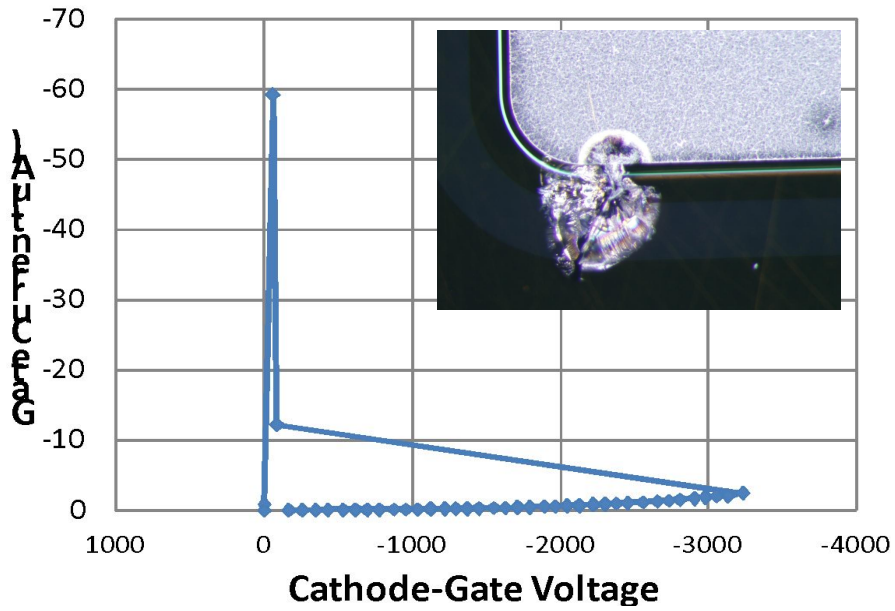
Reliability and Ruggedness are Prerequisites for Wide SiC Power Electronics Adoption

- Material quality and fabrication improvements contribute to device reliability
  - Minimize wafer material defects and improve planarity
  - Eliminate defect generation during processing
- Ruggedness is a device design trade-off
  - Design rugged SiC devices with safe operating areas similar to Si





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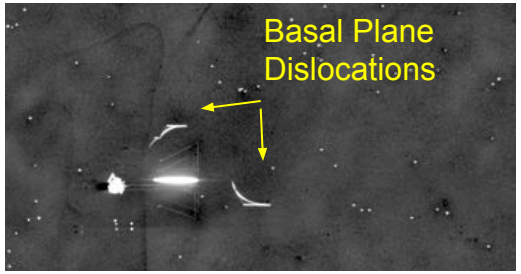
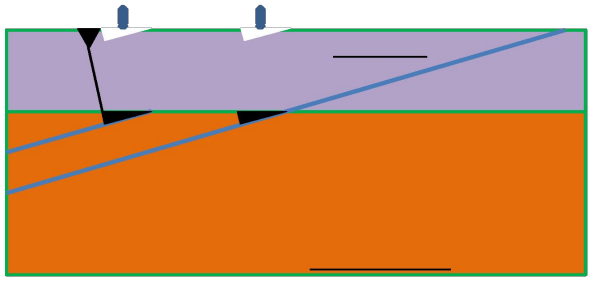
Basal Plane Dislocations Can Compromise SiC Device Reliability and Performance

- Basal Plane Dislocations (BPDs) are defects that can propagate from the substrate to the epitaxial layers where devices are fabricated (material defects).
- Basal plane dislocations can also be generated during the high temperature SiC ion implantation process (processing defects).
- Under bipolar current flow, electron-hole pair recombination at BPDs induces stacking faults, which degrade device electrical characteristics.
- Electron-hole conduction occurs in bipolar devices and in certain modes of unipolar device operation; unipolar devices are also affected by BPDs.
- Techniques are being developed to convert substrate BPDs into benign “Threading Edge Dislocations”, and to eliminate BPD generation during implantation.





BPD induced stacking fault related degradation has limited adoption of high voltage SiC power devices

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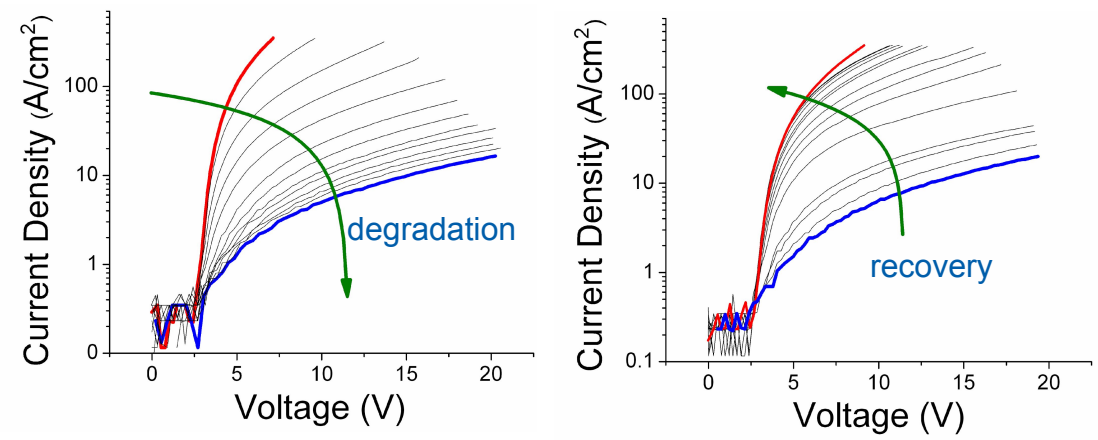
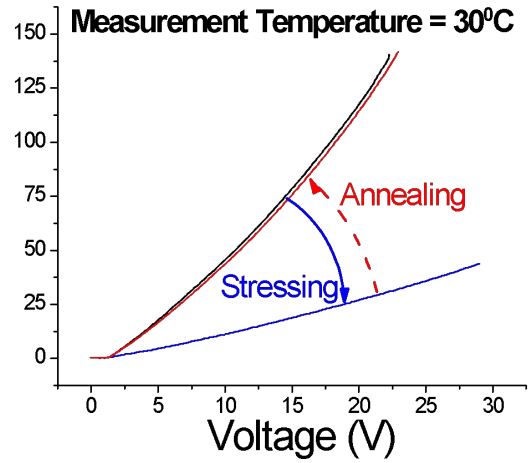
Bipolar Current Flow in the Thick Drift Epilayers of SiC Devices Can Degrade Electrical Characteristics

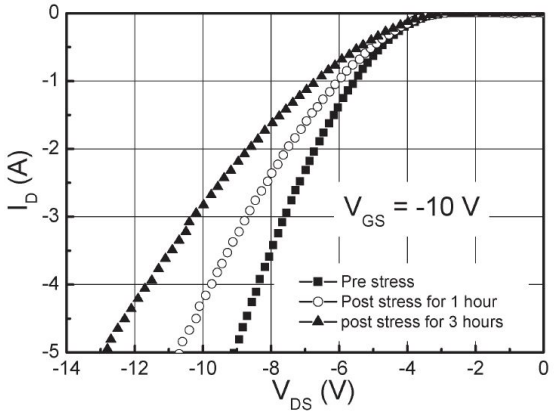


PiN diode V_f degradation and recovery[1]

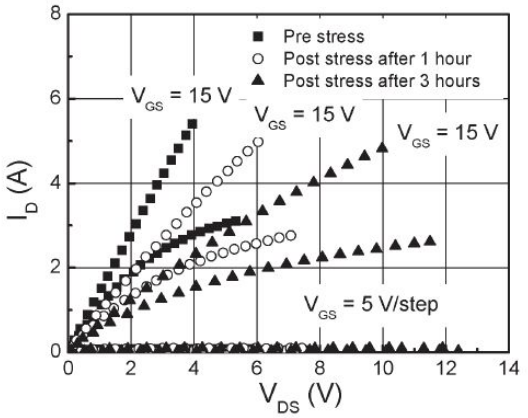


Merged PiN-Schottky (MPS) Diode V_f degradation and recovery[1]

Diodes



Degradation of the body diode V_f in a 10 kV DMOSFET[2]



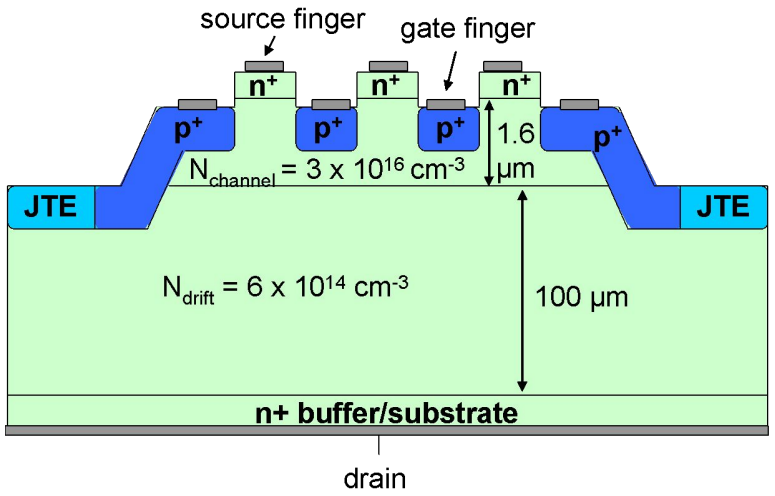
Degradation of on-state characteristics in a 10 kV DMOSFT[2]

MOSFET

[1]J.D. Caldwell et al., MRS Procedings, 2008

[2]Agarwal et al., IEEE EDL, vol. 28, p. 587, 2007

JFETs with 100-µm drift Epilayers were Used to Investigate Bipolar Current Related Degradation



1.5 x 10^{-3} cm^2 active-area JFET

100 µm drift layer

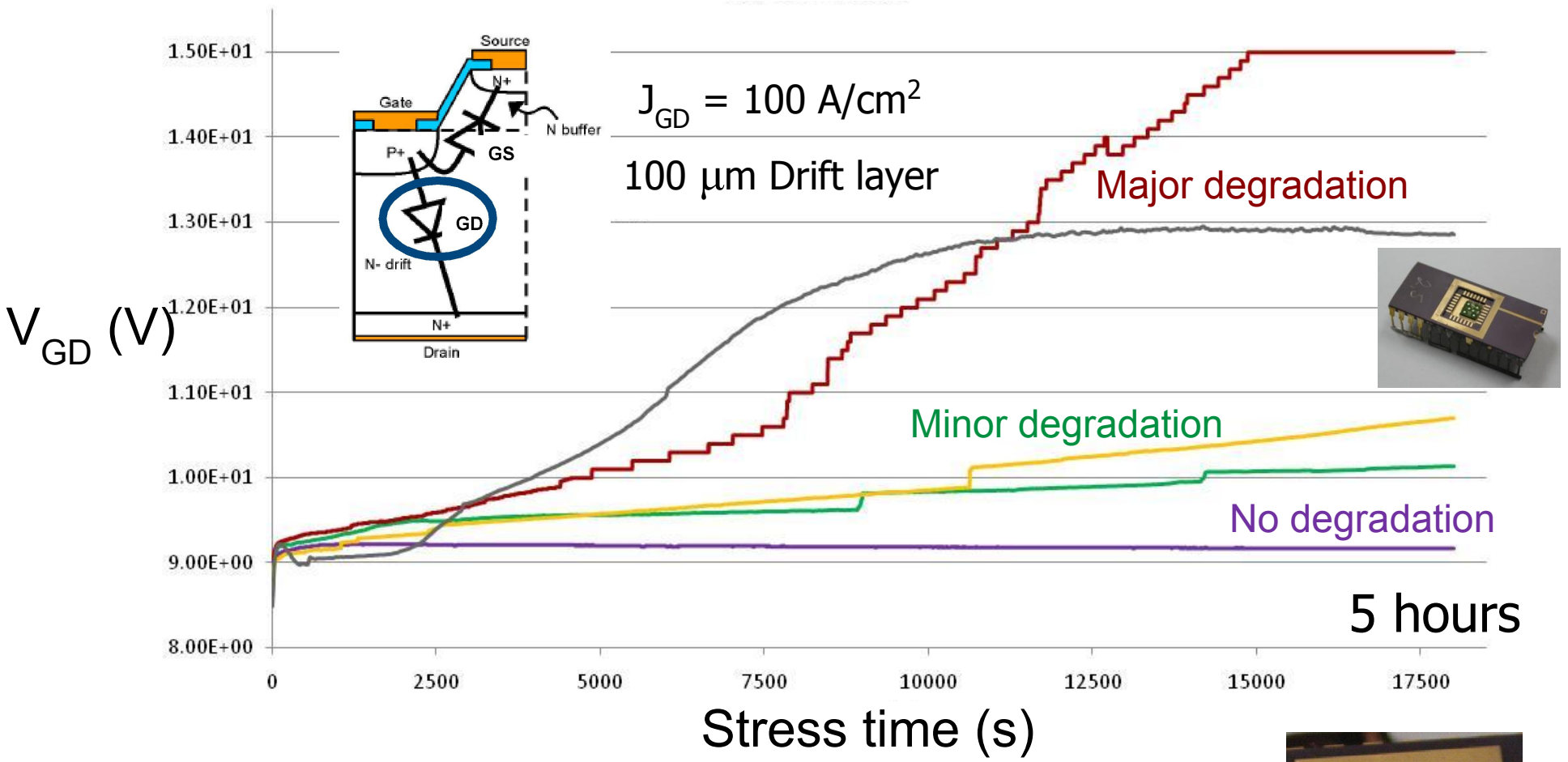
Row/Col	1	2	3	4	5	6	7	8	9
1			5.5	4.4	4.4	1769.3	8.1		
2		9027.0	7.6	9023.7	9045.0	9018.0	4221.0	4.4	
3		34.9	9036.0	9054.0	9045.0	9072.0	7980.9	9009.0	
4		9054.0	4363.7	9018.0	2682.1	9032.6	9063.0	8736.0	26.5
5		9036.0	5695.0	9054.0	4.4	9045.0	9009.0	9108.0	4.3
6		8877.5	9032.6	515.7	9009.0	4944.1	9014.8	9045.0	
7		6.2	9041.5	7257.6	9059.3	9009.0	9072.0	4.3	
8			4.4	5834.8	167.7	4.3	4.4		

Gate-drain breakdown voltage wafer map

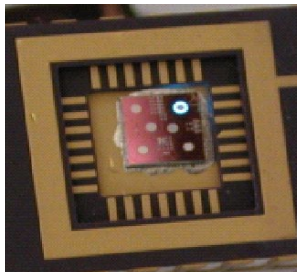
9 kV at 0.1 mA/cm^2 overall yield is 67%

Small JFET area decouples electrical characteristics from the deleterious effects of multiple material and processing defects

Bipolar Current Stressing of JFETs can Lead to Forward Gate-Drain Voltage Degradation



JFETs were subjected to a forced bipolar gate-drain current density of 100 A/cm^2 (920 W/cm^2)



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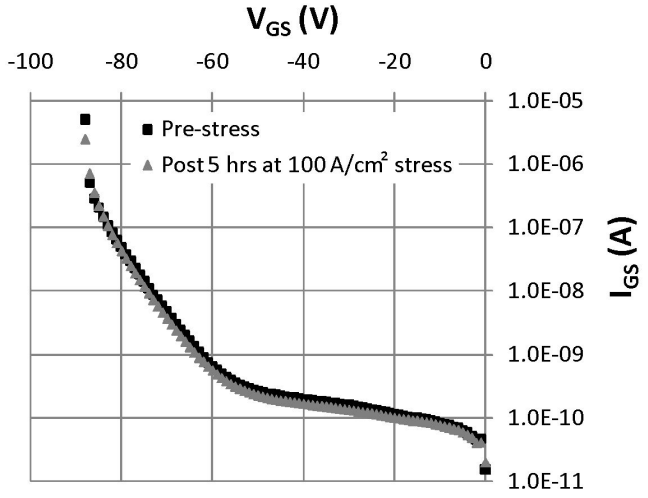
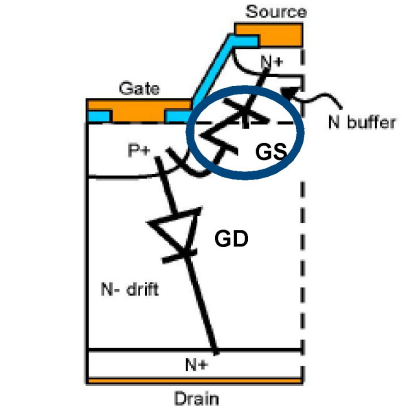
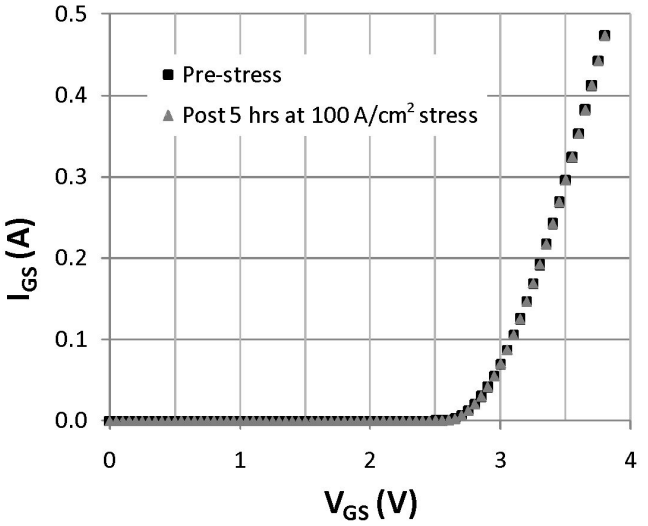
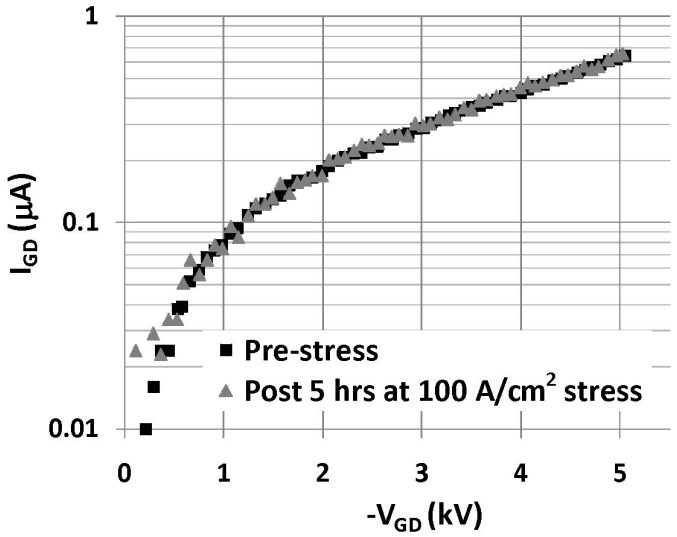
Bipolar Current Degrades Forward Gate-Drain Voltage; Other JFET Diode Characteristics are Unaffected

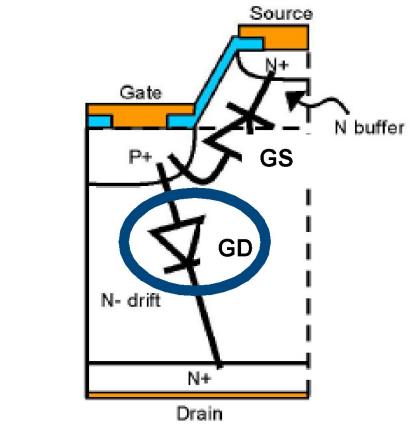




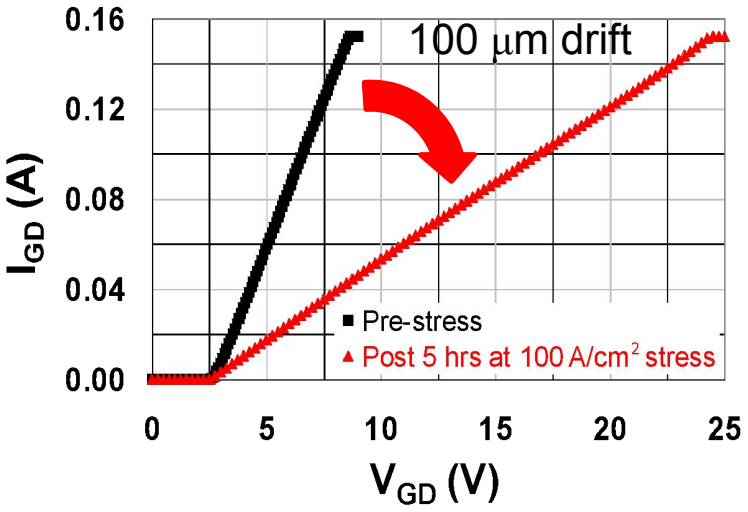
Gate-Source Diode







Gate-Drain Diode



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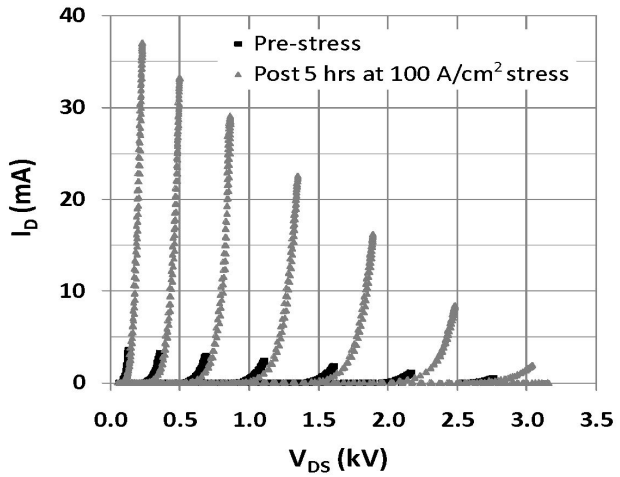
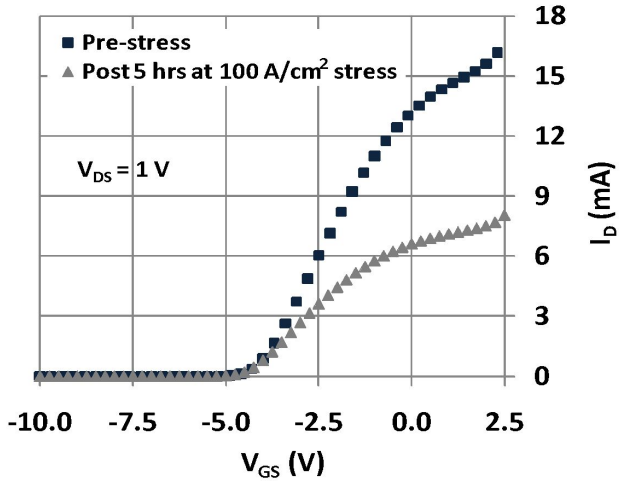
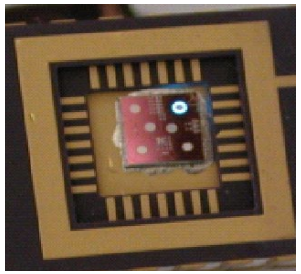
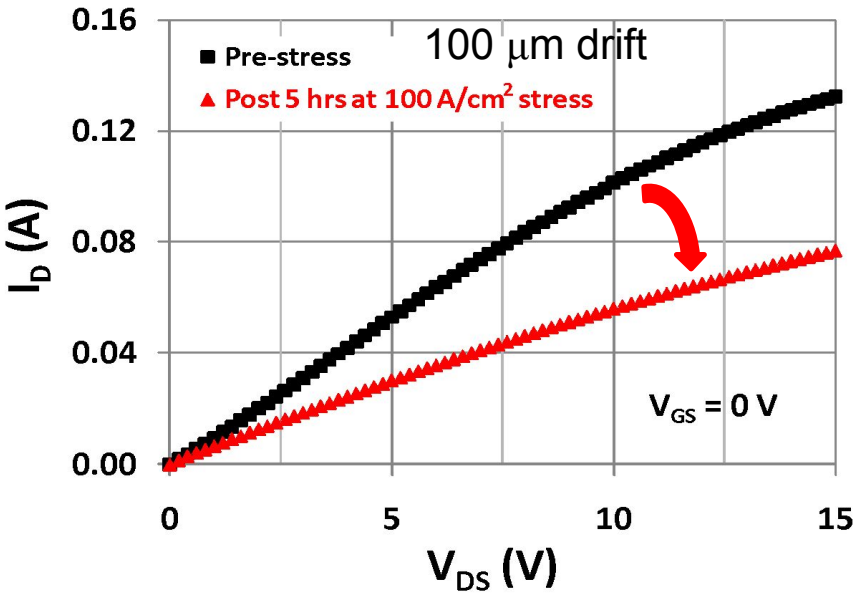
Bipolar Current Flow Degrades Trans-conductance and Forward On-state Current

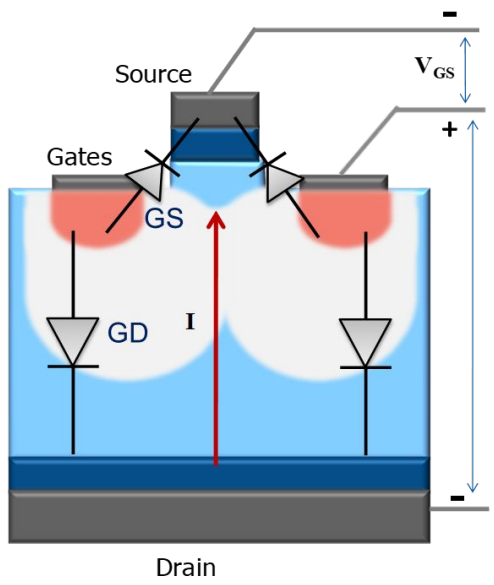






Blocking Voltage is Unchanged, Trans-conductance and On-state Degrade





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Degraded JFETs were Annealed at 350 ˚C for 96 hours in a N_2 Environment

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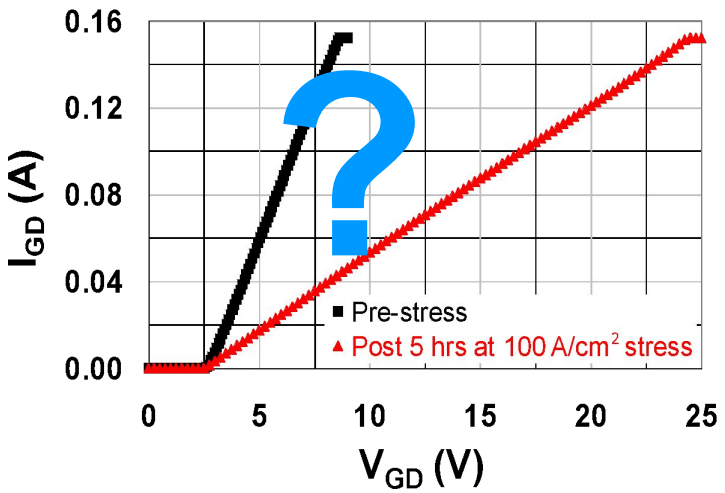
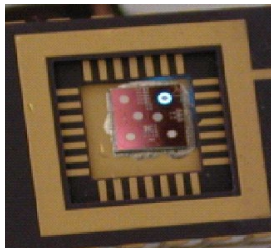
Annealing Reverses Bipolar Current Induced Degradation in SiC PiN and MPS Diodes

350 ˚C JFET anneal conditions:

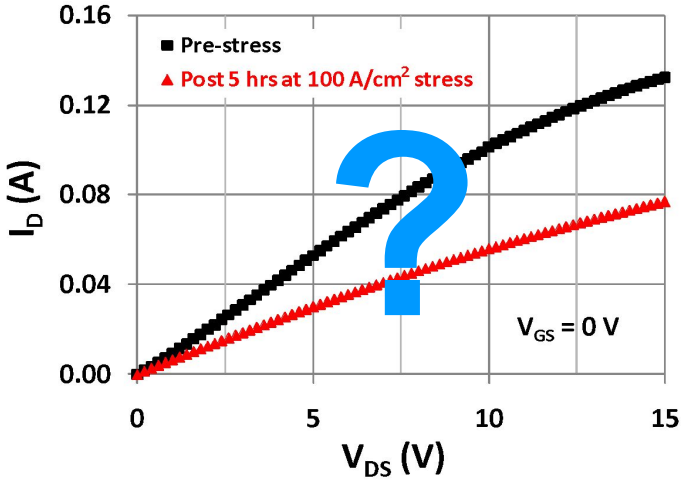
- 4 cycles of 24 hours with ramp up and ramp down
- 96 hours total of continuous anneal

Gate-drain diode degradation



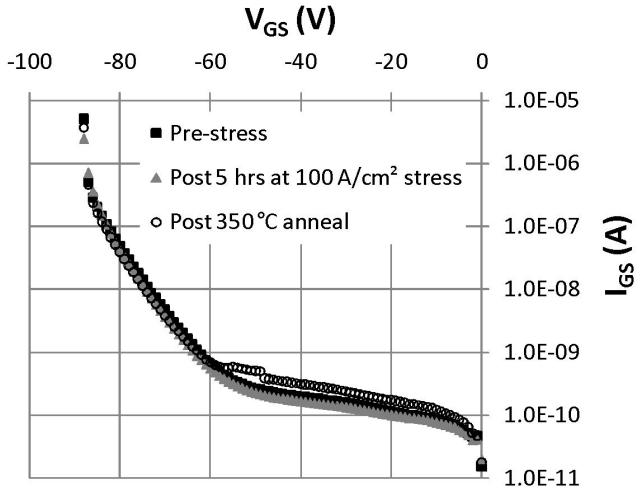


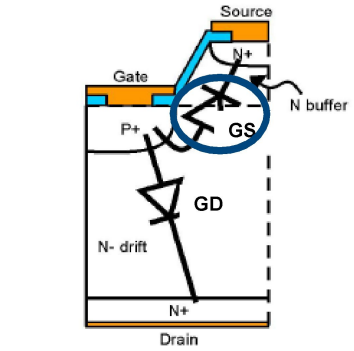
Gate-drain diode degradation



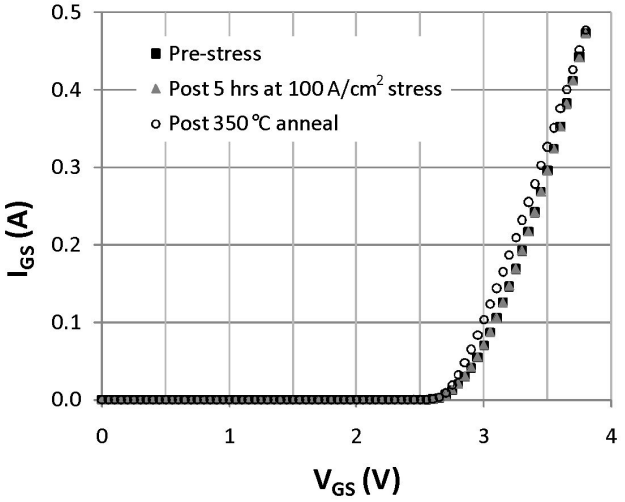
Will annealing reverse BPD related degradation in JFETs?
Does annealing affect non-degraded JFET electrical characteristics?

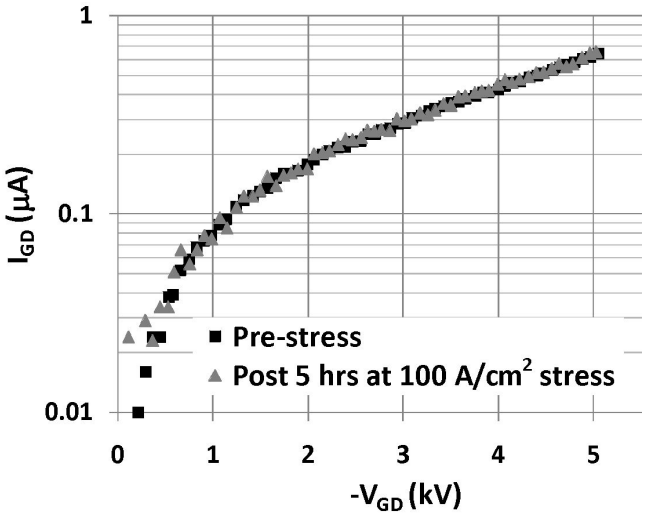
JFET Annealing at 350 ˚C Reverses Gate-Drain Forward Voltage Degradation

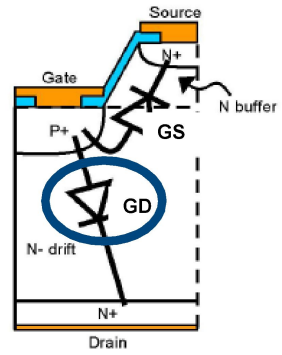




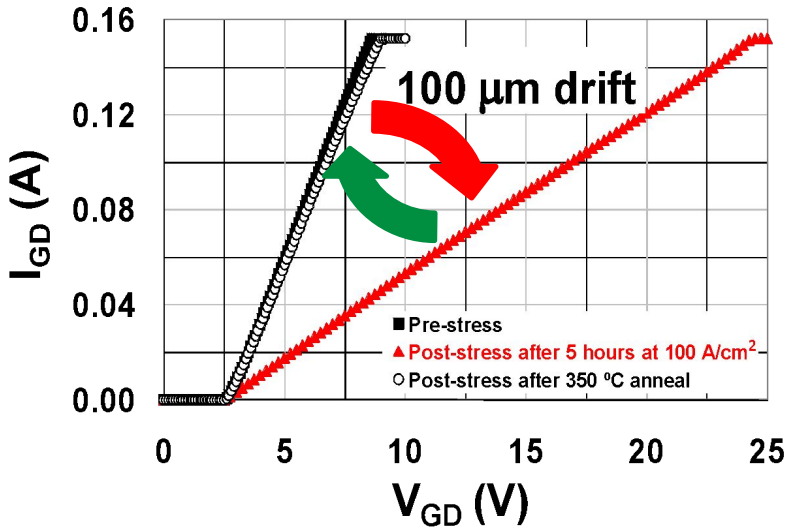
Gate-Source Diode







Gate-Drain Diode



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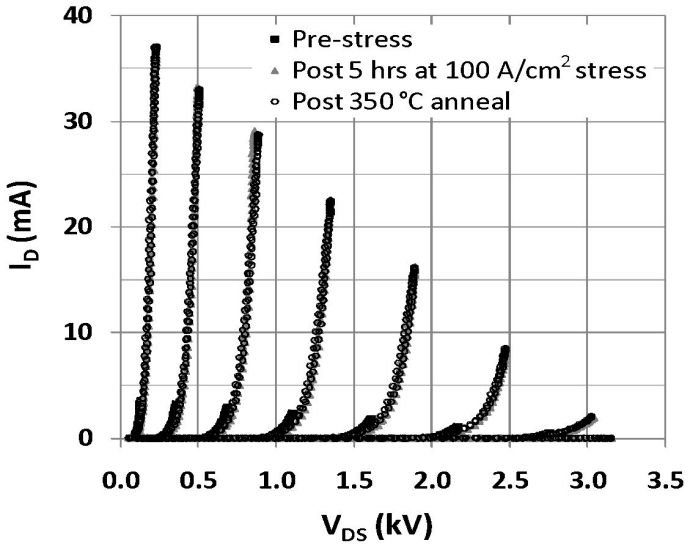
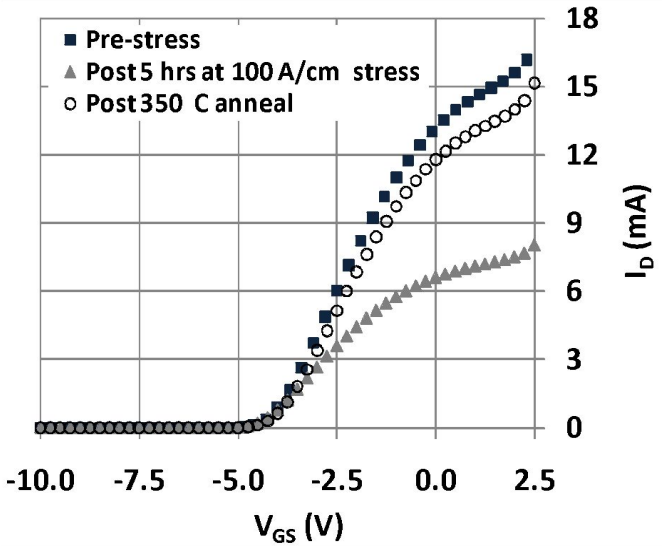
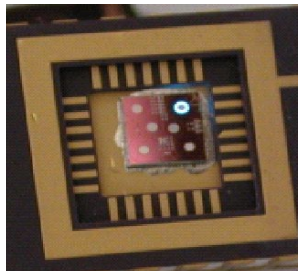
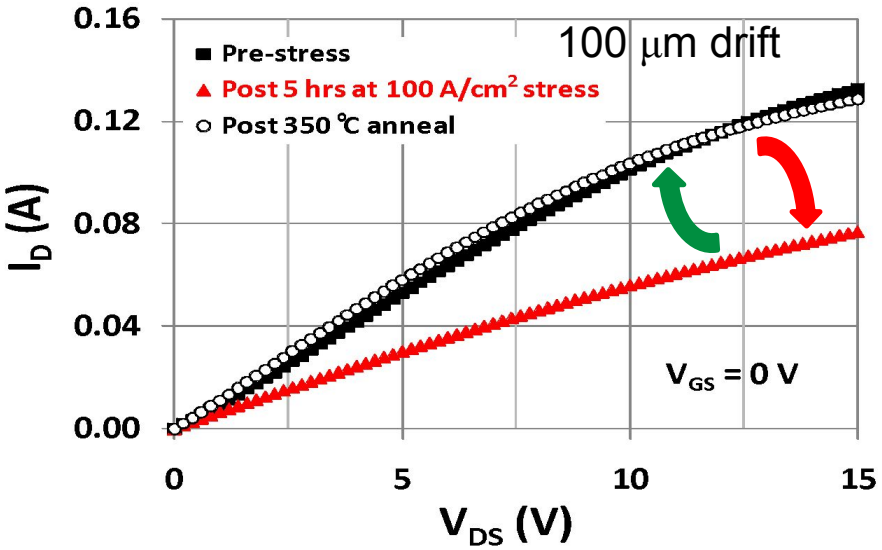
JFET Annealing at 350 ˚C Reverses Forward On-state Current Degradations



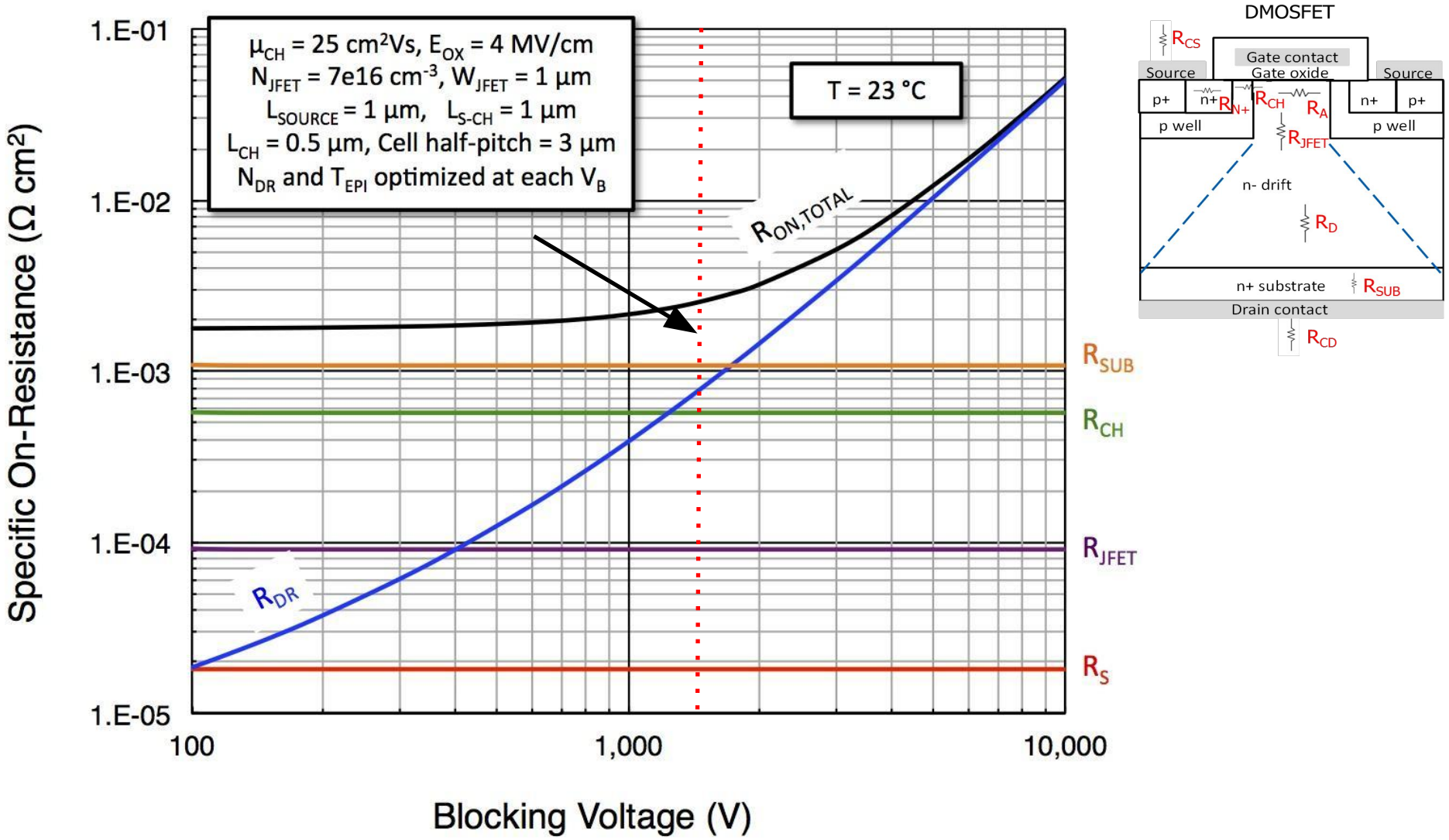






First and only SiC transistors to demonstrate full recovery of their BPD degraded electrical characteristics

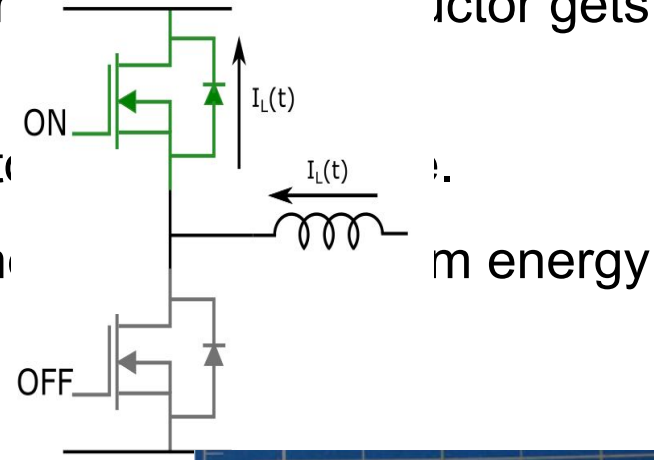
Trade-offs in Resistance and Ruggedness Drive SiC MOSFET Optimization

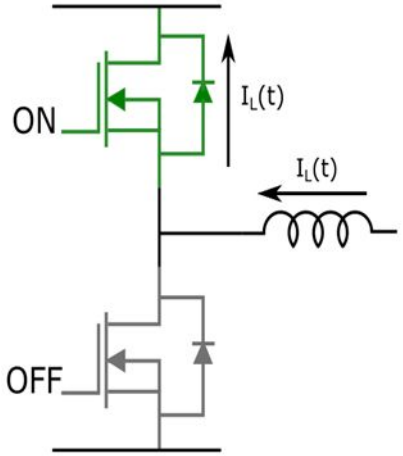


Graph: J. Cooper ECSCRM 2016

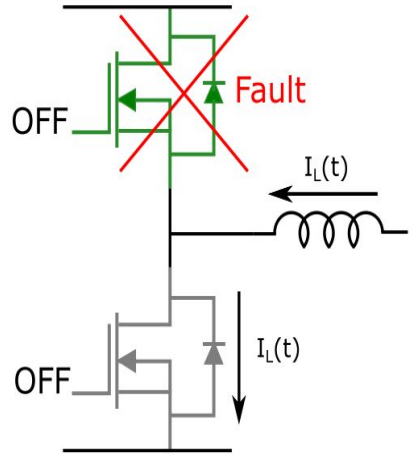
Avalanche Ruggedness Testing Defines Device Safe Operating Area

- During the fault condition the energy stor[illegible]ctor gets dumped into the lower MOSFET.
- In this case, the lower MOSFET goes int[illegible].
- MOSFET avalanche ruggedness is defin[illegible]m energy dissipated without catastrophic damage.

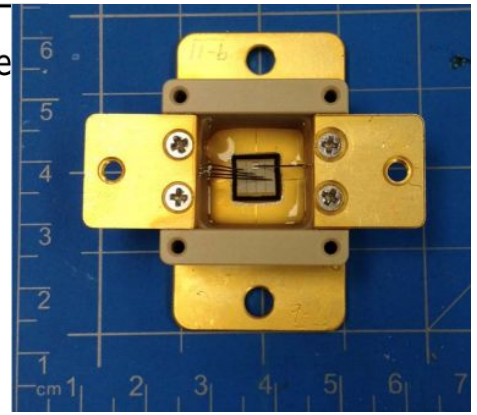




Normal operation



Avalanche condition



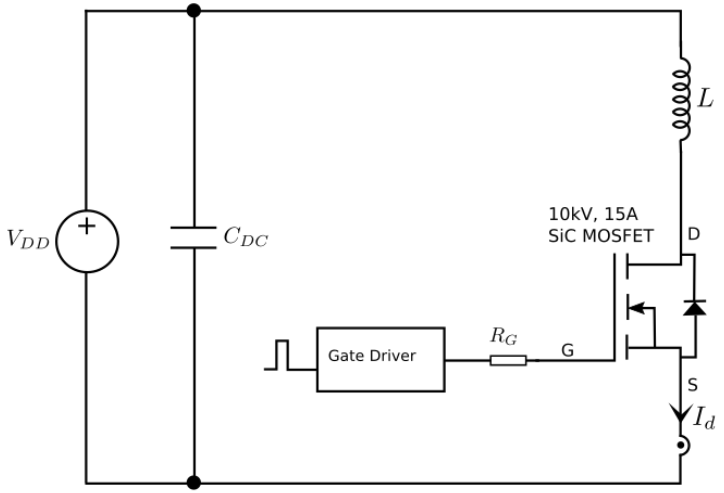
Gen-3 10 kV MOSFET
Active area 32 mm^2

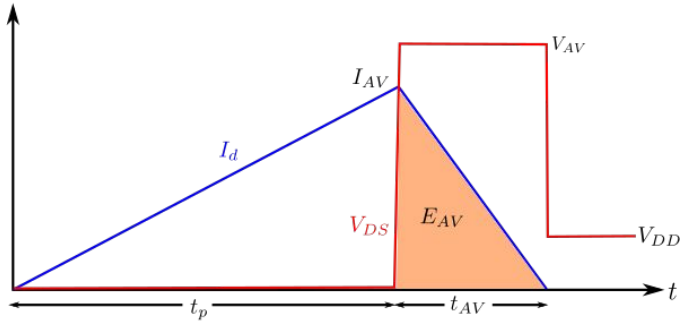
Investigate avalanche ruggedness of Wolfspeed Gen–3 10 kV/15 A SiC MOSFETs

Unclamped Inductive Switching Testing Characterizes Avalanche Ruggedness

Single pulse Unclamped Inductive Switching:

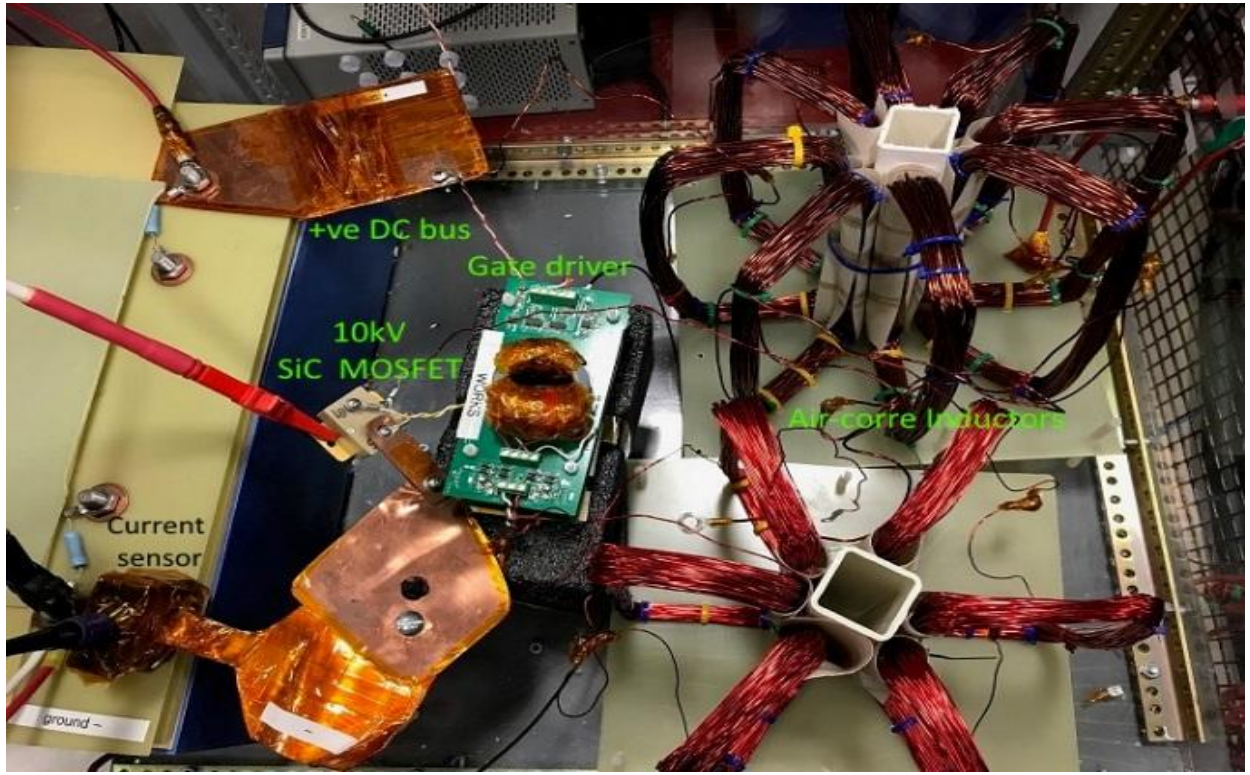
- The inductor L is charged to desired I_{AV}.
- Turning the DUT gate OFF results in avalanche condition.
- The device voltage shoots up to the avalanche voltage.
- Avalanche energy E_{AV} greater than the critical energy results in permanent device failure.
- Avalanche ruggedness is measured by E_{AV}.
- Inductor L is varied to obtain avalanche at different peak current levels I_{AV}.



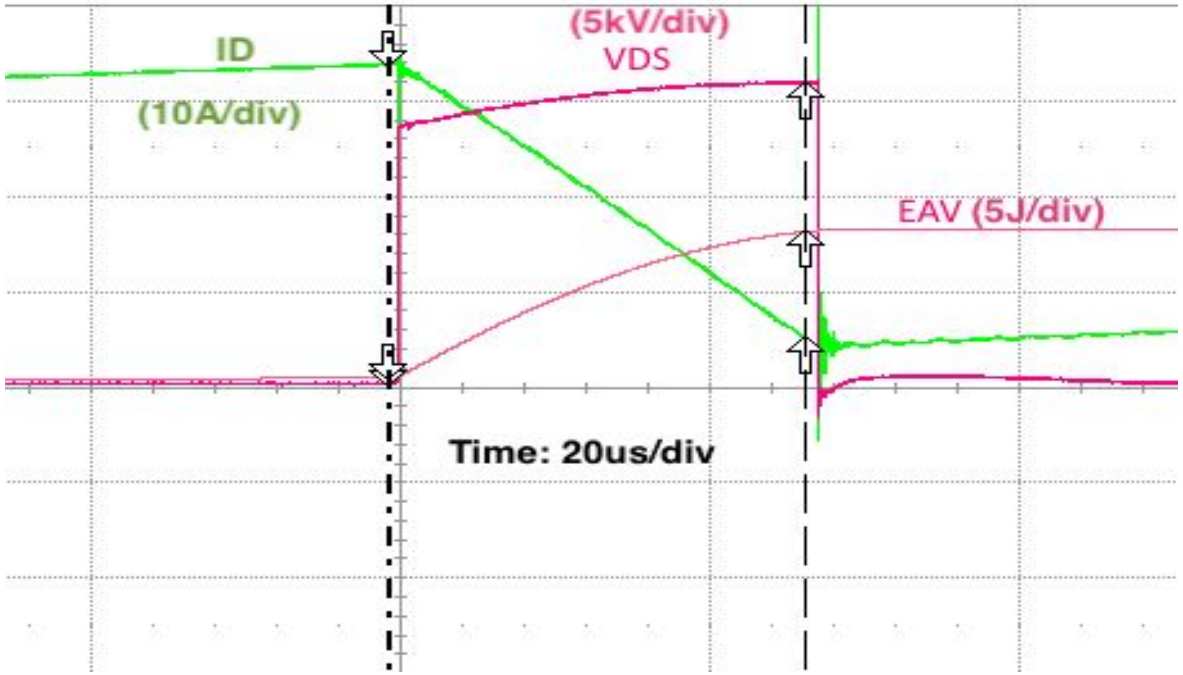


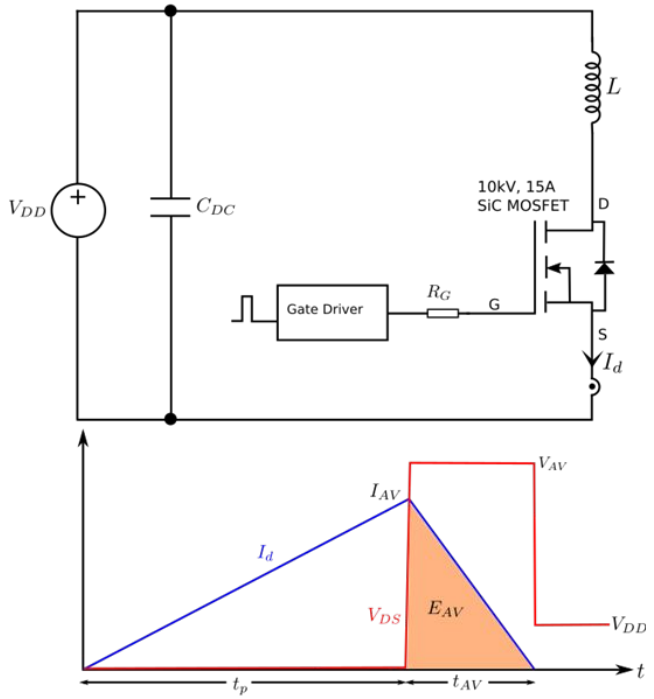
Experimental Set-up of Single Pulse Unclamped Inductive Switching

- Air core inductors
- Pearson CT 3972
- Tektronix P6015A HV probe



Representative Unclamped Inductive Switching Waveforms to Catastrophic MOSFET Failure



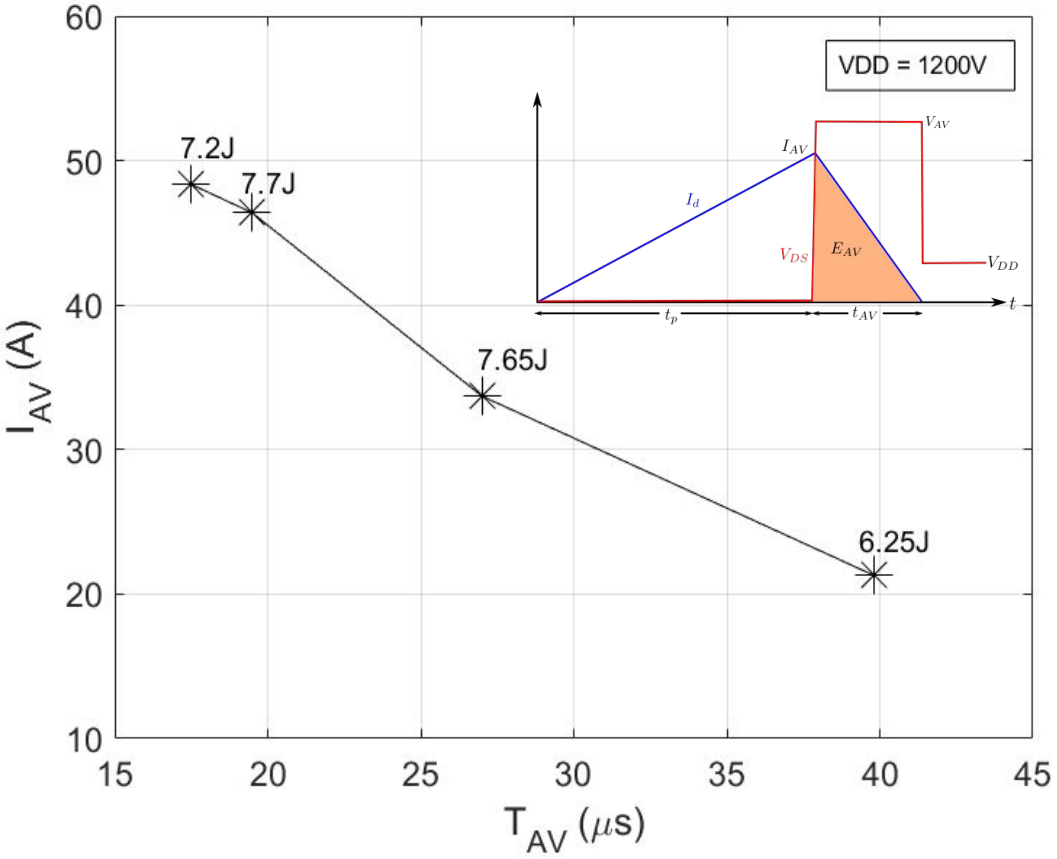


Avalanche test waveforms for a 10kV SiC MOSFET at room temperature

E_{AV} = 7.65 J, I_{AV} = 34 A, t_{AV} = 27 µs, **V_{AV} = 15.88 kV**, V_{DD} = 1200 V, L = 14 mH

MOSFETs Exhibit Average Avalanche Energies of 7.2 J in Unclamped Inductive Switching Testing

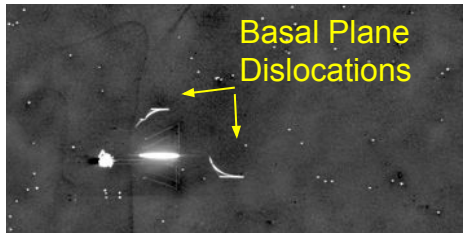
- Inductor L is varied to obtain four different avalanche currents.
- The average avalanche energy at failure is about 7.2 Joules.
- Extrapolating the I_{AV} - t_{AV} curve to the rated current of 15 A results in t_{AV} > 40 µs.
- Typical gate drives interrupt faults in well below 40 µs.

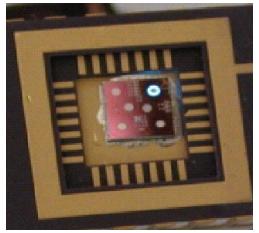


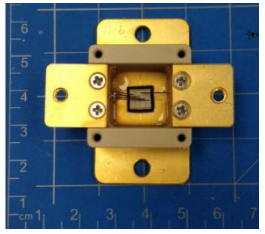
The 10-kV/15-A MOSFETs exhibit avalanche ruggedness with a > 40 µs time to catastrophic failure

High Voltage SiC Devices are Making Strides in Establishing Their Ruggedness and Reliability

- The effects of bipolar stress induced stacking faults on the electrical characteristics of 10 kV SiC devices have been investigated.
- Bipolar stress in the presence of BPDs can lead to forward gate-drain *p-n* junction and on-state conduction degradations that are fully recovered by high temperature annealing.
- Avalanche ruggedness of 10 kV/15 A SiC MOSFETs is characterized using Unclamped Inductive Switching testing.
- The average avalanche energy prior to catastrophic failure is 7.2 J, which is superior to that of earlier generations of 10 kV SiC MOSFETs.
- At the 15 A rated current, the time to MOSFET avalanche catastrophic failure exceeds 40 µs, which is much larger than typical gate drive fault interruption times.







PowerAmerica Accelerates WBG commercialization

POWERAMERICA

11th International MOS-AK Workshop
(co-located with the IEDM and CMC Meetings)
Silicon Valley, December 5, 2018

WBG device fabrication in large-volume Si foundries exploits economies of scale and is key in lowering cost.

Minimizing capital expenditures by exploiting the mature Si-processing capability lowers fabrication costs.

A workforce well trained in WBG power electronics is key in creating the large device demand that will spur volume manufacturing with its cost-lowering benefits.

PowerAmerica funds building-block projects in multiple areas of the WBG supply chain that synergistically culminate in large-scale WBG power electronics adoption.

Questions?

V. Veliadis