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MODENA E REGGIO EMILIA

A Physics-Based Compact Model of Resistive Random Access Memory for Emerging Applications

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Motivation and Purpose

- RTN is a critical issue for RRAM devices (memory / synapse) but it can also be exploited as an entropy source (e.g., in RNGs and PUFs).
- A Compact Model for RTN in RRAMs is still missing.
- The first Verilog-A Compact Model of RTN in RRAMs:
 - Valid in both resistive states.
 - Easily tweakable and adaptable to a variety of materials.
 - Accounts for the intrinsic randomness in the number of defects (i.e., it includes also multi-level RTN) contributing to the RTN and their properties.
 - Can be steadily integrated in existing RRAM device compact models to perform advanced simulations and circuit design for many applications.
- We show how it can be used in the design of the building block of a Truly-Random Number Generator circuit.

Outline

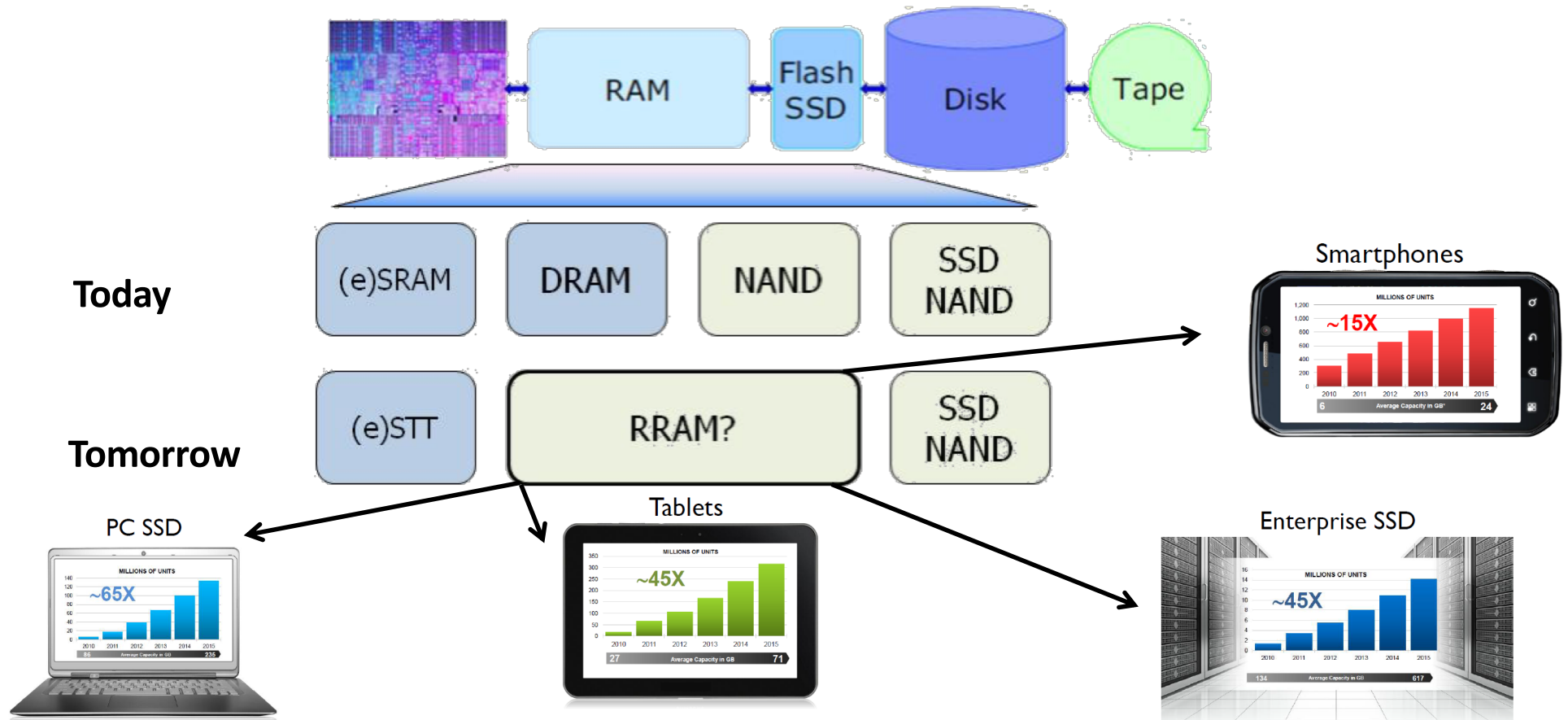
- Introduction
- The RRAM Compact Model
 - The Resistance Model
 - Charge Transport
 - Switching Dynamics (set and reset)
 - Variability
- Including RTN in the Compact Model
 - RTN physics in RRAM
 - Compact Model of RTN in LRS and HRS
 - Validation and Implementation
- Applications
 - RTN-based True-RNG Circuit
 - Logic-in-memory 1-bit Full-Adder
- Conclusions

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Introduction

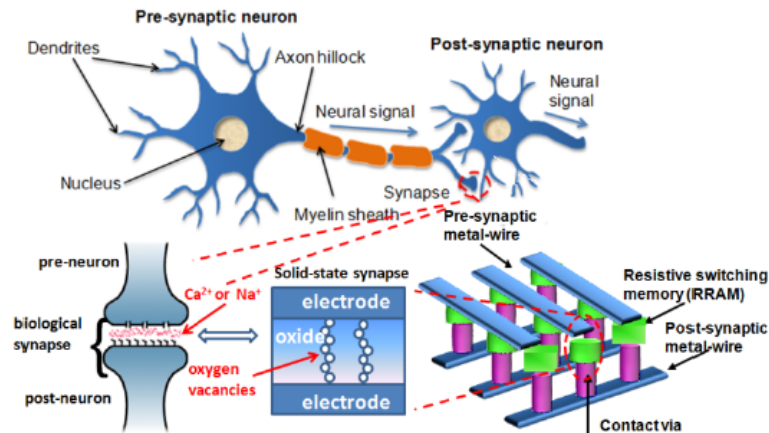
Memory hierarchy: filling the gap



Introduction

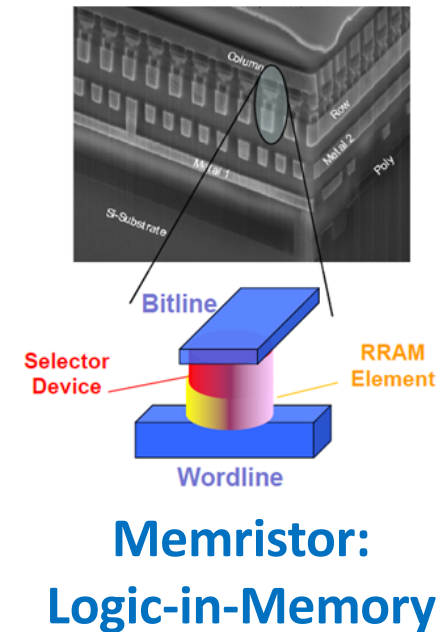
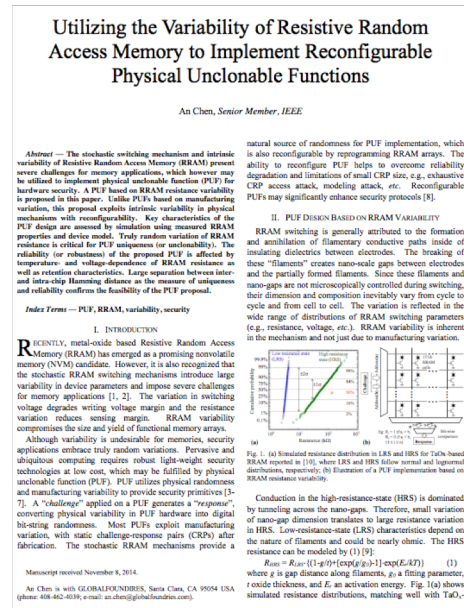
HfO₂-based device: *not only NVM!*

Proposed Applications:



Neuromorphic Computing:
Hardware Synapse

Intrinsically Secure Device:
Unclonable Circuits



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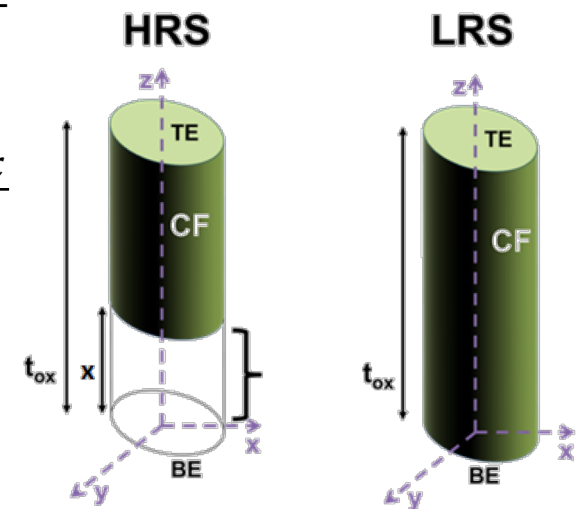
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The Resistance Model

- We model the resistance of the RRAM by assuming:
 - A simplified regular shape of the CF (constant S across CF length)
 - Reading conditions (i.e., low applied field)
 - Full CF in LRS (Ohmic transport)
 - Impact of temperature is neglected but can be easily incorporated in the ρ_{CF} term
 - Ruptured CF in HRS \rightarrow barrier (Trap-Assisted Tunneling conduction)
 - Includes the effect of temperature with an Arrhenius activation term
- Parameters:
 - k estimated by physics-based simulations including TAT
 - E_R extracted from R measurement in HRS at different T
 - ρ_{CF} is taken from the literature

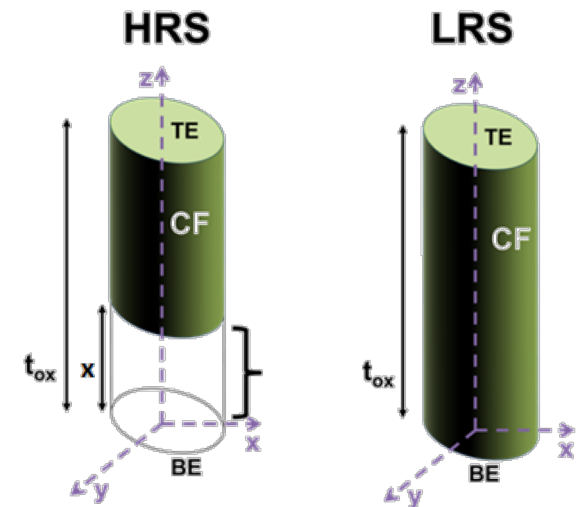
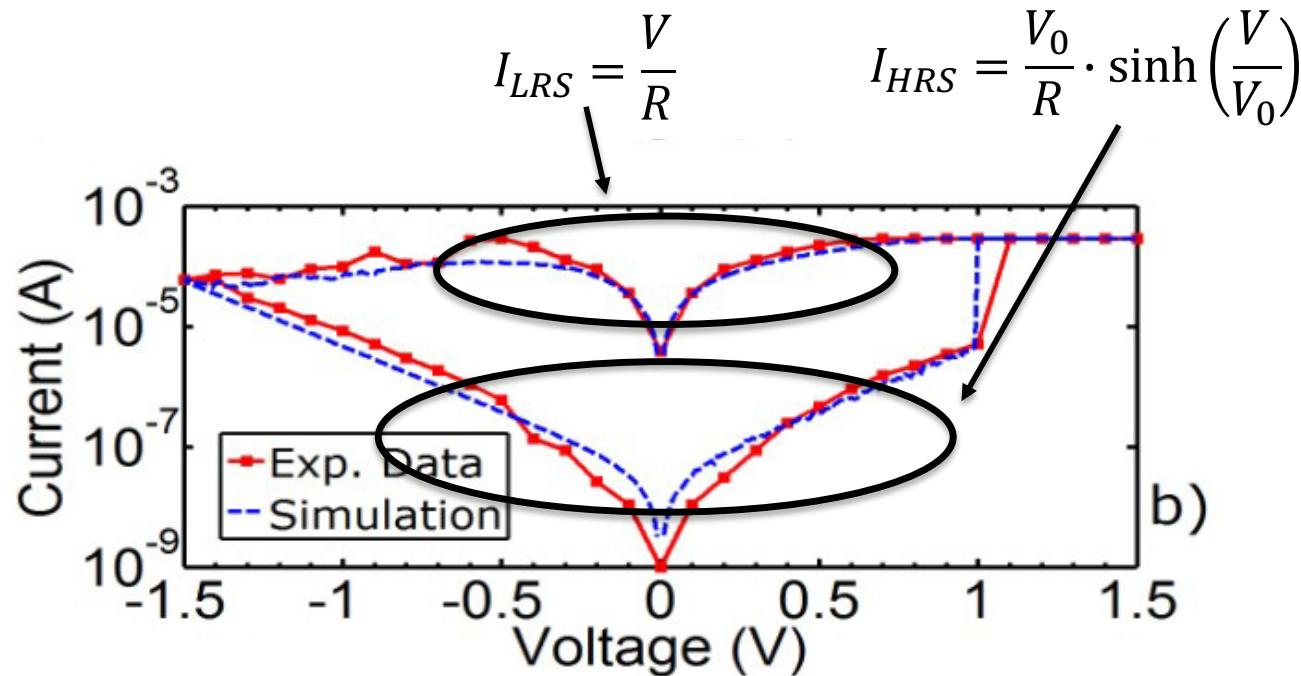
$$R(x, T) = R_{LRS} \left(\frac{t_{ox} - x}{t_{ox}} + \left(e^{\frac{x}{k}} - 1 \right) \cdot e^{\frac{E_R}{k_B T}} \right) \quad R_{LRS} = \frac{\rho_{CF} \cdot t_{ox}}{S_{CF}}$$

General representation of R valid in both LRS and HRS



Charge Transport

- Charge transport is modeled starting from the R description:
 - Full CF in LRS (Ohmic transport)
 - Ohm's law
 - Ruptured CF in HRS \rightarrow barrier (Trap-Assisted Tunneling conduction)
 - Non-linear charge transport accounted for by using a compact formula
 - V_0 extracted from I-V measurement in HRS and further verified by physics-based simulations



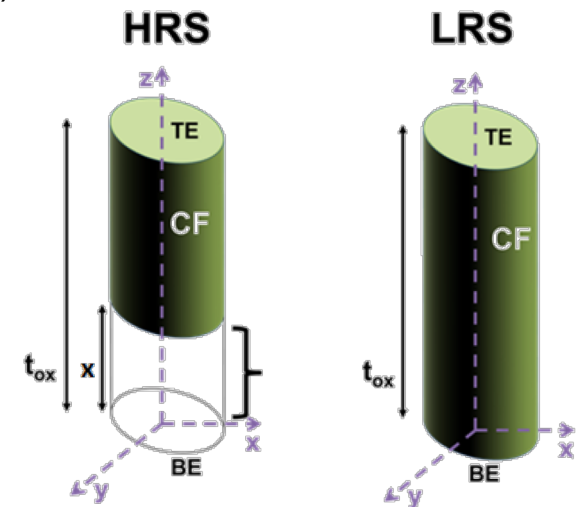
Switching Dynamics

- Switching dynamics is fully encoded in a set of coupled differential equations linking the barrier thickness to the applied voltage (V) and to the internal temperature (T):
 - Reset and Set ops. associated with the barrier growth and collapse
 - Field-driven oxygen ions drift/diffusion and recombination (reset) – parameters E_D , g_0 , a , b
 - Field-accelerated thermochemical Hf-O bond breakage (set) – parameters E_G , f
 - Thermal dynamic effects included
 - Localized power dissipation as a result of charge transport (C_p)
 - Includes a term to model heat exchange between the CF/barrier and its surroundings (k_T)
 - Includes the effect of different ambient temperature (T_0)

$$\frac{dT}{dt} = C_p^{-1} [V \cdot I - k_T (T - T_0)]$$

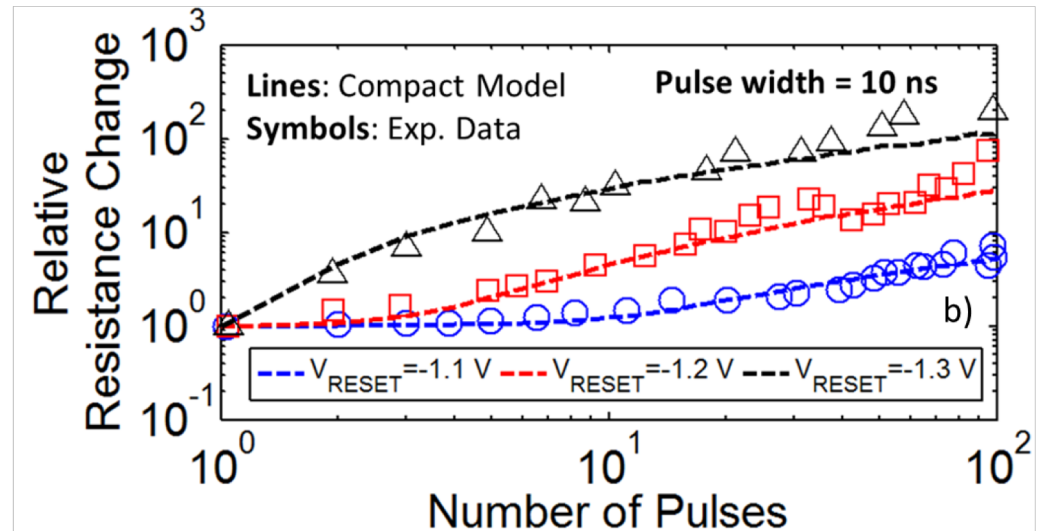
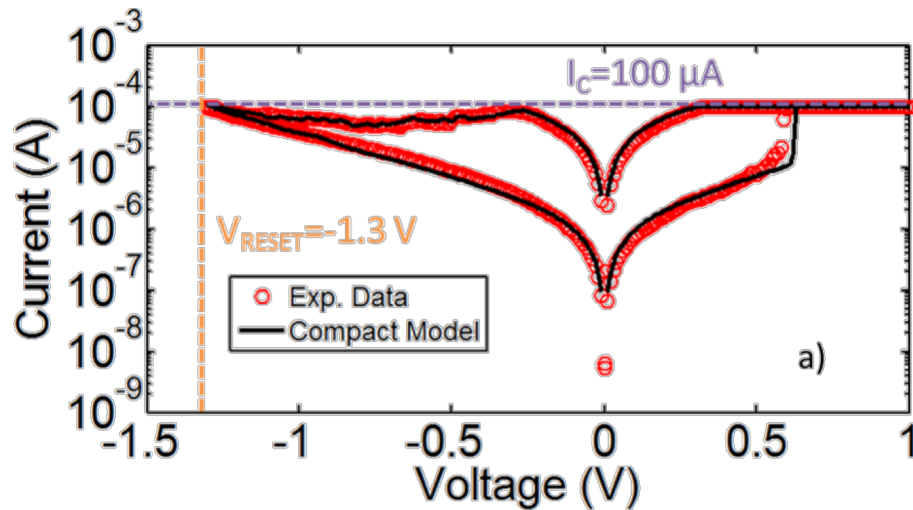
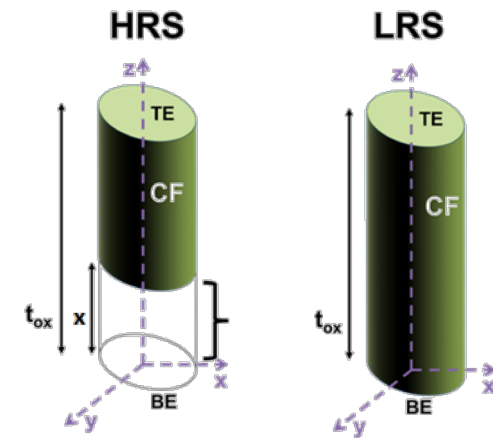
$$\frac{dx}{dt} = c_0 e^{\left(\frac{E_D - (g_0 - ax^b) \frac{V}{t_{ox}}}{k_B T} \right)} \quad (\text{reset})$$

$$\frac{dx}{dt} = -xc_0 e^{\left(\frac{E_G - f \frac{V}{x}}{k_B T} \right)} \quad (\text{set})$$



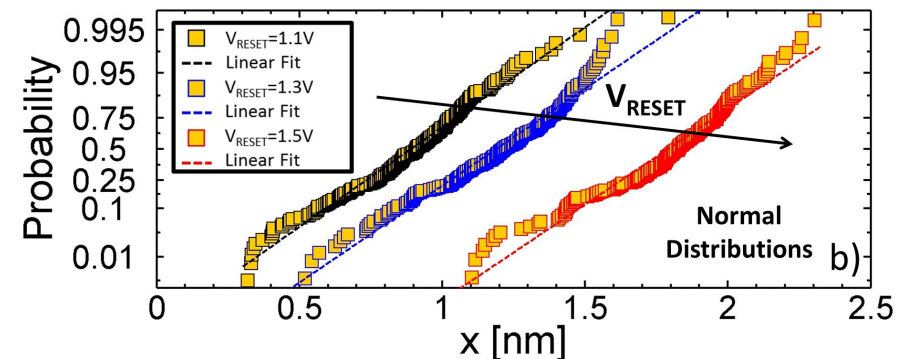
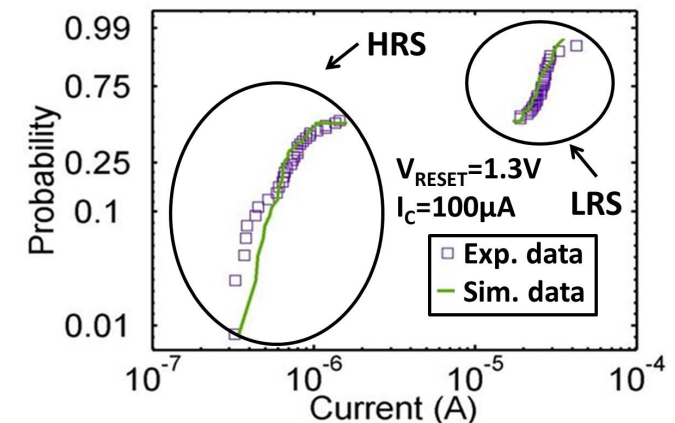
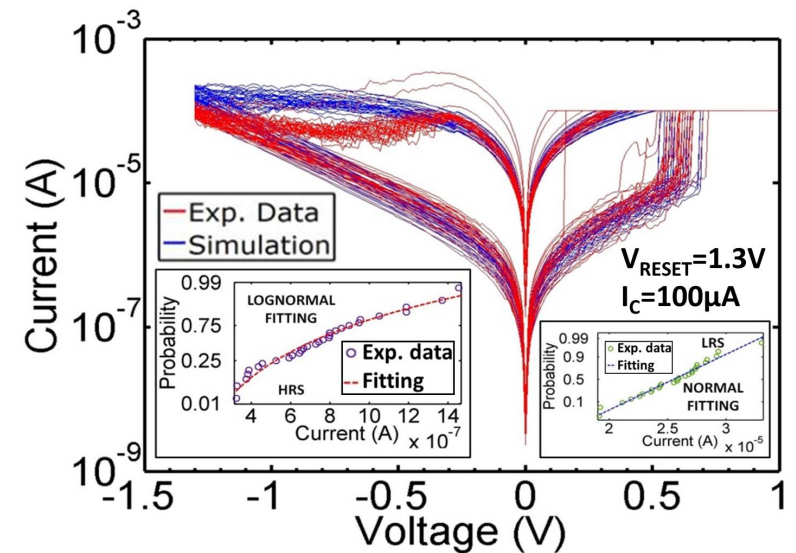
Results

- Model calibrated on exp. data from a TiN/Ti/HfO₂/TiN device
 - DC (quasi-static ramped voltage switching)
 - AC (ns pulsed switching)
- DC data
 - $I_C = 100 \mu\text{A}$, $V_{\text{RESET}} = -1.3 \text{ V}$
- AC data
 - Pulsed reset op.
 - $V_{\text{RESET}} = -1.1 \text{ V} / -1.2 \text{ V} / -1.3 \text{ V}$
 - Pulse width = 10 ns



Variability

- Experimental cycling variability features:
 - Normal R distribution in LRS
 - Log-normal R distribution in HRS (normal distribution of x in HRS)
- Modeled by using two Gaussian variability sources
 - S randomly varied from normal distribution at each SET event
 - x randomly varied (normal distribution) during each RESET event
 - Compact model predicts μ , while σ does not depend on op. conditions and can be easily extracted from variability data and included in the model for variability-aware sim.

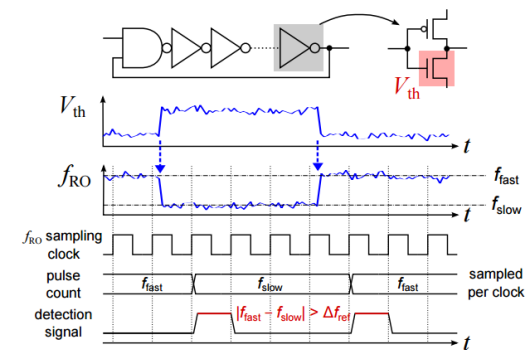
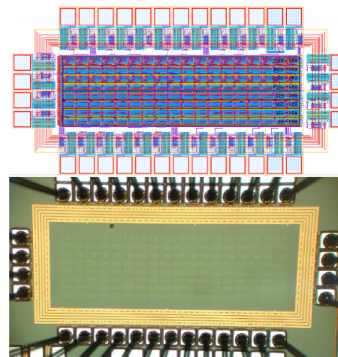
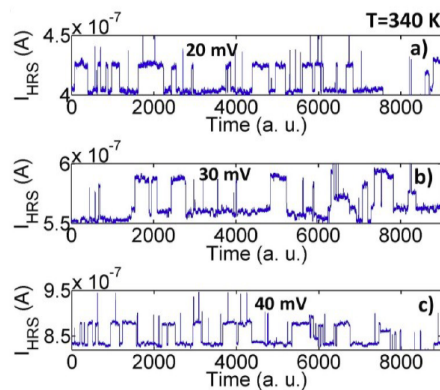
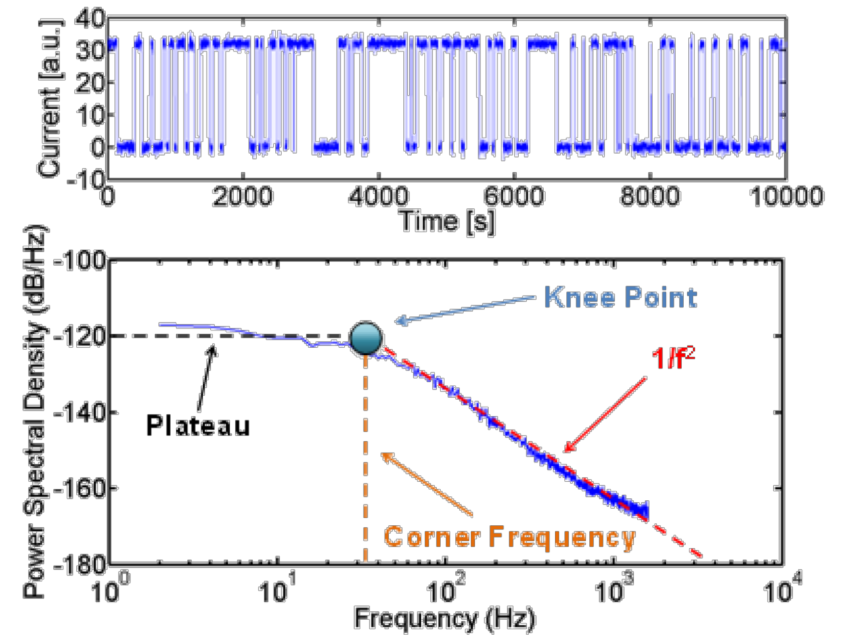


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Random Telegraph Noise

- The dominant noise in RRAM
- **Trouble** or **Resource**?
 - Read errors
 - Reduced effective memory window
 - Synaptic weight random fluctuations
 - Reduced hamming distance in PUFs
 - Reduced effective randomness in RNGs
 - RTN-based RNGs
 - RTN-based PUFs
 - Entropy Source
 - Exploratory tool



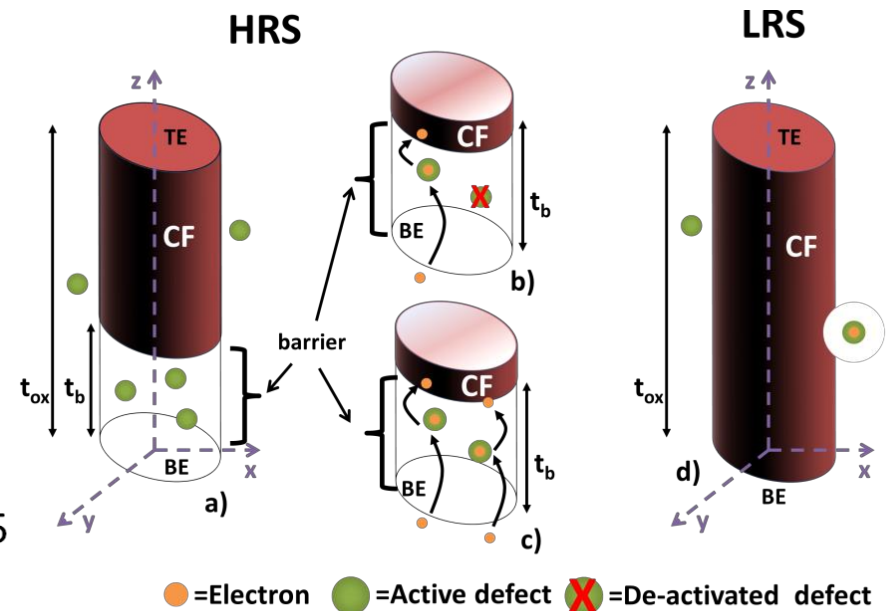
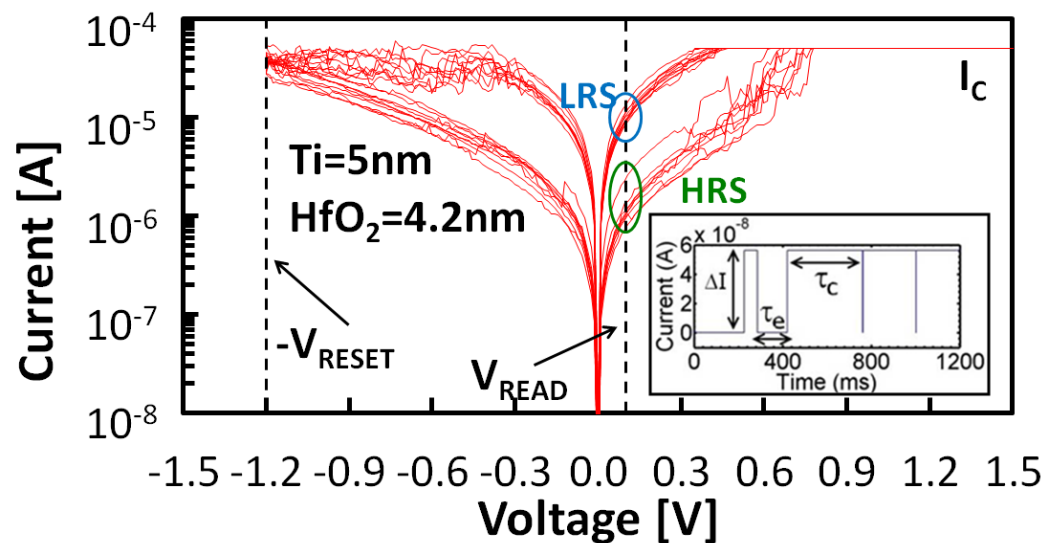
F. M. Puglisi et al. - *IEEE IRPS 2015*

T. Figliolia et al. - *IEEE ISCAS 2016*

M. Yoshinaga et al. - *IEEE ISCAS 2016*

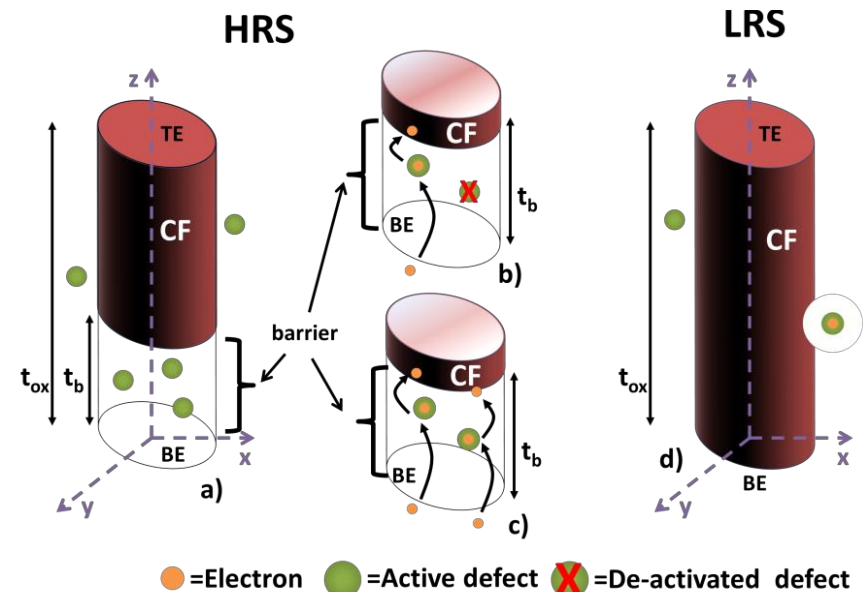
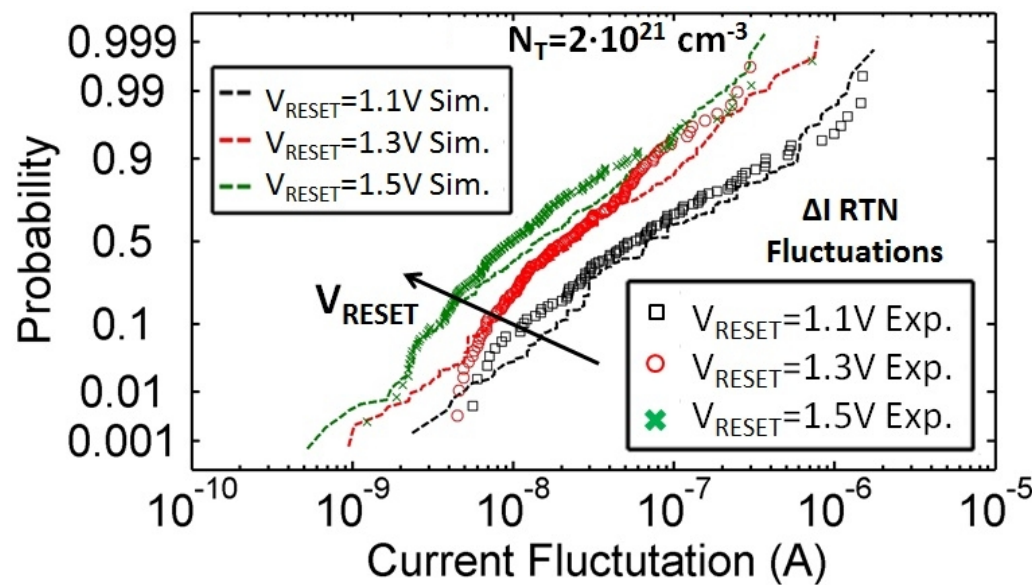
RTN in RRAM: Physics

- The physical picture of RTN in RRAM
 - Due to defects (charge trapping and de-trapping)
 - Can always be seen as an alteration of charge transport
 - Dependent on the resistive state (charge transport is different in the two states!)
- We perform careful RTN analysis in both LRS and HRS, across many switching cycles and on many devices in different conditions (V_{RESET} , I_C , T)



RTN in HRS: Physics

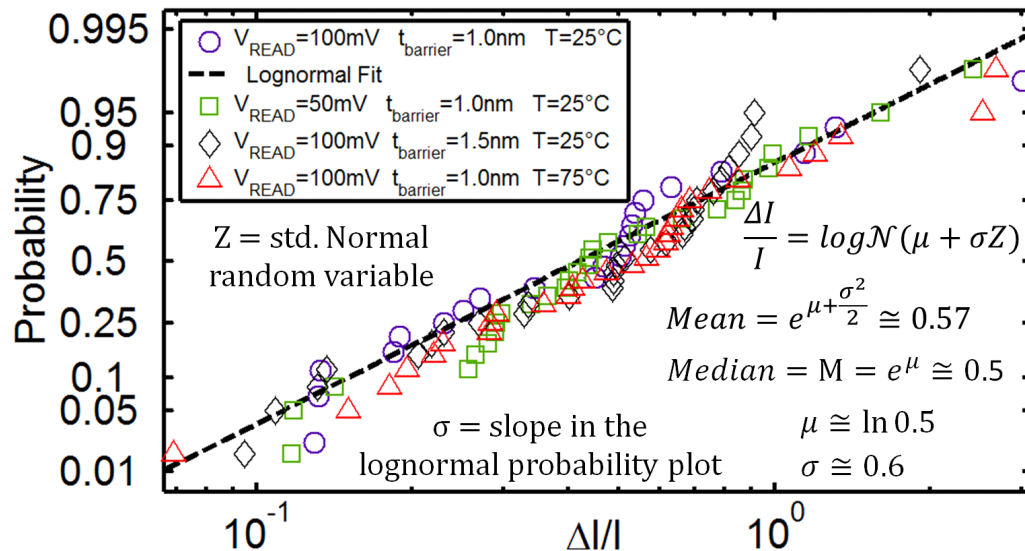
- The physical picture of RTN in RRAM in HRS
 - HRS charge transport is supported by TAT at V_o^+ defects
 - Charge trapping at additional defects (interstitial oxygen) perturbs the local potential drastically affecting TAT transport at V_o^+ defects nearby
- Comparison of exp. data and physics-based simulations including V_o^+ and interstitial oxygen defects confirms the picture.



RTN in HRS: Compact Model

- RTN amplitude (ΔI or equivalently ΔR) statistics in HRS:
 - Charge transport limited by the barrier (TAT at V_o^+ defects)
 - RTN given by V_o^+ defects “activation/de-activation” due to e^- trapping/de-trapping at interstitial oxygen defects close to V_o^+ defects
 - CF-size, barrier-size, voltage, temperature independent
 - Confirmed by physics-based kinetic Monte-Carlo simulations
- Compact formulation of amplitude statistics in HRS

$$M\left(\frac{\Delta R}{R_{HRS}}\right) \cong \frac{1}{2}; \sigma\left(\frac{\Delta R}{R_{HRS}}\right) \cong 0.6$$



Capture and emission times at oxygen interstitials calculated with compact formulae (TAT formalism).

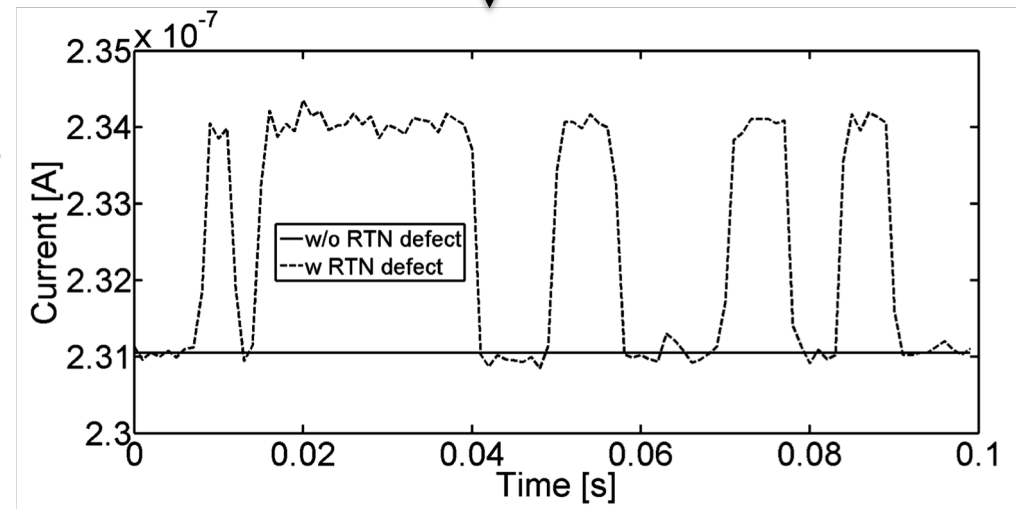
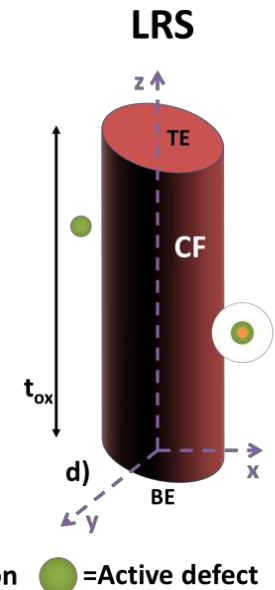
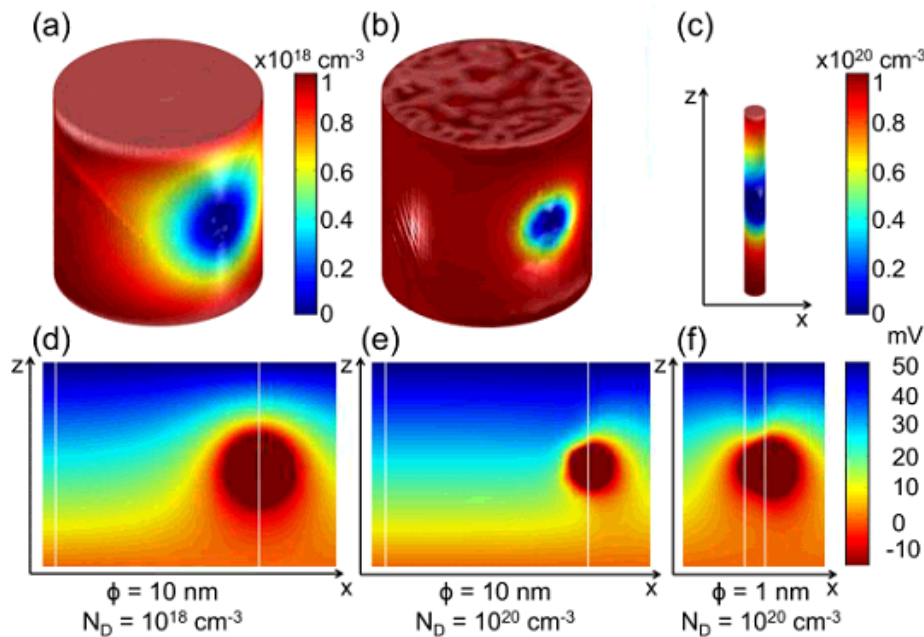
Include dependence on temperature, voltage, and defect position and typology.

$$\tau_c \propto c_0 e^{\left(\frac{x_d}{\lambda_c}\right)} e^{\left(\frac{E_c(V)}{kT}\right)}$$

$$\tau_e \propto c_0 e^{\left(\frac{t-x_d}{\lambda_e}\right)} e^{\left(\frac{E_e}{kT}\right)}$$

RTN in LRS: Physics

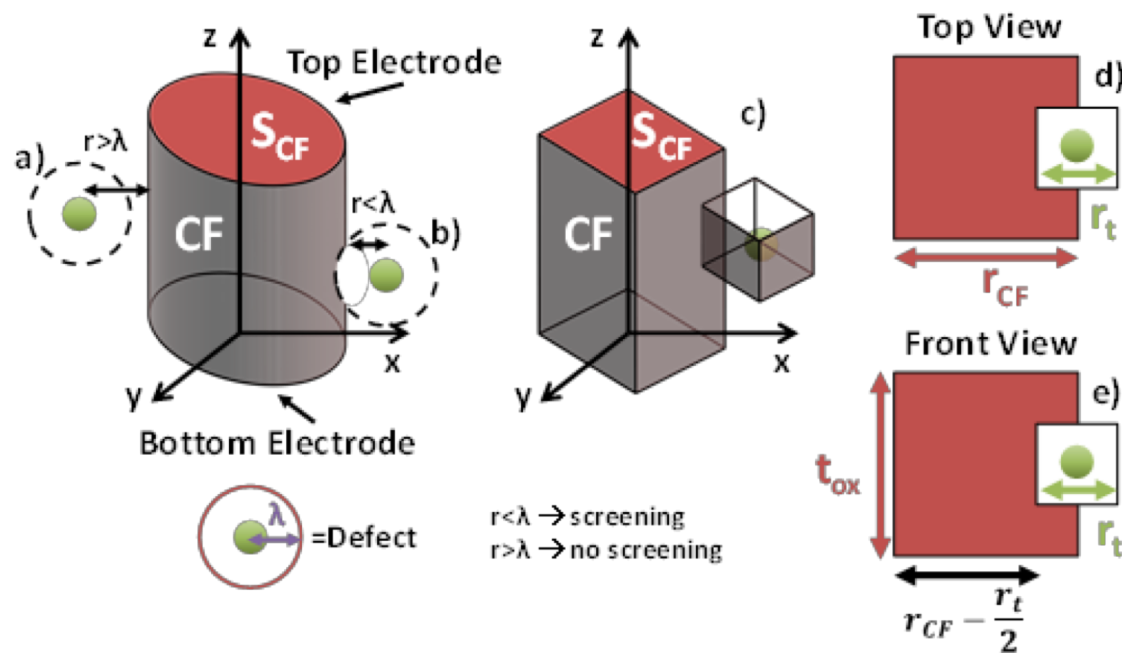
- The physical picture of RTN in RRAM in LRS
 - Charge transport = Delocalized electron flow along the CF
 - CF made of tightly packed V_o^+ defects, therefore their individual activation/deactivation produces no sensible effect
 - RTN due to **screening from trapped charge at defects around the CF**
 - Can be both V_o^+ and O interstitials
 - CF-size dependence (reported in the literature as well)**



S. Ambrogio et al. - *IEEE TED* 2014, vol. 61, no. 8, pp. 2920

RTN in LRS: Compact Model

- RTN amplitude (ΔI or equivalently ΔR) statistics in LRS:
 - Charge transport limited by the CF
 - Screening effect on the CF (CF-size dependent) modeled with geometrical simplification to derive a simple formula
- Compact formulation of amplitude statistics in LRS



$$M\left(\frac{\Delta R}{R_{LRS}}\right) = \frac{r_t^3}{2t_{ox} \cdot S_{CF}}$$

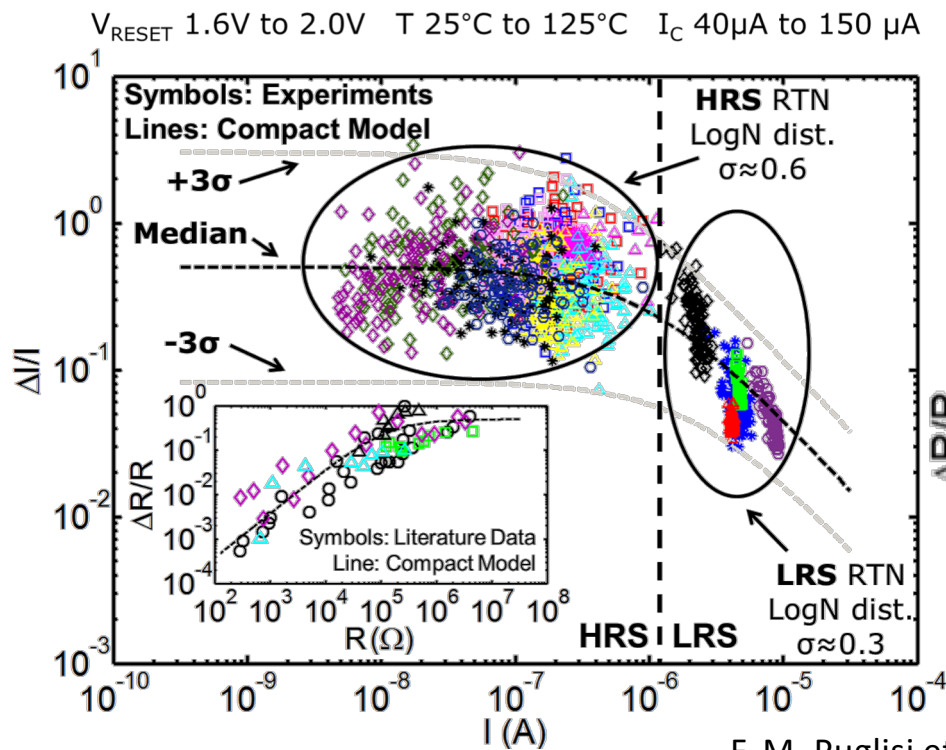
$$\sigma\left(\frac{\Delta R}{R_{LRS}}\right) \cong 0.3$$

Capture and emission times at defects surrounding the CF calculated with the same formulae used for the HRS case.

Include dependence on temperature, voltage, and defect position and typology.

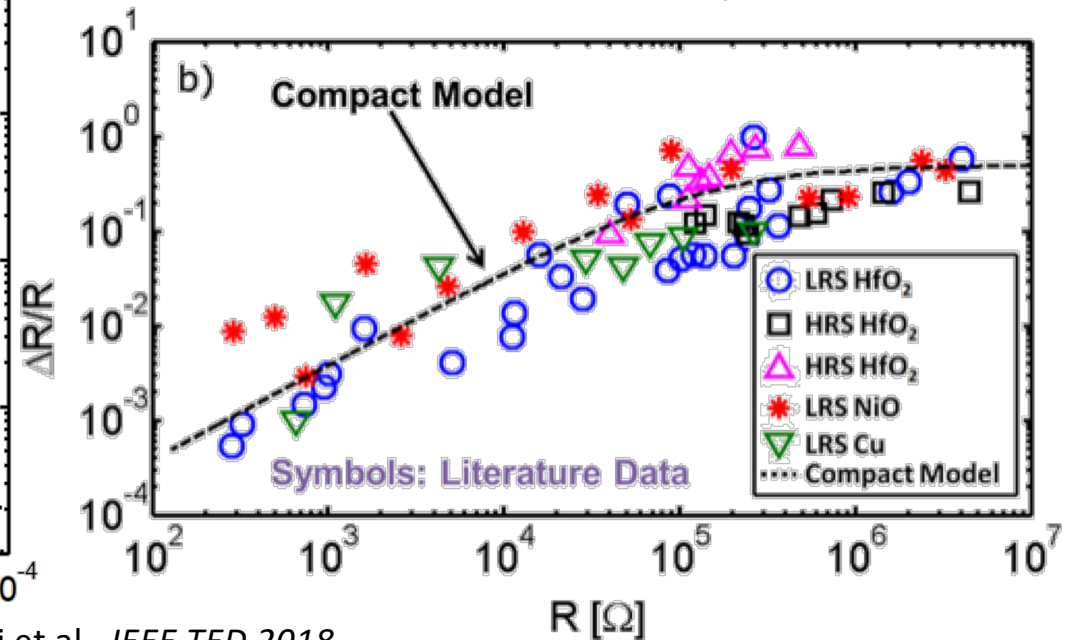
RTN in RRAM: Complete Compact Model

- Complete formulation of RTN amplitude statistics
 - Compact formula valid in both states
 - RTN amplitude statistics correctly reproduced in many different operating conditions (**also with $\pm 3\sigma$ bounds!**)
 - Confirmed by validation against a significantly large dataset and data from the literature (also different materials!)



F. M. Puglisi et al., *IEEE TED* 2018

$$M\left(\frac{\Delta I}{I}\right) = M\left(\frac{\Delta R}{R}\right) \cong \left[\frac{2t_{ox} \cdot S_{CF}}{r_t^3} + 2\right]^{-1}$$

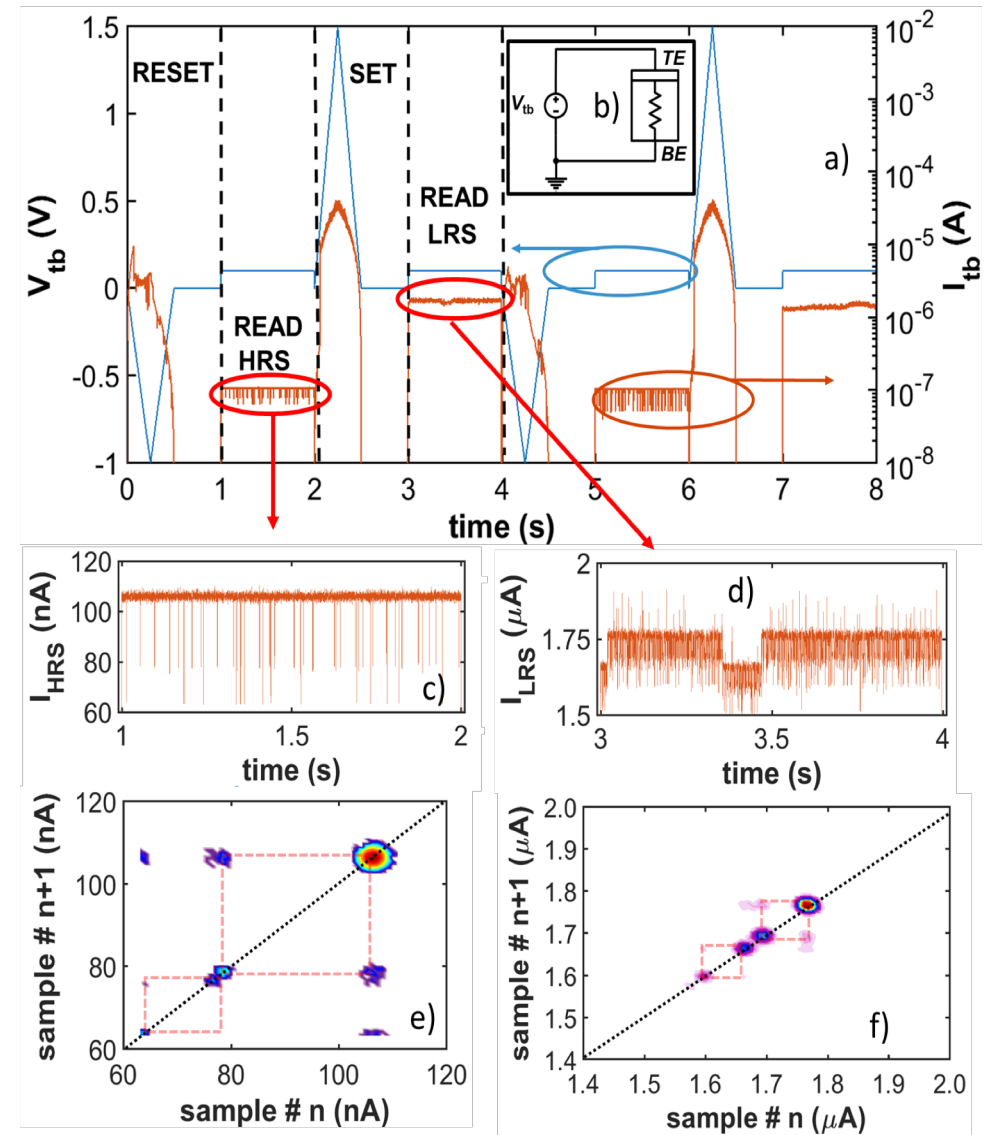


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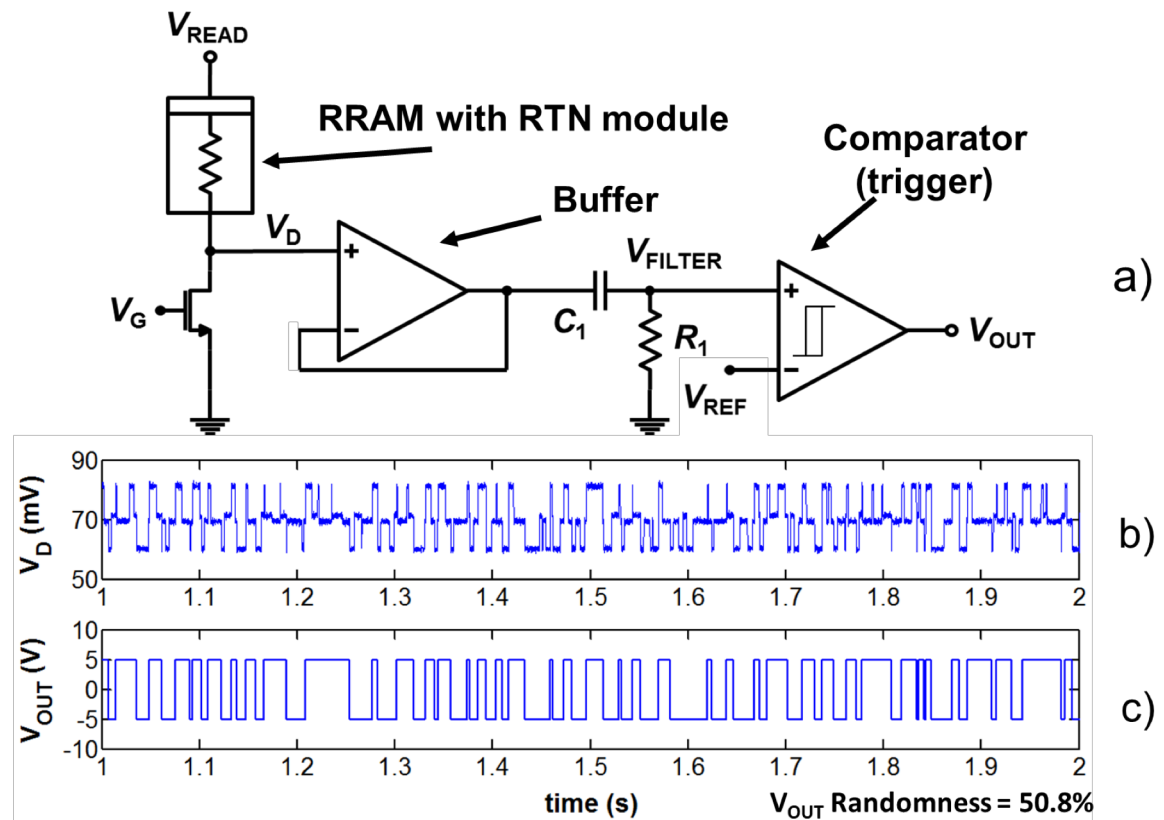
Compact Model Applications

- RRAM Compact Model enables advanced circuit simulations for many emerging applications.
- Here we show two examples
 - Design of the building block of a Truly-Random Number Generator circuit exploiting the RTN randomness as an entropy source
 - Design of a logic-in-memory circuit architecture implementing a 1-bit full-adder accounting for the intrinsic variability of the resistive states and the logic state degradation.



True-RNG Circuit based on RTN

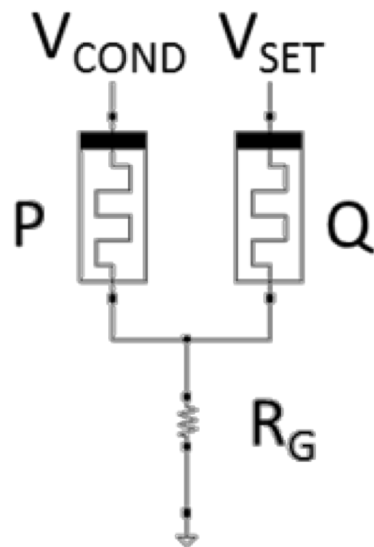
- Using the possibility to simulate RTN transient to design a True-RNG circuit:
 - RRAM device in HRS ($x = 1$ nm).
 - Series transistor.
 - Buffer with a high-pass filter.
 - Comparator.
 - Successful reproduction of the RTN pattern at the output (i.e., random bit stream) also in case of multilevel RTN



F. M. Puglisi et al., *IEEE TED* 2018

Logic-in-Memory Circuits

- LiM associates logic states with RESISTIVE states, not voltage!
 - A RRAM cell (P) holds 1 bit (**memory**) but the same bit also represent a logic value that can be processed in place (**logic**)!
- A very promising LiM scheme to be realized using RRAMs.
- Two ops. (IMPLY and FALSE) that form a complete logic group:
 - All possible logic gates can be built out of IMPLY and FALSE ops.
 - FALSE (i.e., always yields logic 0). Easy to realize with RESET.
 - IMPLY (a two-input operation with the following truth table).



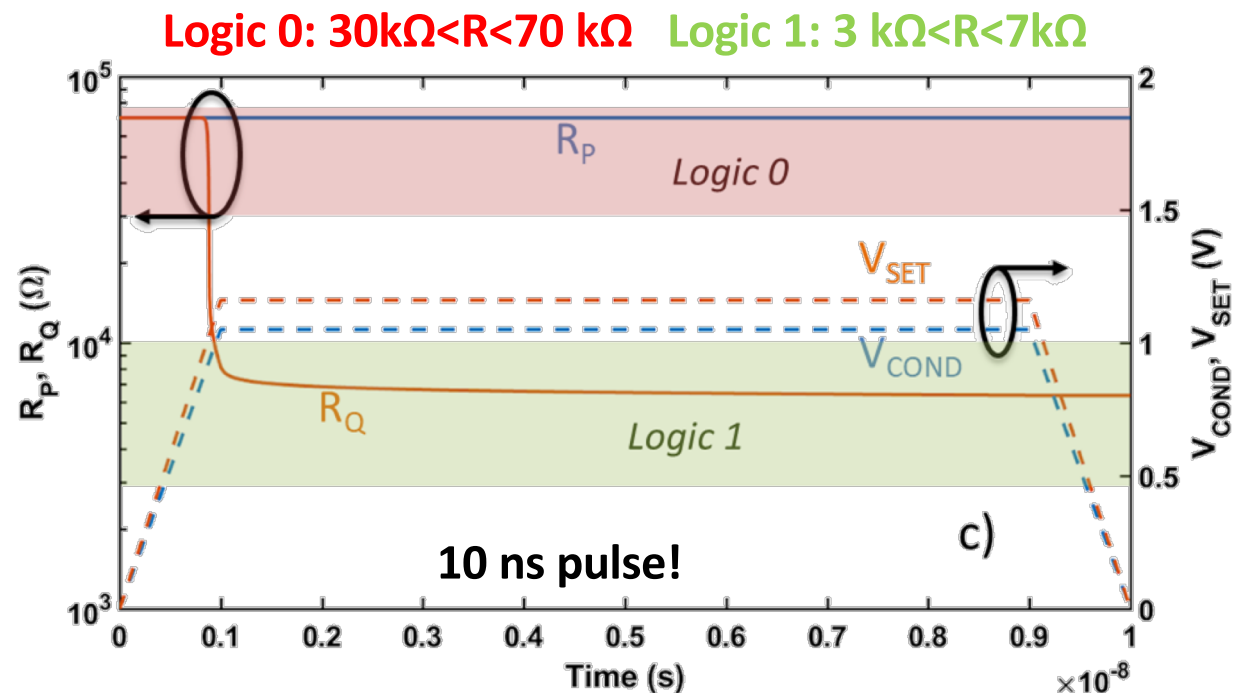
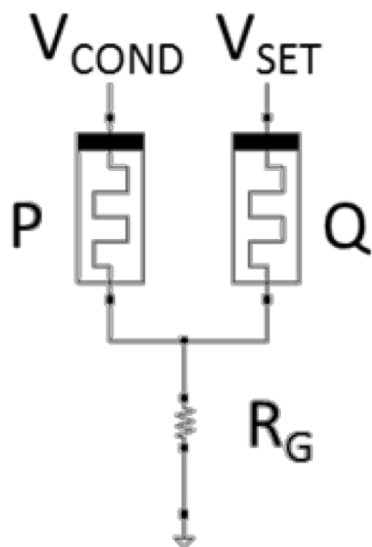
P must not switch!

V_{COND} must be **small** enough!

P	Q	Q'
0	0	1
0	1	1
1	0	0
1	1	1

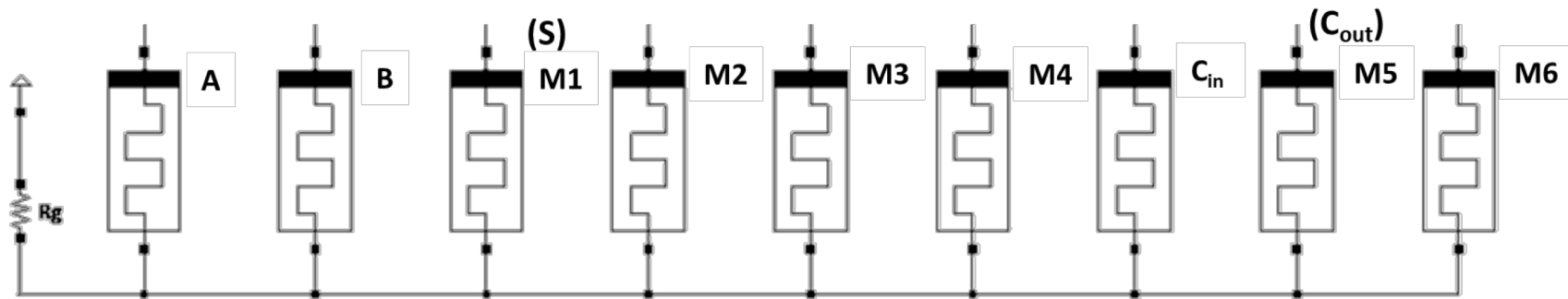
Logic-in-Memory Circuits

- IMPLY performed by applying appropriate voltages to the top electrodes of the two RRAM devices (i.e., V_{COND} and V_{SET}).
- FALSE: reset operation on the individual RRAM device.
- The V_{SET} (= 1.16 V), V_{COND} (= 1.05 V), and R_G (= 4 k Ω) values were derived by using a custom optimization algorithm.
- Logic values chosen given the optimal V_{SET} and V_{COND} together with device variability features in both resistive states.



Logic-in-Memory 1-bit Full-Adder

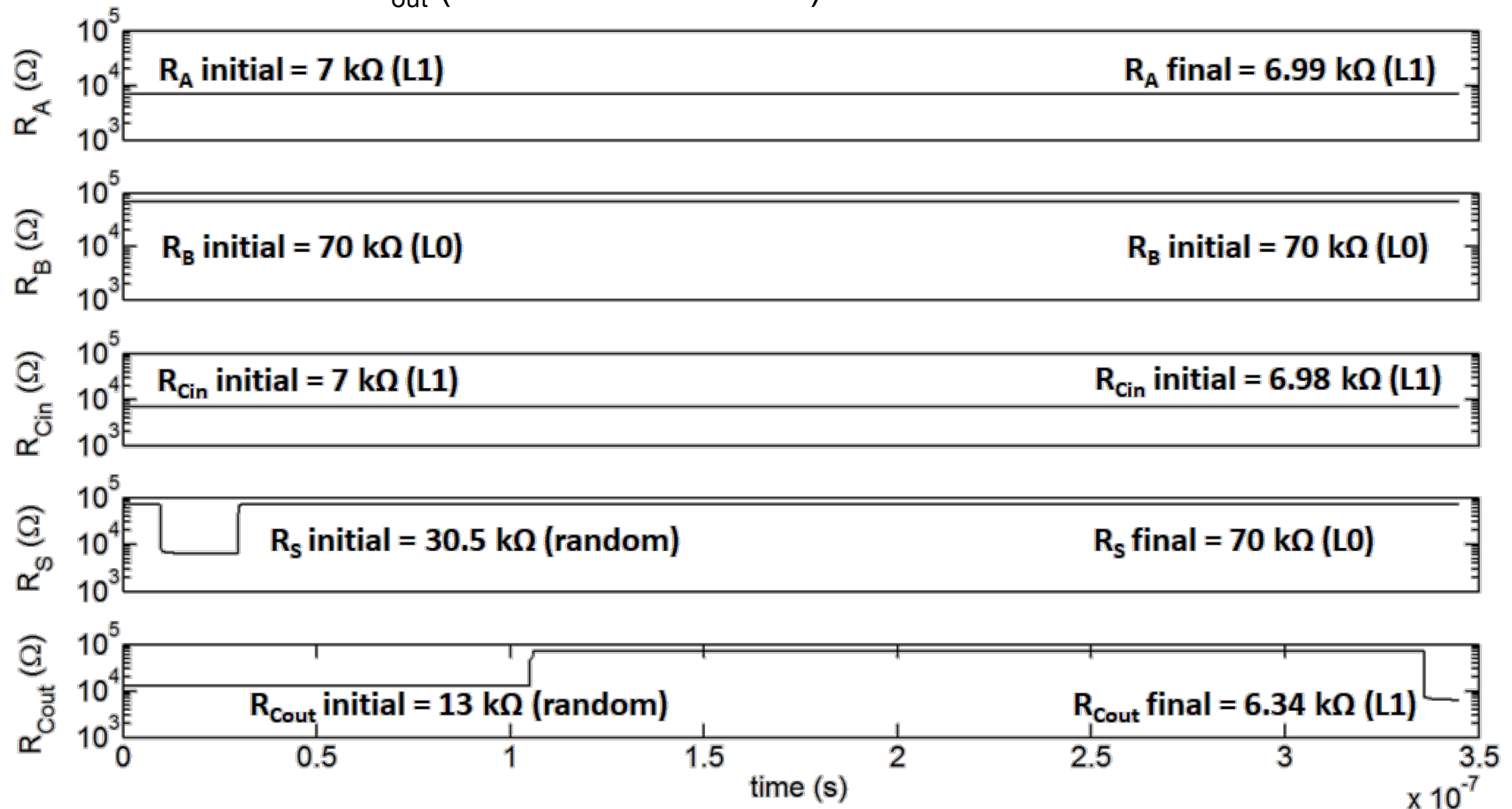
- Proposed implementation of a LiM 1-bit Full-Adder
 - 9 devices and 43 steps (17 FALSE).
 - Input devices logic states is preserved.
 - Initial state of the additional devices is unimportant.



A	0	0	1	1	0	0	1	1
B	0	1	0	1	0	1	0	1
C_{in}	0	0	0	0	1	1	1	1
S	0	1	1	0	1	0	0	1
C_{out}	0	0	0	1	0	1	1	1

Logic-in-Memory 1-bit Full-Adder

- Example: $A=1$ $B=0$ $C_{in}=1$ $S=0$ $C_{out}=1$.
 - S and C_{out} (set to random values).



Logic-in-Memory 1-bit Full-Adder

- Energy consumption breakdown
 - FALSE op. (-3.5 V / 5 ns) is the most energy demanding.
 - IMPLY performed with 10 ns pulses (optimized V_{COND} and V_{SET}).
 - Total energy consumption is 6.4 nJ.

Device	IMPLY Energy	FALSE Energy	Total Energy
A	2.659 pJ	0	2.659 pJ
B	254.5 fJ	0	254.5 fJ
C_{in}	254.5 fJ	0	254.5 fJ
M1 (S)	4.201 pJ	3 x 376 pJ	1.128 nJ
M2	7.778 pJ	3 x 376 pJ	1.128 nJ
M3	4.345 pJ	3 x 376 pJ	1.128 nJ
M4	9.191 pJ	3 x 376 pJ	1.128 nJ
M5 (C_{out})	6.23 pJ	3 x 376 pJ	1.128 nJ
M6	635 fJ	2 x 376 pJ	0.752 nJ
Full Adder			6.4 nJ

Logic-in-Memory 1-bit Full-Adder

- Energy consumption optimization and benchmarking
 - FALSE conditions are heavily impacting on energy and time.

FALSE Pulse Time / Voltage	FALSE Energy	Total Energy	Total Exec. Time
5 ns / - 3.5 V	376 pJ	6.4 nJ	345 ns
250 ns / - 2.5 V	4.02 nJ	68.04 nJ	4782 ns

- LiM can compete with CMOS if R/W contributions are considered.

	This work	State-of-the-art	CMOS
Execution Time	345 ns	108 μ s Exp. [9] >3.77 μ s Sim. [4]	\approx ps [9] \approx 0.5 ms*
Energy Cons.	6.4 nJ	19.5 nJ Exp. [9] Unavail. in Sim.	\approx fJ [9] \approx 50 μ J*
Footprint	$\leq 4F^2$	$\leq 4F^2$	$6F^2$
# of Steps	43	27 Exp. [9] 29 Sim. [4]	1
# of Devices	9	8 Exp. [9] 6 Sim. [4]	36 FETs

*includes the energy and time needed to read 3 bits (A, B, C_{in}) and write back two bits (S, C_{out}) to an external flash memory.

Exp. in [9] use relatively long pulses ($\approx \mu$ s). Using similar pulse width we get comparable energy consumption (67 nJ vs. 19.5 nJ). However devices and R_G are slightly different.

Excellent dependability of the proposed approach!

[4] S. Kvatinsky et al., IEEE Trans. VLSI Systems, vol. 22, no. 10, pp. 2054-2066, Oct. 2014.

[9] L. Cheng et al., 2017 J. Phys. D: Appl. Phys. 50 505102.

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Conclusions

- Proposed compact model of RRAM devices
 - Completely physics-based, works in all regime of operation (also ns-pulsed AC regime)
 - Easily tweakable and adaptable to a variety of material systems
 - Includes thermal effects, variability, and RTN (also multi-level)
 - Validated against a large experimental dataset, literature data, and refined physics-based simulations.
 - Written in Verilog-A for advanced circuit simulations for many applications: memory, neuro, PUFs, RNGs, more...
- The model can be successfully used to design innovative circuits and reliably evaluate their performance (e.g., energy consumption)
 - T-RNG circuits for security, authentication, cryptography
 - LiM 1-bit Full Adder architecture with excellent energy/time performances, in-line with experimental data

Thanks to...

- Luca Larcher's group @ DISMI – UniMORE (Italy)
- Andrea Padovani, Luca Vandelli @ MDLSoft Inc. (U.S.A.)
- Gennadi Bersuker, Dmitry Veksler (at the time of research @ Sematech (U.S.A.))
- Key Leong Pey, Nagarajan Raghavan @ SUTD (Singapore)
- Christian Wenger @ IHP Microelectronics GmbH (Germany)
- Many other students and colleagues

**Thank you for your
attention**

...Questions?