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ÉCOLE NATIONALE SUPÉRIEURE D'INGÉNIEURS DE CAEN
& CENTRE DE RECHERCHE

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New Verilog A Model Compiler for SPICE 3F5

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1− Introduction

=> Why Verilog A ?? (Main Goals) :

=> Rigth derivatives (Jacobian for Newton−Raphson...)

=> be sure of Right Matrix loading ...

=> simplify , decrease a lot the time, to implement a new model into SPICE

=> avoid the polemics when convergency PB :

=> no convergency or iteration number too high

=> low convergency : TRAN : too long simulation time

Where does convergency PB come from ??

=> from the model itself ??

=> from some bad derivatives in the reference C ??

=> from the bad implement from CAD supplier ??

=> from no Right Limiting Function strategy ??

=> Why not using Mot−Adms Verilog A compiler ?? :

=> I test the last 4 versions : Aug 2004 (Verilog A compiler from Laurent LEMAITRE...)

=> but :

=> not compatible with SPICE3F5 ... (could be in the future ?? using XML ??)

=> today : Works only for DC Analysis .... (main problems for HICUM is TRAN ...)

=> do not support Verilog A Analog Function :

=> return Function :ex: "ia = func_ia(V(a),V(b),xb) ;"

=> IN OUT parameters for Analog Function

=> no return Function :ex: "func_ia(V(a),V(b),xb) ;"

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2− Features supported in this SPICE Verilog A compiler :

=> Errors , warnings (syntax && variables ...) decoding...
=> Only 1 module per Verilog A code
=> today : only the Model way
=> no Device of Model (instance)
=> no test banch ...
=> some features not yet implemented :
=> function idt()
=> V(n1,n2) <+ exp
(in fact only : I(n1,n2) <+ exp is needed in Model ...)
=> Noise Analysis ...
=> today : only available on PC LINUX

=>Verilog A Analog Functions
=> with return value
ex: "ia = func_ia(V(a),V(b),xb) ;"
=> with In−Out parameter values : "xb"
=> with no return value :
ex: "func_ia(V(a),V(b),xb) ;"
=> Device && Model parameter may be separated
=> "temp" && "area" are automatically added ...
=> "getveriloga" : loading into SPICE of compiled model
=> Spice3F5 Analysis supported :
=> OP , DC and related Analysis
=> AC , PZ and related Analysis
=> TRAN
=> RF analysis : HB,QP,CE

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3− Development phases :

using some GNU tools :

=> flex 2.5 (fast scanner generator && "lex" compatible)

=> bison 1.35 (YACC−compatible Parser Generator)

and starting from Bison examples : calc, ltcalc, mfcalc ...

3−1 decode & generate 1 line of expression & Derivatives

validate all features : + − * / = cos() afunc() ...etc

3−2 decode & generate all lines & expression & Derivatives of 1 model

=> on simple models ex : RCMOD ....etc

=> on complex model : HIC213 ....

validate all features : parameters, module ...etc

3−3 generate Matrix loading & files : for OP

validate :

=> on simple circuits ex : RCMOD ....etc

=> on complex circuits using BJT : HIC213 ....

3−4 generate Matrix loading & files : for TRAN

validate :

=> on simple circuits ex : RCMOD ....etc

=> on complex circuits using BJT : HIC213 ....

3−5 generate Matrix loading & files : for other Analysis :

AC , PZ , ... RF Analysis : HB, QP, CE

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4 − 1 : example of : Simple R C model

```
module modrc(a,b,nx,ny,nz) ;
  inout a,b ;
  electrical  a,b,ci,nx,ny,nz;
  real rx,iac,qcb,vab,vac,vcb ;

  device parameter real r = 1k ;
  device parameter real c = 1p ;
  model  parameter real vc1 = 0.0 ;
  model  parameter real vc2 = 0.0 ;

analog begin
  vab = V(a,b);
  vac = V(a,ci);
  vcb = V(ci,b);
  rx  = r * (1.0 + vc1*vab + vc2*(vab*vab)) ;
  iac = vac / rx ;
  qcb = c * vcb ;
  I(a,ci) <+ iac;
  I(ci,b) <+ ddt(qcb) ;
  I(ci) <+ V(ci)/1.0e12;
  I(nx) <+ V(nx)/1.0e12;
  I(ny) <+ V(ny)/1.0e12;
  I(nz) <+ V(nz)/1.0e12;
end
endmodule
```

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4 − 1 : example of : Simple R C model

```
int
MODRCevaluate (a, b, ci, nx, ny, nz, cktin, herein, hboff)
double     a, b, ci, nx, ny, nz ;
CKTcircuit     *cktin;
MODRCinstance  *herein;
int   hboff;
{
   .............          Values & Derivatives setting
   vab.val=a−b ;
   vab.D_a=1.0 ;
   vab.D_b=−1.0 ;

   ........................  Expressions  & Derivatives setting
    rx.D_a=r*(vc1*(vab.D_a)+vc2*(vab.val*(vab.D_a)+vab.val*(vab.D_a))) ;
    rx.D_b=r*(vc1*(vab.D_b)+vc2*(vab.val*(vab.D_b)+vab.val*(vab.D_b))) ;
    rx.val=r*(1.0+vc1*vab.val+vc2*(vab.val*vab.val)) ;

    ..................................  Matrix   loading   I_a_ci
     *(here−>MODRCINaAptr)  += I_a_ci.D_a ;
     *(here−>MODRCINaBptr)  += I_a_ci.D_b ;

    ..................................  RHS   loading   I_a_ci
     _ieq  = I_a_ci.val ;
     _ieq −= I_a_ci.D_a*a ;
     _ieq −= I_a_ci.D_b*b ;
    ..........................................................
    (ckt−>CKTrhs[NUM_Na]) −= _ieq ;
    (ckt−>CKTrhs[NUM_Nci]) += _ieq ;
```

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4 − 2 : example of Bipolar : HICUM models

HIC203 : HICUM level 0 (5 external nodes & Self Heating)

HIC213 : HICUM level 2.1 (5 external nodes & Self Heating)

=> numerical values results very close of previous HICUM212
(classical manual implement from referenceFortran code)

=> better convergency behaviour when OP && TRAN
(can be seen only for complex circuits)

=> still needs some Model specific limiting functions
(can be seen only for complex circuits)

notes : complex circuits means :
=> with a high number of BJT transistors
=> with high GAIN
=> with feedback ...

ex : an BJT ECL ring oscilator of 41 stages ...

4 − 3 : MOS : examples close of EKV 2.6 models :

EKV26VA : Verilog A close of ekv26_SDext_tiburon.va
EKV26VASH : idem EKV26VA & Self Heating

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5− Remaining Works ...

=> Noise Analysis ...

=> remaining features : "idt ()" , "V(n1,n2) <+ exp" ....

=> How to introduce the Limiting functions needed when Strongly no linear model ??

=> Spice Verilog A Compiler for HP workstation under HPUX

6− Other Developments :

=> a lot of new features & improvement for Spice3F5

- Spice driven from schematic ...
- Subckt Parameters
- Process Block
- New Spice RF :
  - S parameter Analysis & port + nport
  - New Harmonic Balance Analysis : HB,QB, CE

=> ATELECAD kit

- => schematic capture
- => logic simulation
- => Layout : MAGIC 6 :
  - => extended version for Bipolar : DRC etc ...
  - => new feature : component generators ....