

Compact Model Verilog-A Standardization

Panel Discussion

MOS-AK Washington

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Verilog-A Domination ^{Nearly} Complete

CMC Standard Models	Original Language	Current	Comments
BSIM3	C (Spice3)		Replaced by BSIM4
BSIM4	C (Spice3)		To be replaced by BSIM6
BSIM6	Verilog-A	Verilog-A	Pending CMC acceptance (12/2011?)
BSIMSOI	C (Spice3)	Verilog-A	as of 4.4.0 (12/2010)
PSP	Verilog-A	Verilog-A	
HiSIM	C (Spice3)	C and VA	
HiSIM-HV	C (Spice3)	C and VA	
HICUM	FORTRAN	Verilog-A	as of 2.11 (2004?)
Mextram	C (SiMKit)	Verilog-A	as of 504.6 (4/2005)
MOSVAR	Verilog-A	Verilog-A	
R2_CMC, R3_CMC	Verilog-A	Verilog-A	
Diode_CMC	Verilog-A	Verilog-A	

Verilog-A Advantages

- Excellent for model development
- Automatic derivatives
 - Tedious to do by hand
- Simulator-independent
 - No need to write interface code
- Supported in all key simulators
 - Easy for industry partners to use

Simulator Support

Simulator Vendor	Support Level
Accelicon	2.3 (partially)
Agilent	LRM 2.3.1
Cadence	LRM 2.3 (partial)
Mentor Graphics	LRM 2.2
Silvaco	LRM 2.2
Synopsys	2.2/2.3

- Source: EDA Vendor Reports to CMC
- LRM 2.2 (Nov 2004) contained Compact Model Extensions
- LRM 2.3.1 was released in June 2009

What's missing

- Verilog-A Debugger
 - Lynguent has some capabilities
- Free, standard, widely-used tool
 - Nothing compares to Spice3
 - QUCS uses non-standard netlist
 - ADMS hard to use

Remaining Problems

- Verilog-A not (yet?) ideal for model distribution
- Compilers not equally capable
 - Optimization sometimes lacking
- Models don't use a consistent style
 - Hard to extract documentation