Compact Modeling of Silicon Carbide Lateral FETs for High Temperature Analog and Digital Circuits

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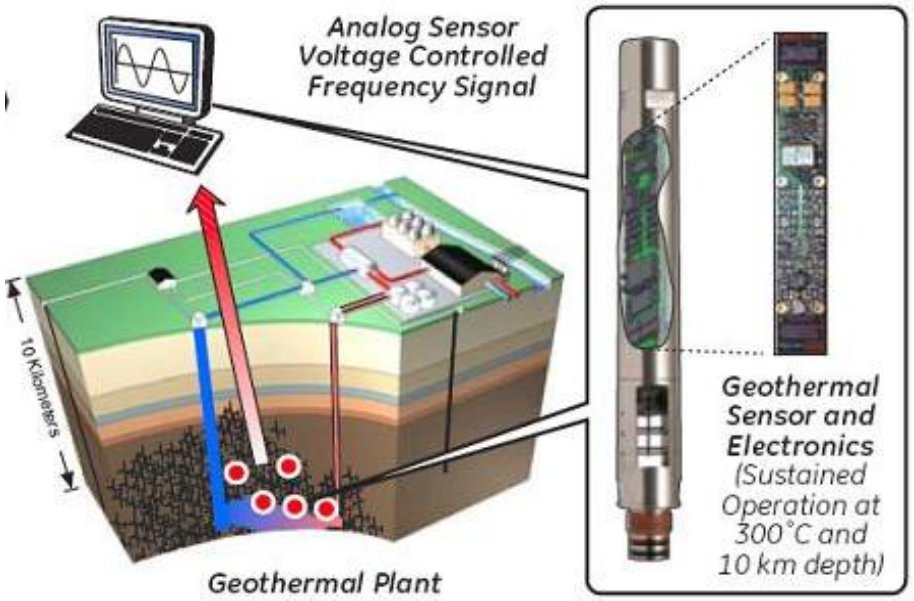
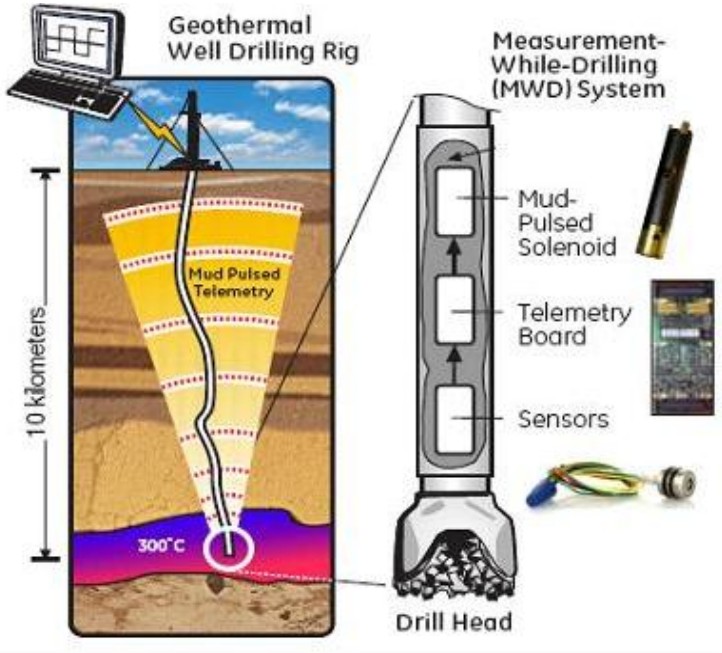
Overview





Program Objectives:

- Enable geothermal wellbore monitoring through the development of SiC based electronics and ceramic packaging capable of sustained operation at temperatures up to 300˚C and 10 km depth.
- Demonstrate the technology with a temperature sensor system

Program Objectives:

- Develop electronics for telemetry for measurement while geothermal drilling
- Demonstrate Pressure and temperature sensor systems multiplexed through a telemetry system

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Impact of Research

Project Objective

Develop electronics platform technology for operation at 300°C and demonstrate a temperature sensor system

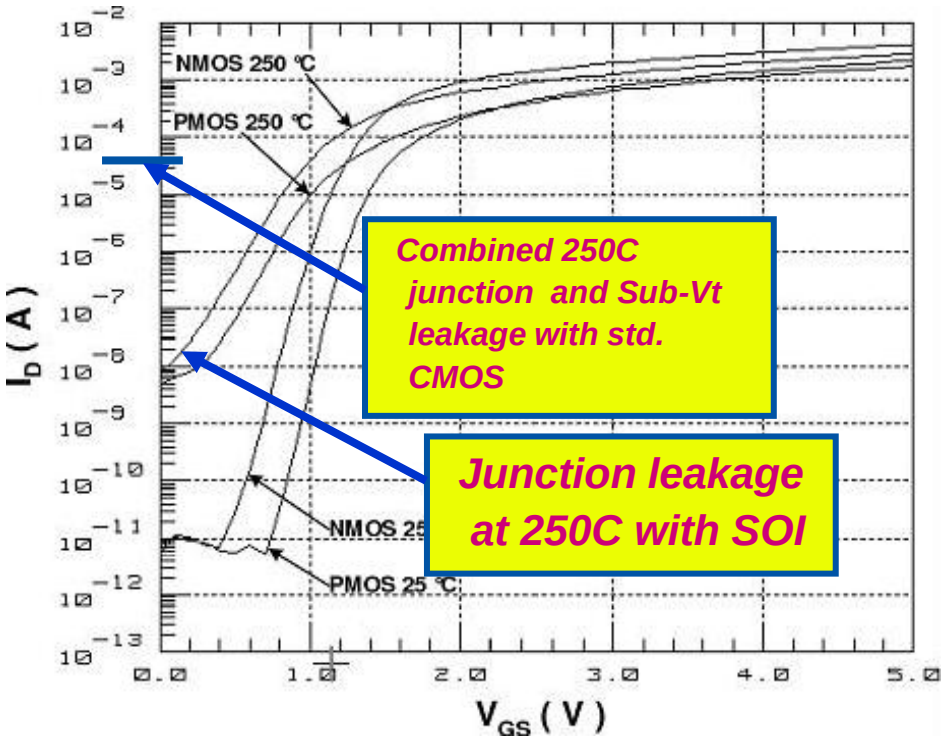
Benefits to Geothermal industry

- Enable high temperature well construction – logging tools developed using this technology can enable economic drilling
- Better reservoir characterization through long term reservoir monitoring – sensors based on this technology will be designed to operate at high temperatures for months

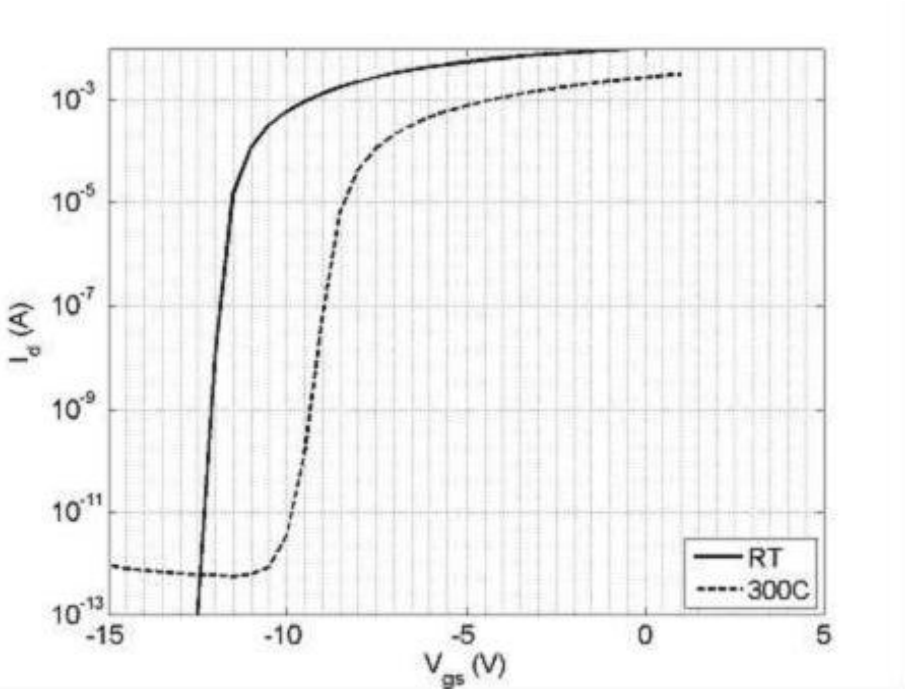
Key innovations

- Silicon carbide based analog integrated circuits used for active electronics – The integrated circuits attempted in this project will allow signal conditioning of sensor element signal at high temperature.
- Ceramic based packaging and board materials that are rated to operate at 300°C – Traditional organic based substrates or lead based packaging materials will not be used

Choice of substrate



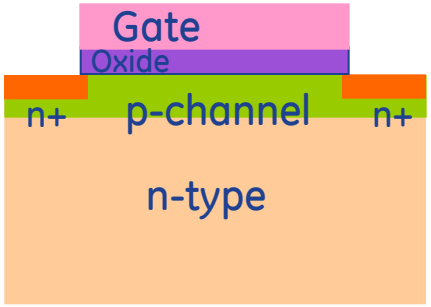
Silicon and SOI

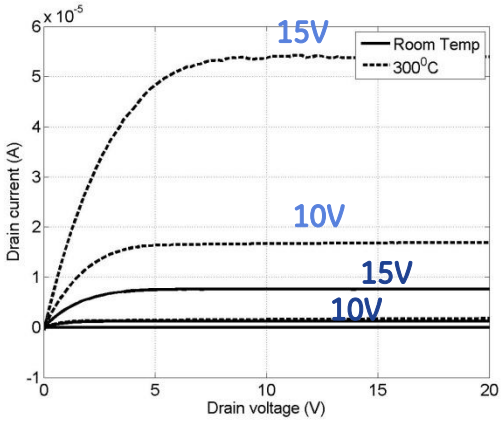


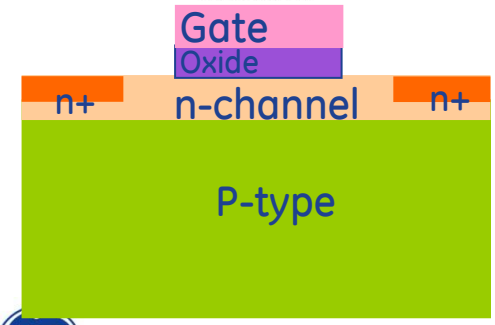
Silicon Carbide

The band gap of SiC (3.26 eV) compared to the band gap of Si (1.12eV) is the reason for the low leakage of p-n junctions at high temperatures

SiC MOSFETs







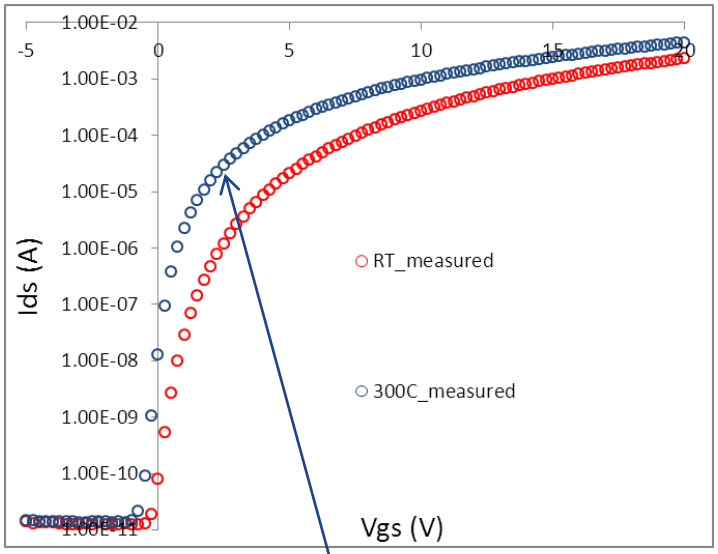
Enhancement-mode MOSFET

- Normally off – Efficient use of semiconductor real estate, ease of scaling
- Low mobility due to poor oxide carbide interface leads to poor performance, operate only in saturation region
- Threshold voltage temperature coefficient is much larger (~15 mV/°C) than in silicon devices (2 mV/ °C) making analog design more complicated
- Current increases with increasing temperature – conventional silicon modeling tools cannot be used

Depletion-mode MOSFET

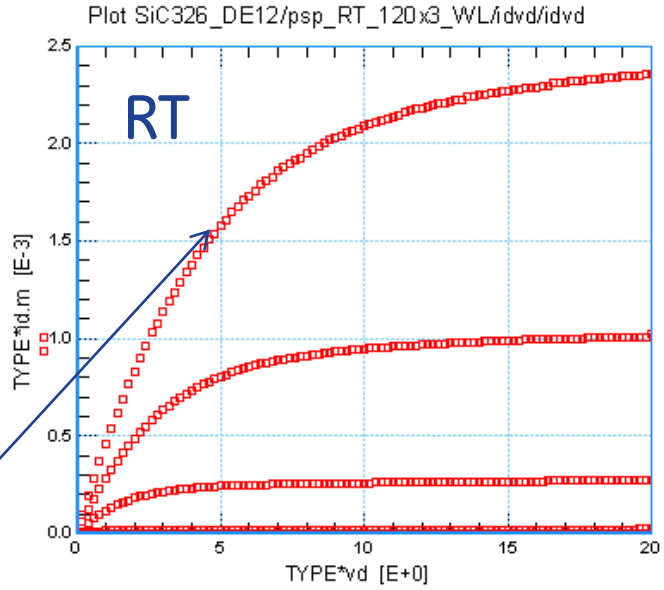
- Normally on – Inefficient use of real estate for digital circuits
- Low E_{field} intensity in drain region – Higher reliability of gate oxide
- High mobility of channel electrons and can be operated in linear region
- A building block for analog circuits

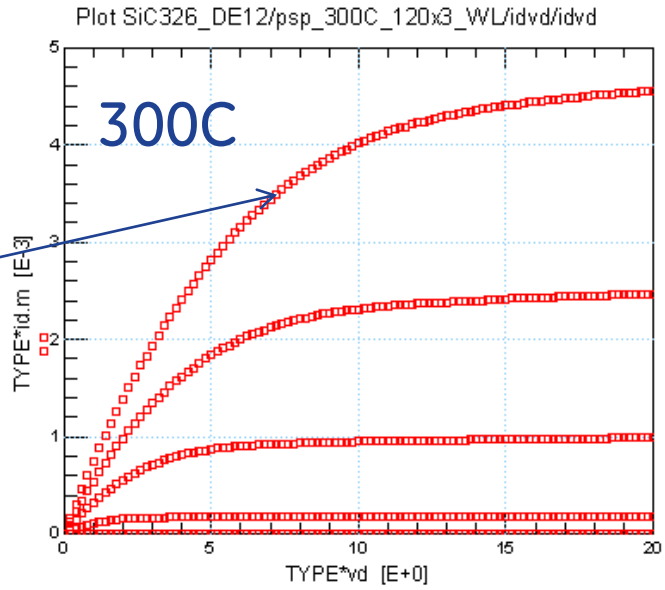
SiC LFET Temperature Behavior



Transfer curve gets sharper (less leaky) at 300C

Output current higher at 300C compared to RT





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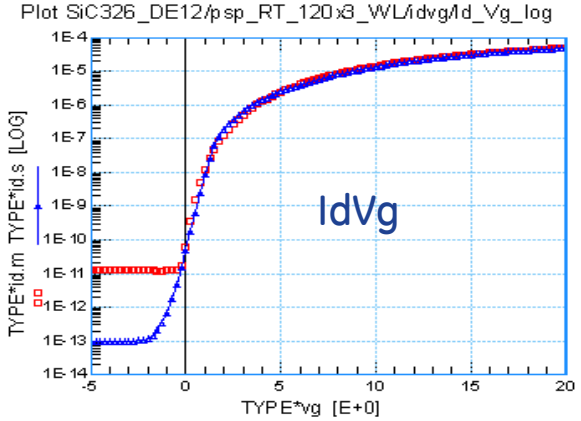
Device Modeling

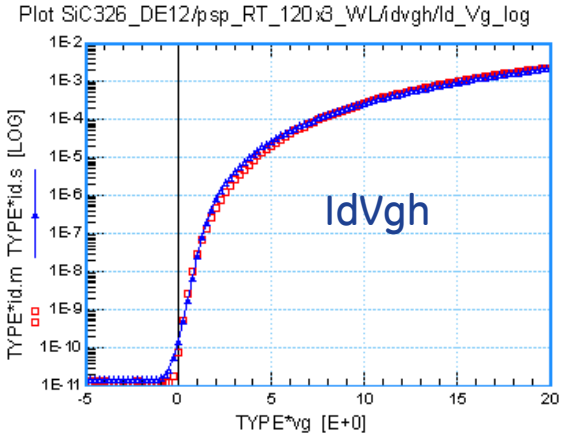
- No native compact models for SiC LFETs
- Physics of SiC-SiO_2 interface still under investigation
- No universal mobility curve – mobility greatly affected by interface quality (surface roughness)
- Temperature behavior different from Si devices

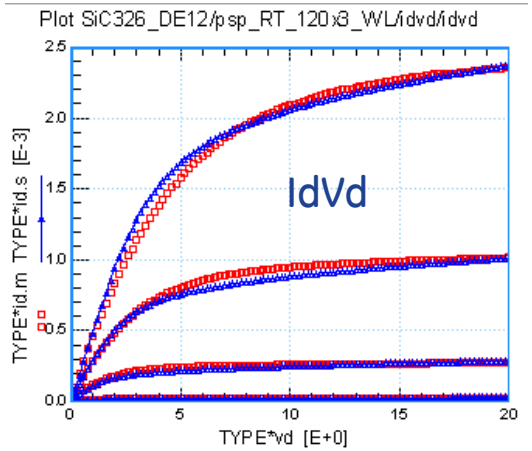
Device Modeling

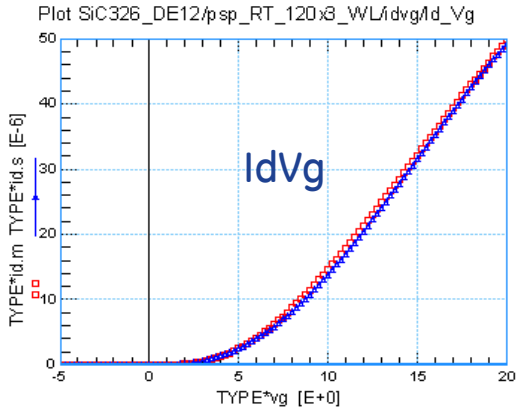
- SPICE Level 2 and Level 3 models used initially
- They were insufficient in the subthreshold region and scaling was poor
- Current CMC standard PSP model was then used to model the FETs
- Binned approach taken for temperature scaling

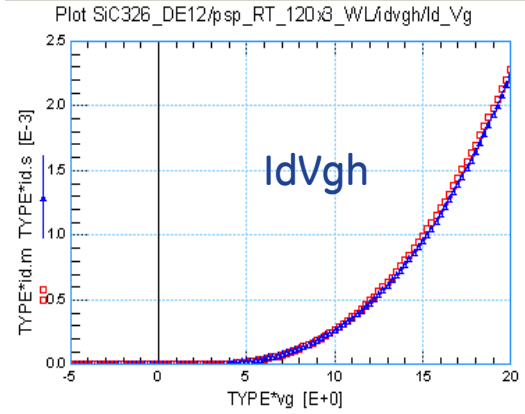
PSP Model Performance – 120ux3u NMOS @ RT

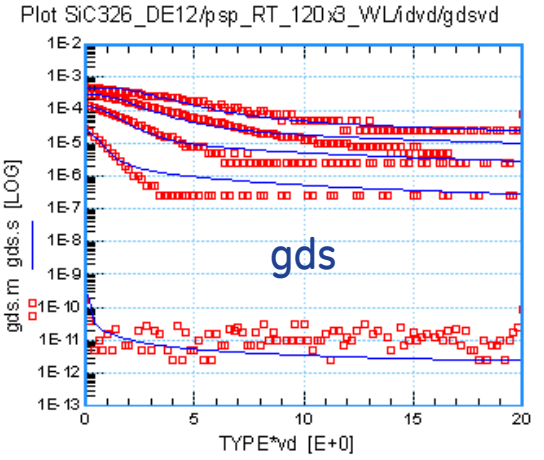












Transfer characteristics at Vds=0.1V
Transfer characteristics at Vds=15V
Drain family at Vgs=0V-20V in steps of 5V
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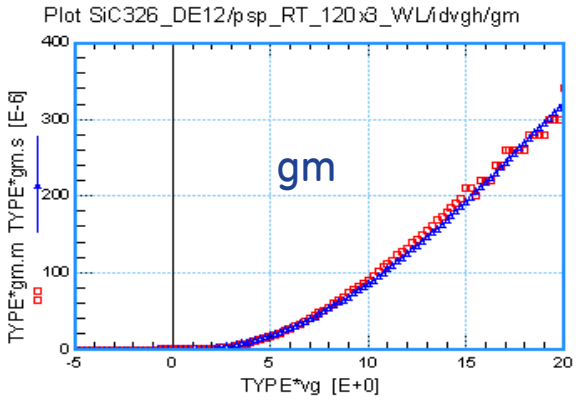
Transconductance (gm) at Vds=15V



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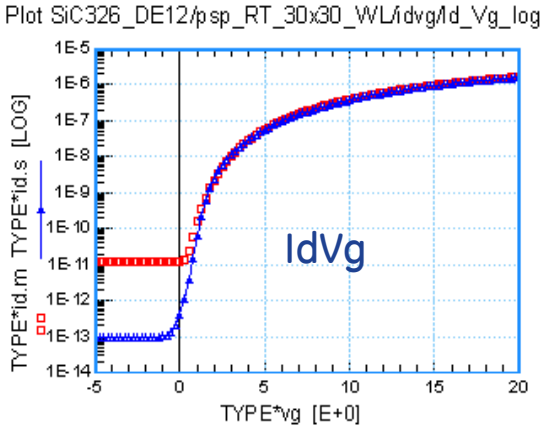
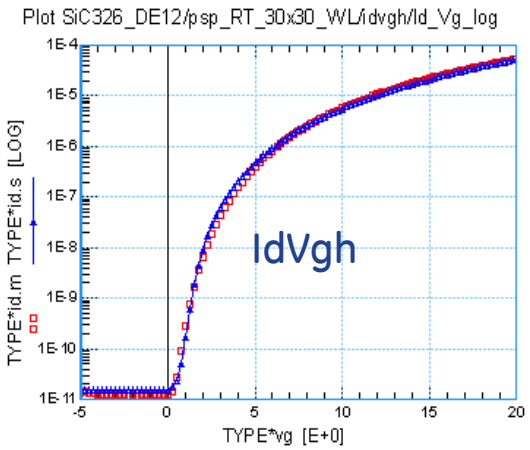
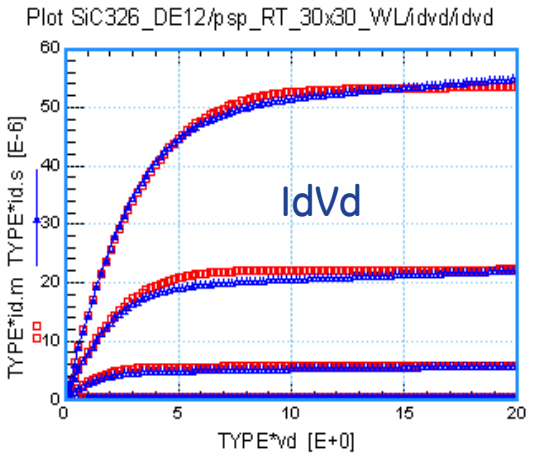
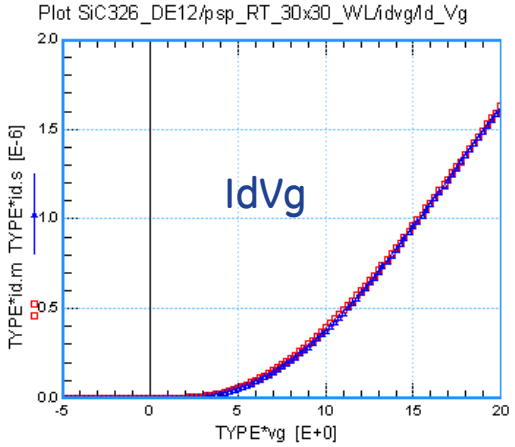
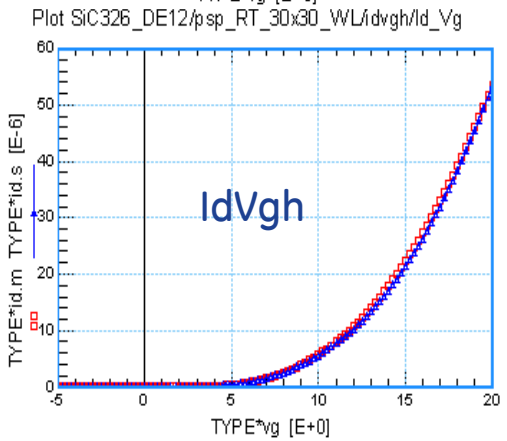
PSP Model Performance – 30ux30u NMOS @ RT

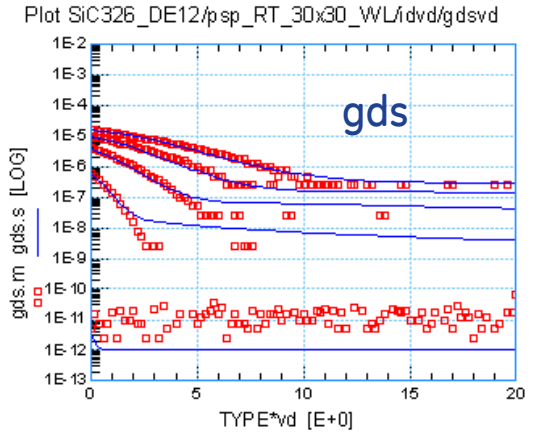


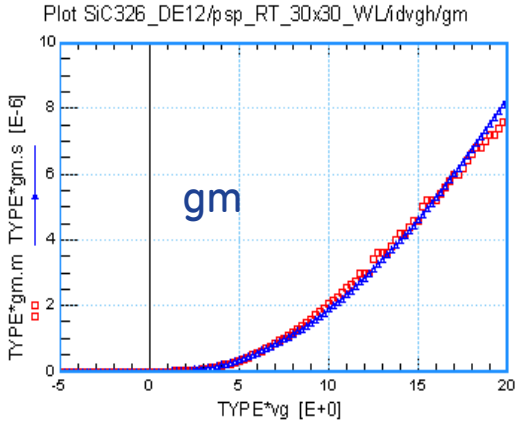












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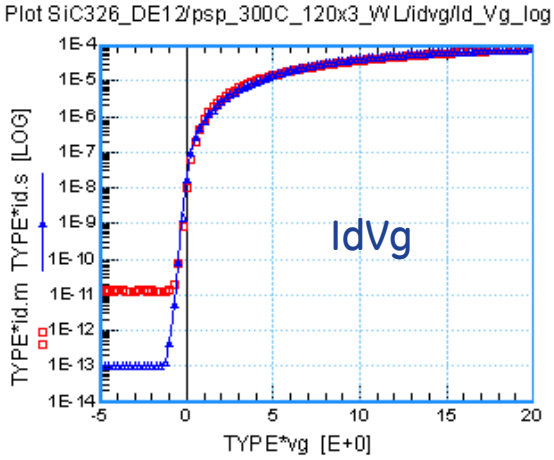
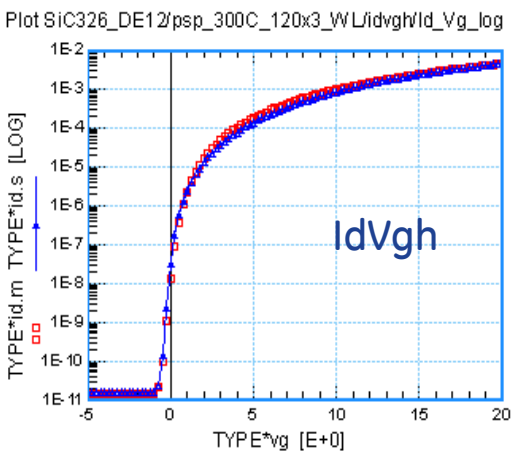
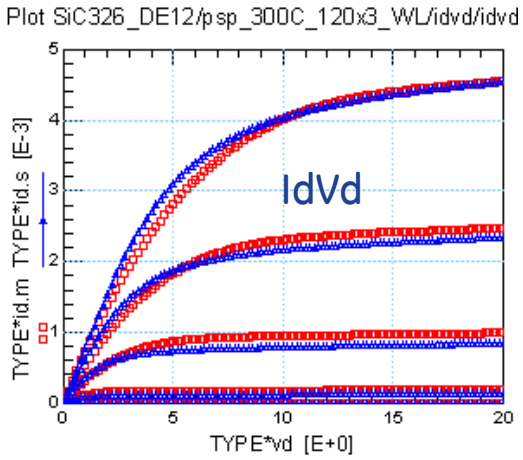
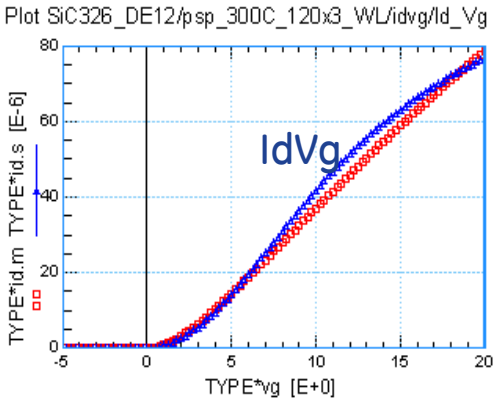
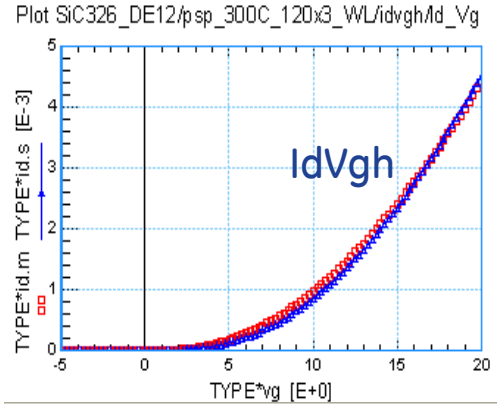
PSP Model Performance – 120ux3u NMOS @ 300C

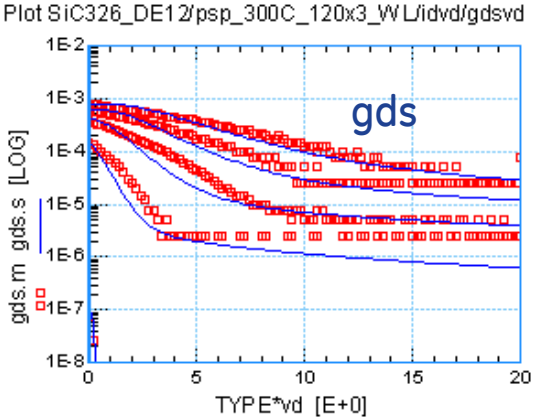


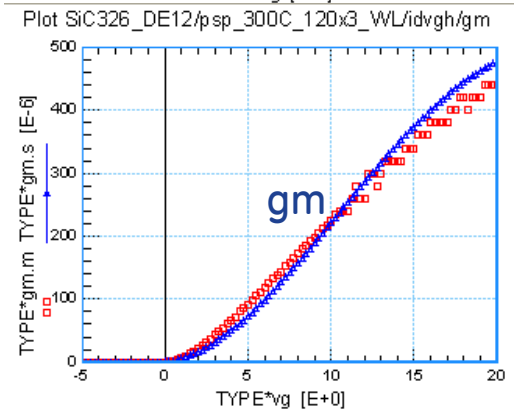












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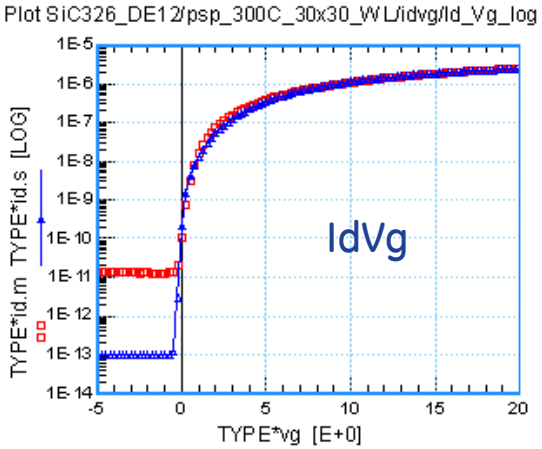
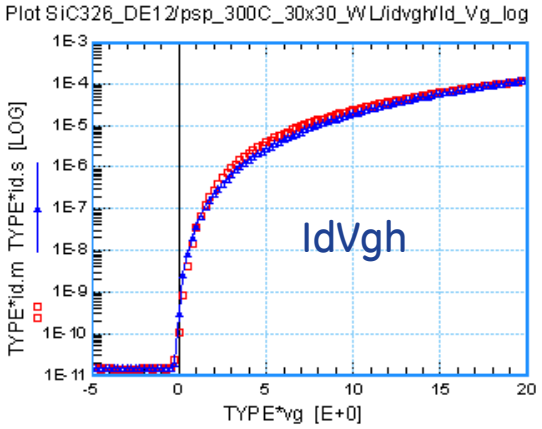
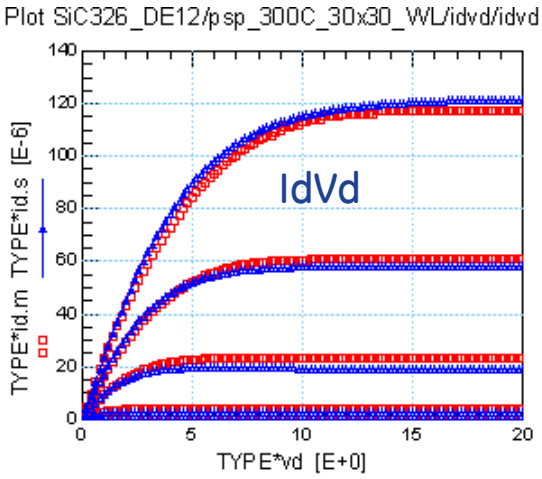
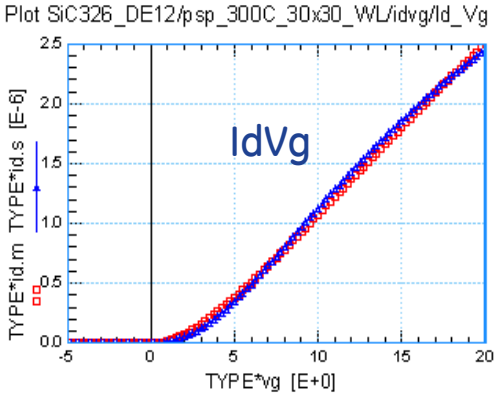
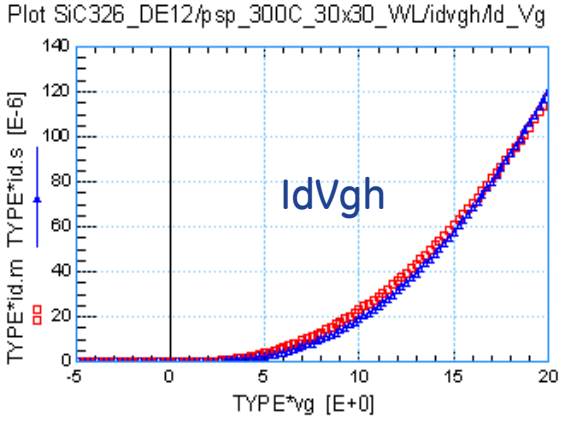
PSP Model Performance – 30ux30u NMOS @ 300C

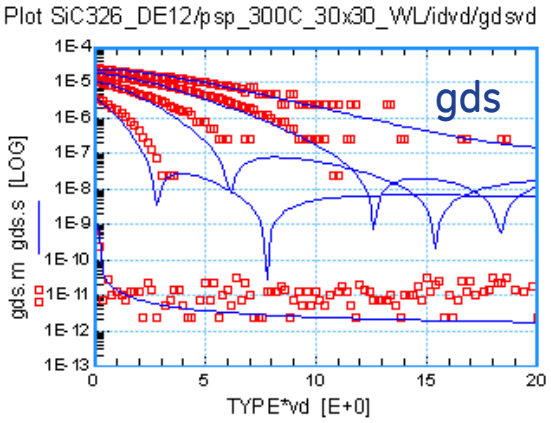


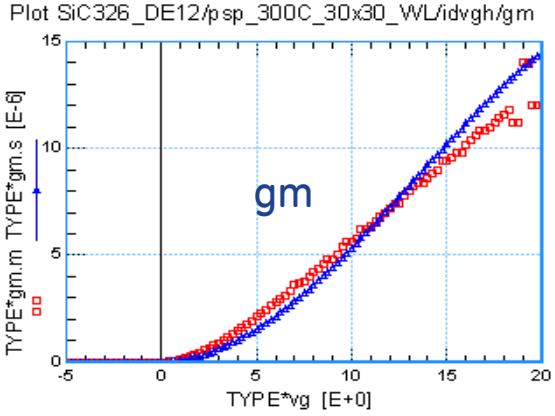












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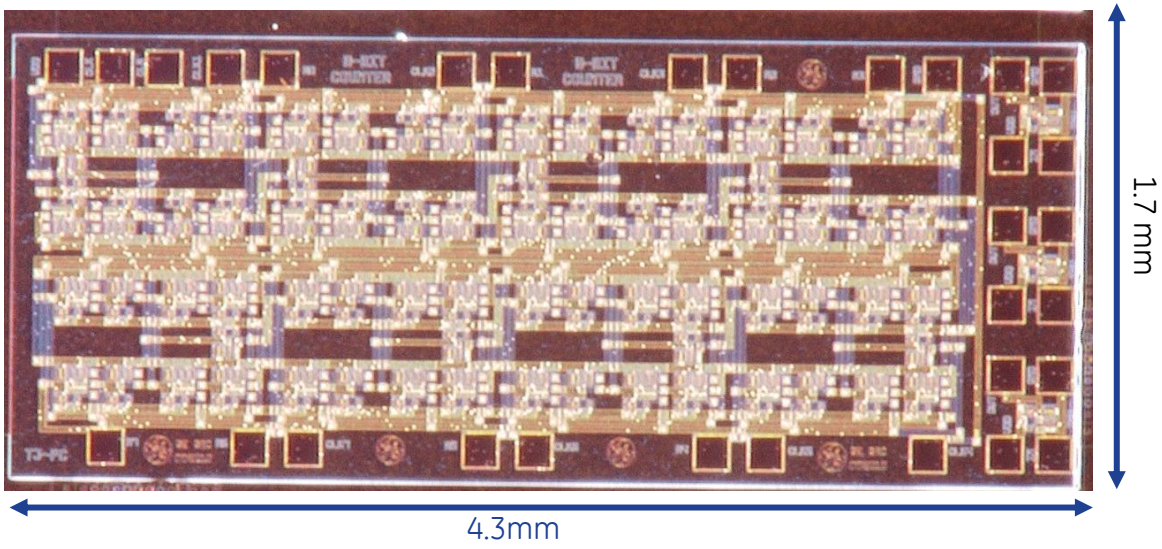
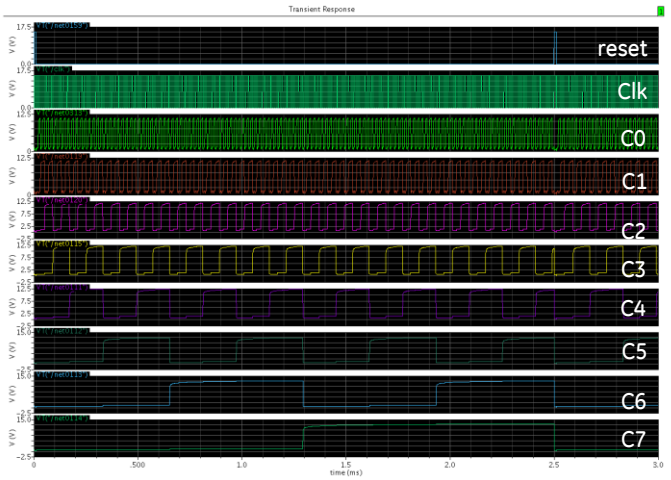
Parameter Extraction

- Extraction methodology provided by NXP had to be modified
- CT (interface states parameter) and CS (coulomb scattering parameter) had to be introduced in multiple steps
- Several iterations needed to extract parameters successfully

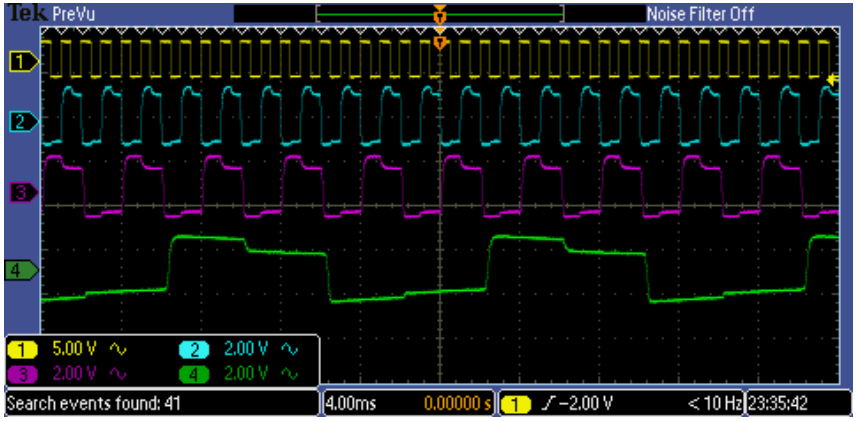
Digital IC lot Design and Fabrication

8-bit counter IC containing nearly 280 transistors

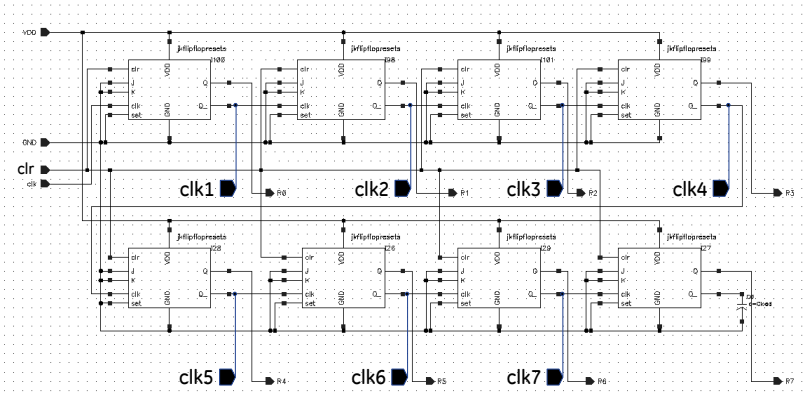




Simulation of 8-bit counter at 300C



300C 4-bit Counter waveform



Schematic of 8 bit digital counter IC

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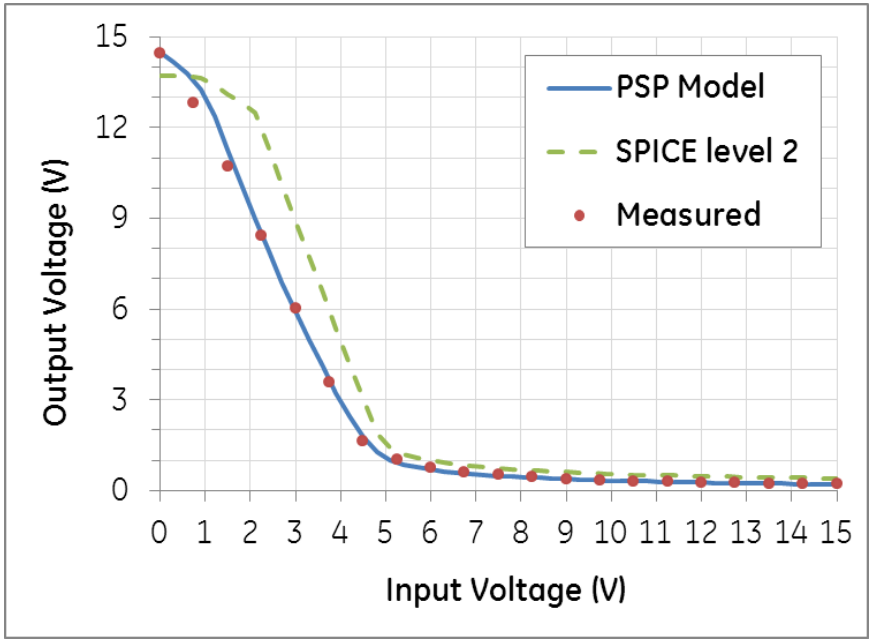
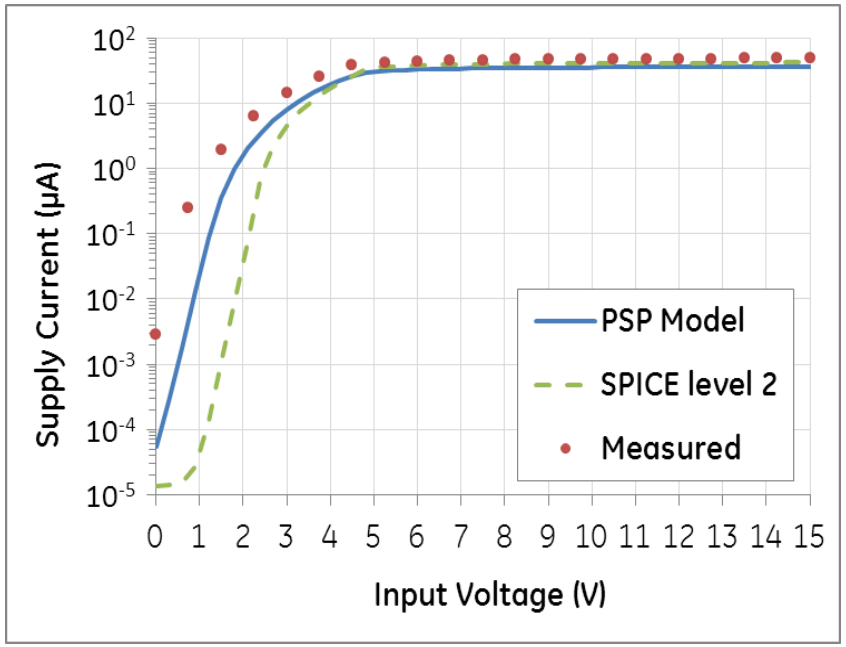
Model Validation With Fabricated Ckt



Measured and simulated Vout vs. Vin for SiC inverter at 300°C.



Measured and simulated supply current vs. Vin for SiC inverter at 300°C.

Summary

- High temperature integrated circuits needed for geothermal exploration
- SiC most promising candidate
- PSP model was successfully used to extract parameters for enhancement mode devices
- PSP model can be enhanced to include SiC device physics
- Circuits designed with above model used to build extreme environment circuits
- Circuits currently undergoing long term reliability testing at GE