Device Modeling
and
Technology Characterization

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Modeling and Technology Characterization Department

- Company overview
- Modeling Department overview
- Test Chip
- Technology Characterization
- Model Quality ‘Metric’
- Conclusions
Corporate Overview

● Leading provider of:
  ● High-performance, field-programmable RISC Microcontrollers and Digital Signal Controllers
  ● Analog and Interface products
  ● Non-volatile EEPROM and Flash Memory products
  ● Flash IP solutions

● ~ $1.8 Billion revenue

● More than 8,000 employees

● Headquartered near Phoenix in Chandler, AZ
Balanced Revenue

Over 80,000 Customers!!
Annual Net Sales Growth

- 92 consecutive quarters of profitability

$ Million

FY93  FY94  FY95  FY96  FY97  FY98  FY99  FY00  FY01  FY02  FY03  FY04  FY05  FY06  FY07  FY08  FY09  FY10  FY11  FY12  FY13

MCU | Memory | Analog | Licensing | Other
Modeling Department
Design and layout our test structures
Develop measurement procedures and do the measurements

Generate device models

Technology Characterization
Validate and ‘measure’ goodness of foundry provided models
Validate ‘parts’ of foundry provided PDKs
Joint device development projects with internal and external fabs
Test Chip
Test Structure Selection
TEST CHIP

◆ Purpose
  ➢ Technology electrical characterization
  ➢ Model validation

◆ All supported devices represented on test chip
  ➢ Internal—additional ‘special’ devices
  ➢ External—Microchip’s device representation

◆ Passive devices included on test chip

◆ All measurements made on wafer(s), not packaged devices or scribe structures
Technology Test Chip
Technical Justifications for Foundry

- Technology Characterization
  - Guides for more intelligent engagement in a particular technology such as standard cells modified for a particular technology
  - Data not available from foundry
  - Validation of foundry data
  - Device support of design debugging (i.e. validation of resistor tempcos)
  - Characterization of ‘new’ effects at these advanced nodes, (i.e. WPE, LOD, etc.), which helps to support analog designs.
- Microchip specific tests and exercise of the supported devices
- Validate foundry process capability which results in better manufacturability or higher yields of products at new technology nodes.
Technology Test Chip
Technical Justifications for Foundry

- **Model Validation and Enhancements**
  - Validate foundry provided models
  - Enhance or improve accuracy of foundry provided models
  - Validation of models at extended temperature or extended bias ranges
  - Validation of layout effects such as WPE, LOD, and CGSC

- **Monitoring or re-characterization of technology in the future**
  (ability to determine electrically ‘deltas’ in device characteristics).

- **Internal Technology Development**
  - Over 50% of test structures on test chips are designed for technology characterization
  - New supported devices are characterized
  - Ability to monitor device characteristics over time
  - Ability to determine process cliffs
W - L Space
Our typical representation of W-L space

- It depends on our engagement of the technology
- It enables us to create device models if the need exists
- It assists with validation of certain aspects of the device models in our applications
- Validation of layout effects such as WPE, LOD, and CGSC

Foundry representation of W-L space

- Used to generate device models
- It is their ‘generic’ representation of the W-L space

Typical Test chip is a combination of both representations of the W-L space
TECHNOLOGY CHARACTERIZATION

STANDARD CELL DEVELOPMENT
0.25μ Matrix Lot
SubVt Intercept  LV-NMOS
Vds=2.5V   25C
All Splits    - - - - Nominal Size

Channel Length (microns)

pamps/µ-width

Wafer 3-SSS
Wafer 5-SST
Wafer 7-SFT
Wafer 9-FST
Wafer 11-FFT
Wafer 13-FFF
Wafer 25-TTT
Technology 'Node' Performance Comparison
Subthreshold Intercept vs. Gate Delay
Typical Process Vdd = Nominal

Product Requirements

Cell Lib. A (T= 25,85,125)

Cell Lib. B (T= 25,85,125)

Cell Lib. C (T= 25, 85, 125)
Technology 'Node' Performance Comparison
Subthreshold Intercept vs. Gate Delay
Typical Process  Vdd = Nominal

Product Requirements

Gate Delay (psec.)

Subthreshold Intercept (pamp/µ-width) [n+p]
Model Quality ‘Metric’
Mathematical robustness
- Negative resistances, discontinuities in models (especially at bin boundaries)
- Temperature stability (especially over the complete W-L space)

Standard dc and small signal data compared to models
- Corner model validation
- Monte-Carlo validation of variation
- Validate mismatch, layout effects (WPE, LOD, etc) with silicon measurements
- Low power requires good sub-threshold models or a measure of ‘goodness’
- Ring oscillator measurements and simulation comparison over Vdd and temperature range
w(um)=10; L(um)=0.5; vbs(V)=0; T(C)=0

Vgs (V)
0.00
0.33
0.66
0.99
1.32
1.65
1.98
2.31
2.64
2.97
3.30
3.63

Ids (A)
5.65E-3
4.24E-3
2.82E-3
1.41E-3
-4.36E-7

Vds (V)
0.00
0.825
1.65
2.47
3.30

RMS: 0.052
MAX: 0.082

Group
- Mea
- Model
Modeling and Technology Characterization Department

Ion vs Ioff  W/L = 10/0.5

T=25°C
T=125°C
T=160°C
CONCLUSIONS

- Device modelers need a variety of skills
- Engaging with foundries ‘intelligently’ requires more than accessing ‘off the shelf’ design collateral (PDKs)
- Variety of tools are available to help with efficient model quality evaluation

THANK YOU