MICROCHIP

Device Modeling and Technology Characterization

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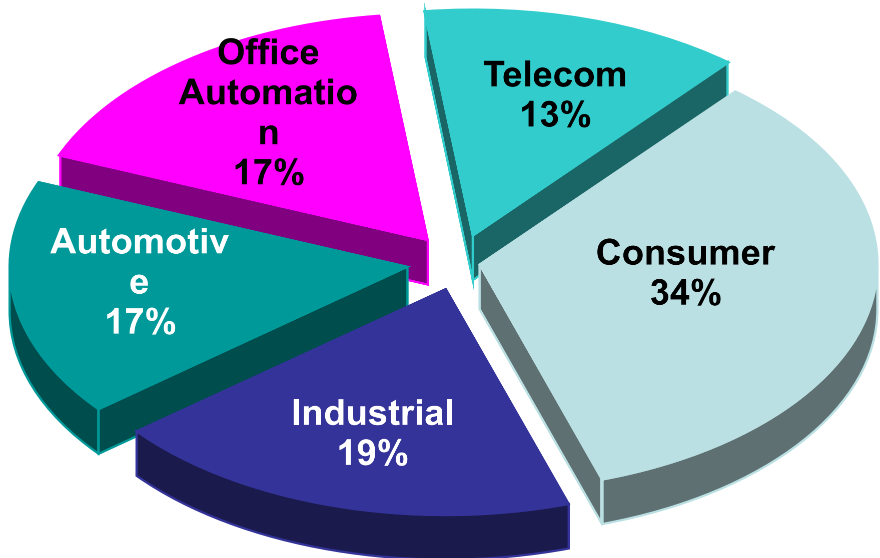
- Company overview
- Modeling Department overview
- Test Chip
- Technology Characterization
- Model Quality ‘Metric’
- Conclusions

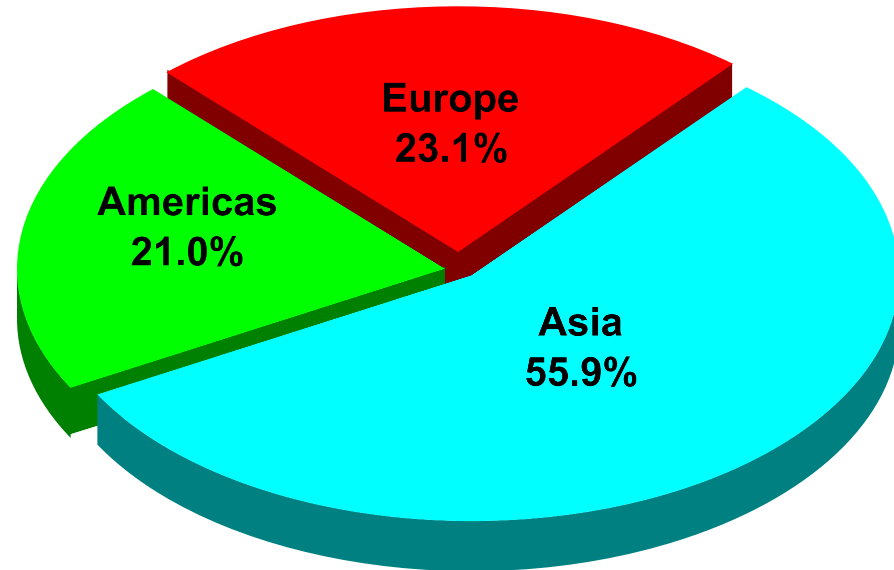
MICROCHIP

Corporate Overview

- **Leading provider of:**
  - High-performance, field-programmable RISC Microcontrollers and Digital Signal Controllers
  - Analog and Interface products
  - Non-volatile EEPROM and Flash Memory products
  - Flash IP solutions
- **~ $1.8 Billion revenue**
- **More than 8,000 employees**
- **Headquartered near Phoenix in Chandler, AZ**

Balanced Revenue





Over 80,000 Customers!!

Annual Net Sales Growth

Modeling Department

Modeling and Technology Characterization Department

- Design and layout our test structures
- Develop measurement procedures and do the measurements
- *Generate device models*
- Technology Characterization
- Validate and ‘measure’ goodness of foundry provided models
- Validate ‘parts’ of foundry provided PDKs
- Joint device development projects with internal and external fabs

Test Chip

Test Structure Selection

TEST CHIP

- **Purpose**
  - Technology electrical characterization
  - Model validation
- **All supported devices represented on test chip**
  - Internal—additional 'special' devices
  - External—Microchip's device representation
- **Passive devices included on test chip**
- **All measurements made on wafer(s), not packaged devices or scribe structures**

Technology Test Chip
Technical Justifications for Foundry

- Technology Characterization
  - Guides for more intelligent engagement in a particular technology such as standard cells modified for a particular technology
  - Data not available from foundry
  - Validation of foundry data
  - Device support of design debugging (i.e. validation of resistor tempcos)
  - Characterization of 'new' effects at these advanced nodes, (i.e. WPE, LOD, etc.), which helps to support analog designs.
- Microchip specific tests and exercise of the supported devices
- Validate foundry process capability which results in better manufacturability or higher yields of products at new technology nodes.

Technology Test Chip
Technical Justifications for Foundry

- **Model Validation and Enhancements**
  - Validate foundry provided models
  - Enhance or improve accuracy of foundry provided models
  - Validation of models at extended temperature or extended bias ranges
  - Validation of layout effects such as WPE, LOD, and CGSC
- **Monitoring or re-characterization of technology in the future**
  (ability to determine electrically 'deltas' in device characteristics).
- **Internal Technology Development**
  - Over 50% of test structures on test chips are designed for technology characterization
  - New supported devices are characterized
  - Ability to monitor device characteristics over time
  - Ability to determine process cliffs

W - L Space

MICROCHIP

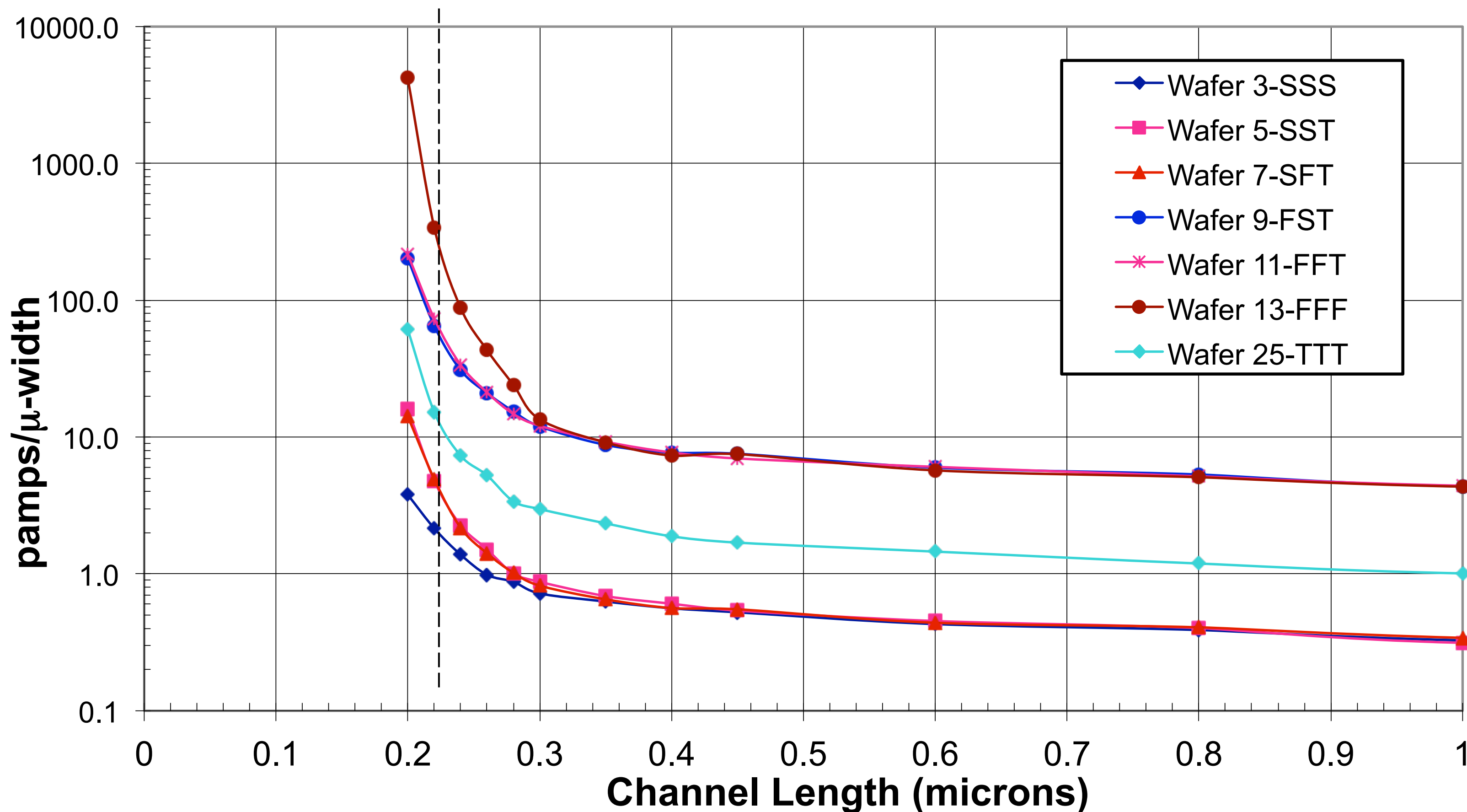
W-L Space Representation

- Our typical representation of W-L space
  - It depends on our engagement of the technology
  - It enables us to create device models if the need exists
  - It assists with validation of certain aspects of the device models in our applications
  - Validation of layout effects such as WPE, LOD, and CGSC
- Foundry representation of W-L space
  - Used to generate device models
  - It is their ‘generic’ representation of the W-L space
- Typical Test chip is a combination of both representations of the W-L space

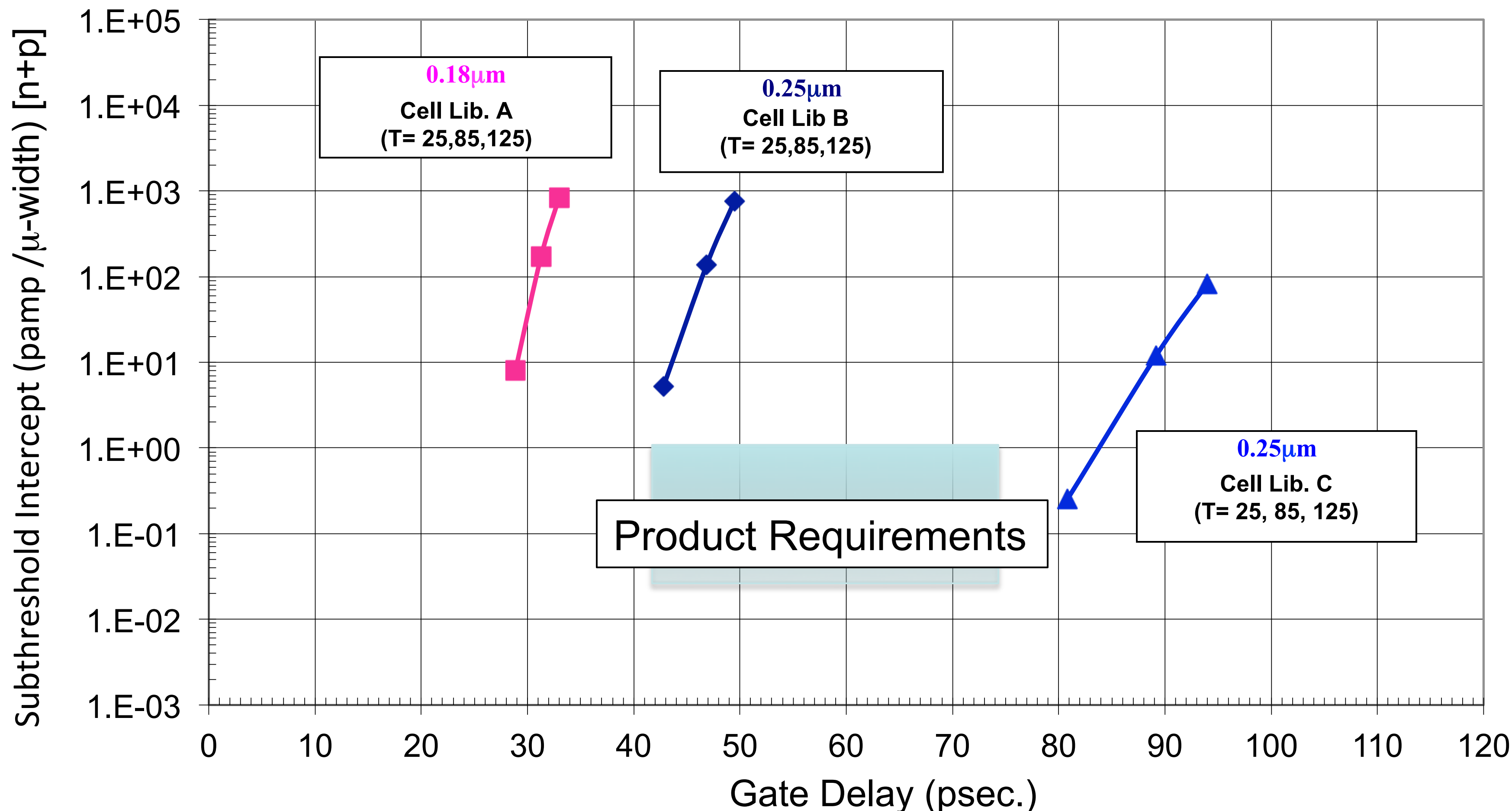
TECHNOLOGY CHARACTERIZATION

STANDARD CELL DEVELOPMENT

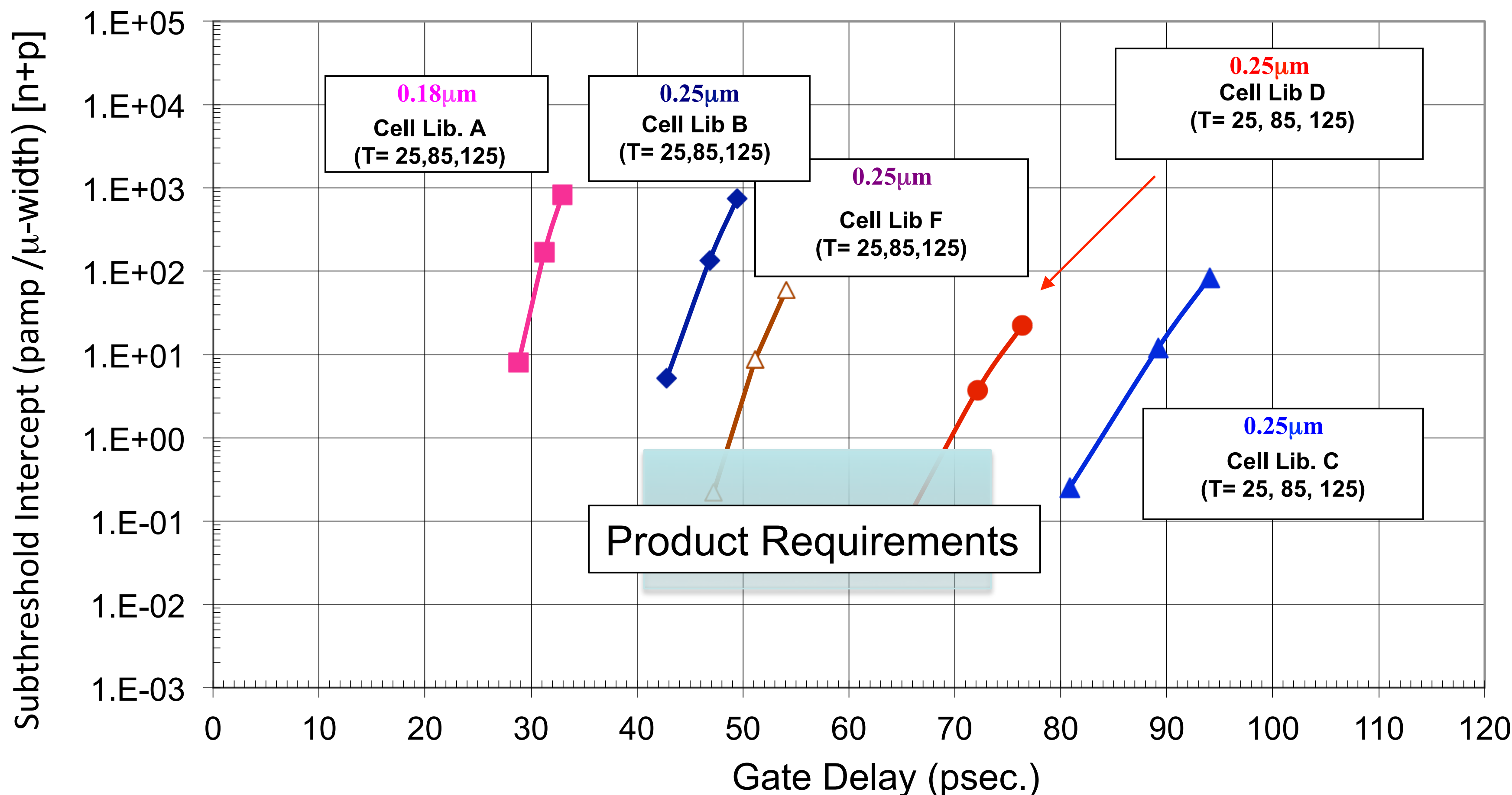
Modeling and Technology Characterization Department



Modeling and Technology Characterization Department



Modeling and Technology Characterization Department



Model Quality 'Metric'

- **Mathmatical robustness**
  - Negative resistances, discontinuities in models (especially at bin boundaries)
  - Temperature stability (especially over the complete W-L space)
- **Standard dc and small signal data compared to models**
  - Corner model validation
  - Monte-Carlo validation of variation
  - Validate mismatch, layout effects (WPE, LOD, etc) with silicon measurements
  - Low power requires good sub-threshold models or a measure of ‘goodness’
  - Ring oscillator measurements and simulation comparison over Vdd and temperature range

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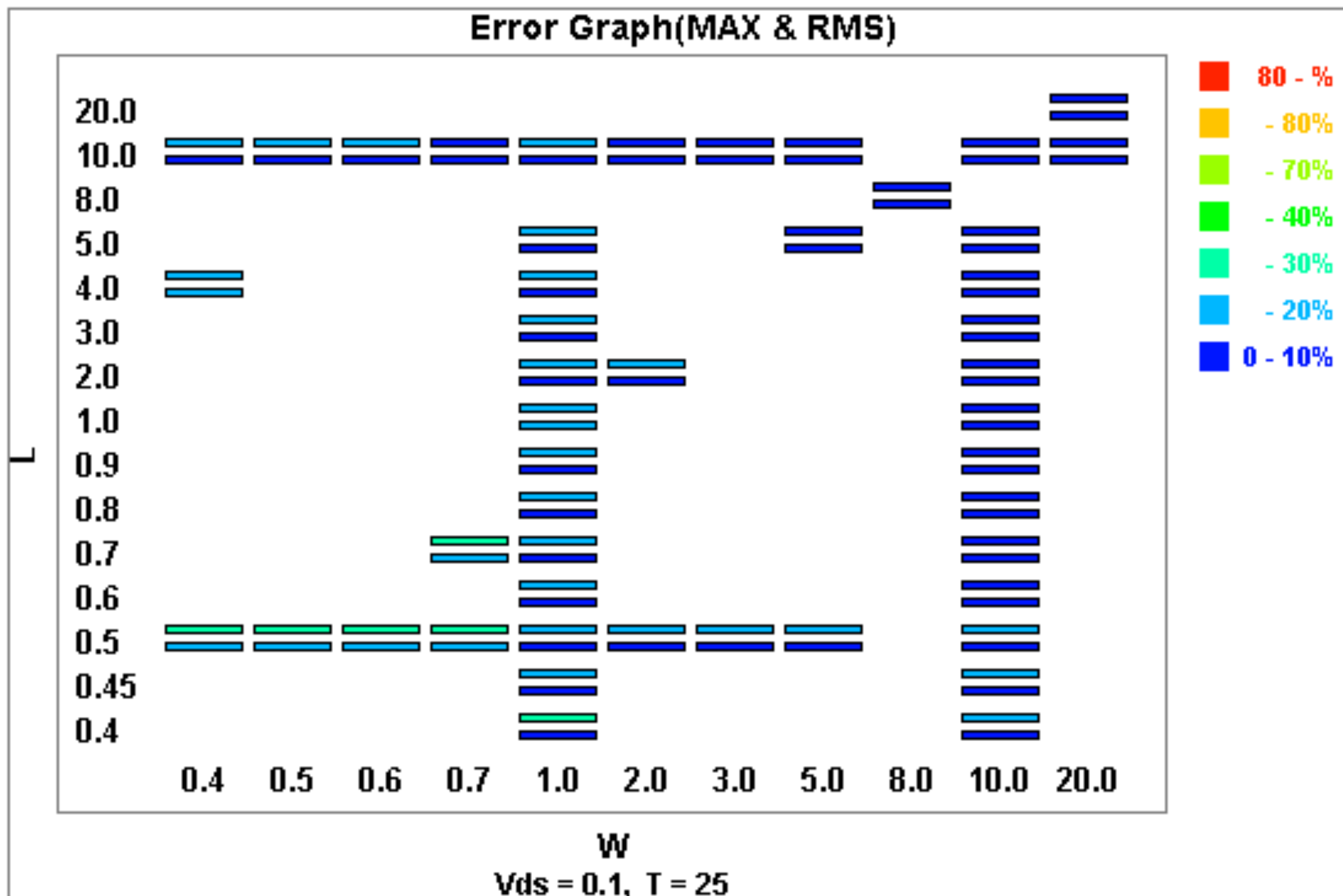

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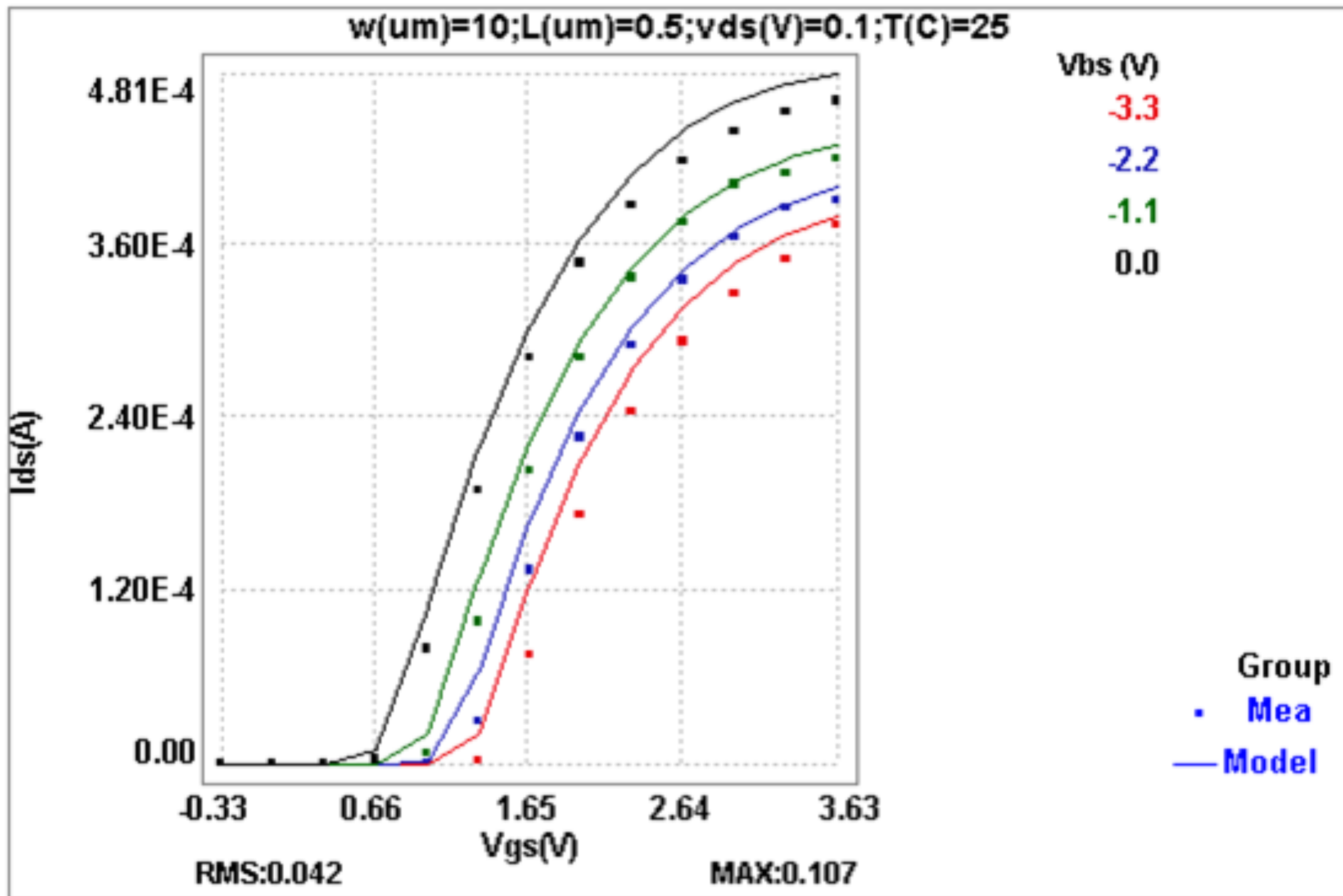

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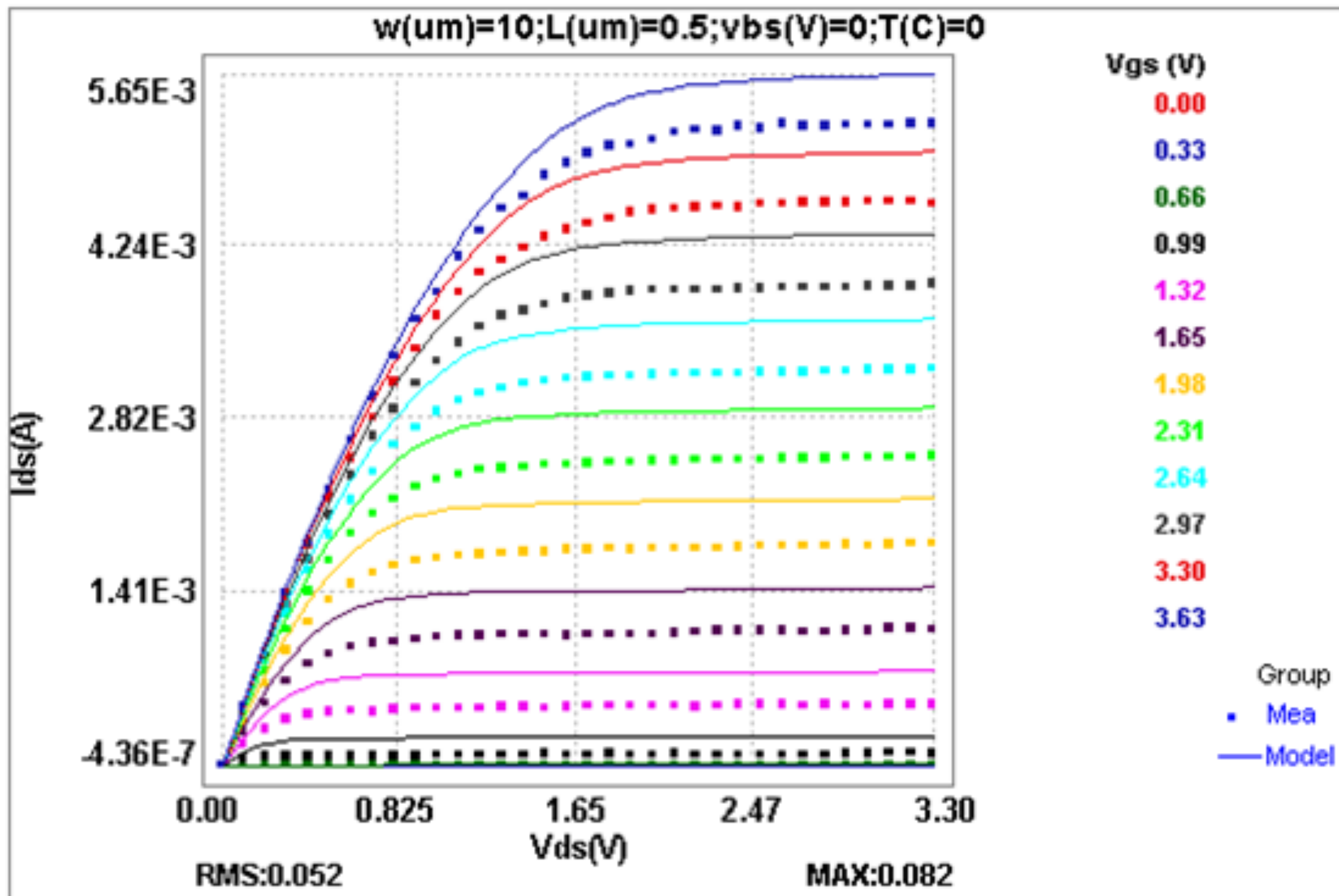
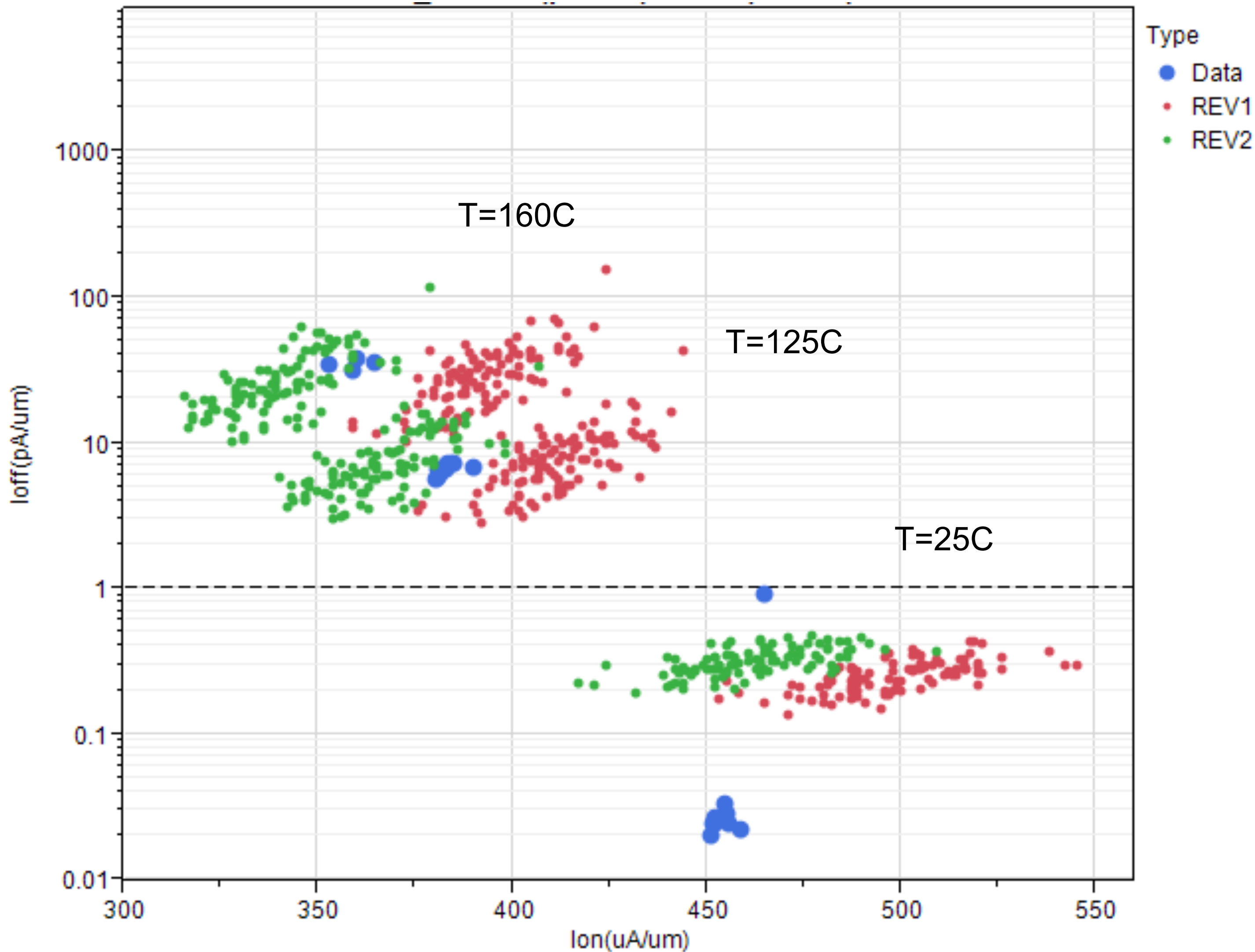


Modeling and Technology Characterization Department

Ion vs Ioff W/L = 10/0.5



CONCLUSIONS

- Device modelers need a variety of skills
- Engaging with foundries ‘intelligently’ requires more than accessing ‘off the shelf’ design collateral (PDKs)
- Variety of tools are available to help with efficient model quality evaluation

THANK YOU