IEEE EDS CM-TAC Overview

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Washington, DC

IEEE Electron Devices Society (EDS)

- 14 Technical Area Committees (TACs)
  - under VP of Technical Activities Prof. Burghartz
- One of these is Compact Modeling (CM)
- Revitalized at the start of 2013
  - converged on list of goals
  - commenced work on these goals
- Highlighted in October 2013 issue of EDS Newsletter

40 of them invited, 3 book chapters and 8 patents. He is the founding director of the MIT Center for Graphene Devices and 2D Systems, and the MIT GaN Energy Initiative.

Elison Matioli received his B.Sc. degree from Ecole Polytechnique (France) in 2006 and his Ph.D. degree

from the Materials Department at the University of California, Santa Barbara in 2010, working on GaN-based LEDs and solar cells. He is currently a post-doctoral fellow in the Electrical Engineering and Computer Science Department at MIT working on GaN-based transistors.

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Technical Activities Committee on Compact Modeling launches platform on Verilog-A modeling

Colin McAndrew
EDS Compact Modeling TAC Chair

Research and development on semiconductor devices has been an exciting field to work in for the past 60 or so years. That field, and many of our jobs, has been funded by the economic engine that is the microelectronics industry: Basic device research is fun and intellectually satisfying, but it is the integrated circuits (ICs), and products they are used in, that provide the revenue needed to keep the industry moving forward. Since the 1970's IC design has been based on SPICE simulation, and the basic electron devices are encapsulated in SPICE in the form of models, called *compact models*. Compact models are, in essence, the key link between process technologies and circuit design. As devices, and the physical phenomena that affect their electrical behavior, continue to evolve, so must compact models. Although there is an industry standards body for the area, the Compact Model Coalition (CMC), it strives to respond quickly to business needs rather than driving for the best possible technical and physically rigorous approaches and solutions. The IEEE Electron Devices Society therefore has a Technical Area Committee (TAC) on compact modeling (CM) to concentrate on the technical aspects of compact modeling.

After several rounds of brainstorming, on where the IEEE EDS CM-TAC (that's quite a mouthful of acronyms!) could most profitably direct its attention, we came up with a list that includes these items:

- Officially document compact model benchmarks (assemble and place under the IEEE umbrella all the existing work on benchmarks).
- Provide standard Verilog-A macro definitions for general common compact modeling needs.
- Provide standard Verilog-A macro definitions for *p-n* junctions (which appear as intentional or parasitic parts of many semiconductor devices).
- Define coding standards for Verilog-A.
- Provide simple but non-trivial Verilog-A examples for people to use as a starting point for other models.

This is an aggressive set of goals, but by setting standards to evaluate the physical correctness of compact models and collating and expanding best practices in Verilog-A coding of compact models we intend to help the industry raise the bar on quality. The need for education in these areas may seem curious: Surely it's obvious whether a compact model is physically correct or not? And the adoption of Verilog-A as the *de facto* standard for compact modeling a decade ago completely removed the major cause of errors in compact model (wrong derivatives; these are automatically generated in Verilog-A), so Verilog-A models should be higher quality than C code, right?

Sadly, that is not always the case. Verilog-A is a flexible language, flexible enough to allow you to implement unphysical or poorly converging models (gives you "enough rope to hang yourself" as the saying goes). And it significantly lowers the entry barrier to developing a compact model, opening the field to people not tutored in how to write a good model. Best practices for writing models in Verilog-A have been documented, but are not widely known and rarely followed. The initial focus of the CM-TAC has therefore been on assembling, extending, and explaining the reasons that underlie recommended best practices for Verilog-A modeling, and providing standard macro definitions to help people writing Verilog-A models adopt common practices (besides providing a more consistent coding style for models this can also help EDA companies implement models). We have had several rounds of iteration in documenting the best practices and standard macro definitions, and are now deciding how

Participants

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Colin McAndrew (chair)	Freescale
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also contributions by: Kiran Gullapalli (Freescale), Gert-Jan Smit (NXP)

Ground Rules

- Objective: 100% technical
- All output completely publically available
- EDS TAC aims
  - support of EDS VP Publications
  - support of EDS VP Conferences

Goals

1. **Define coding standards for Verilog-A**
2. **Provide general Verilog-A macros**
3. **Provide *pn*-junction Verilog-A macros**
4. **Provide simple, but non-trivial, Verilog-A examples**
5. **Document compact model benchmarks**
   - assemble in one place (exist already, but in disparate places)
6. **Set up CM "open issues" list**
7. **Endorse Verilog-A→SPICE code generator**

Status

- **Emphasis to date is Verilog-A "best practices"**
  - **despite good information already existing (Coram, BMAS 2004) it is widely ignored**
- **CMC and NEEDS also targeting this**
  - **CM-TAC includes key CMC and NEEDS people**
- **"Best practice" document drafted**
  - **asked to propose as article for JEDS**
    - Journal of the Electron Device Society
    - Open-Access, all-electronic IEEE EDS publication
- **At present revising for JEDS submission**

Status (cont'd)

- Have defined both general and *pn*-junction Verilog-A macros
  - will provide on IEEE EDS web site
- Have an initial example model
  - significantly enhanced R3 model for JFETs and nonlinear resistors (diffused and poly)

R3 Enhancements

- **Extended temperature, geometry dependence**
  - **necessary for velocity saturation**
- **Enabled both depletion pinching and velocity saturation effects to be made arbitrarily small**
  - **necessary for poly resistors**
  - **without *any* numerical issues**
    - highly nontrivial to do, even though sounds easy
- **Significantly improved JFET modeling**
  - **DIBL, CLM, vastly improved full pinch-off model**
- **Many other less major updates**
- **All based on extensive comparison to data**