Xyce Update

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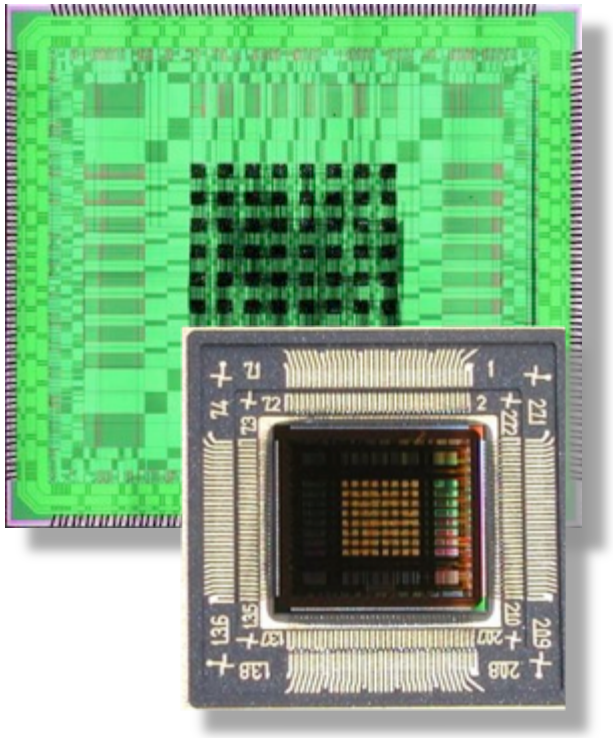
Xyce Parallel Circuit Simulator

- Xyce: Massively Parallel circuit simulator:
  - Distributed Memory Parallel (MPI-based)
  - Unique solver algorithms
  - SPICE “Compatible”
  - Industry standard models (BSIM, PSP, EKV, VBIC, etc)
  - ADMS model compiler
- Analysis types
  - DC, TRAN, AC
  - Harmonic Balance (HB)
  - Multi-time PDE (MPDE)
  - Model order reduction (MOR)
  - Direct and Adjoint sensitivity analysis
  - Uncertainty quantification (UQ) via Dakota.
- Sandia-specific models
  - Prompt Photocurrent
  - Prompt Neutron
  - Thermal
- Other, non-traditional models
  - Neuron/synapse
  - Reaction network
  - TCAD (PDE-based)
- Xyce Release 6.4
  - Open Source!
  - GPL v3 license



http://xyce.sandia.gov

Next release (v6.4) ~December 2015

Open Source Releases

Release every 6 months.

Xyce v6.0 (first open source) October, 2013

Xyce v6.1 April 2014

- Parallel HB, MPDE and AC analysis.
- BSIM-CMG model
- New digital models
- Dynamically linkable devices (beta implementation)

Xyce v6.2 October, 2014

- Calculation of transient direct sensitivities.
- Support for lead current calculation and output for Harmonic Balance (HB) analysis.
- Improved interpolation for both the Trapezoid and Gear time integrators.
- Improved results output (.PRINT) capabilities.
- New models for a lumped transmission line and a digital latch.
- Fixes for nearly 60 bugs and enhancement requests.

Open Source Releases

Xyce v6.3 ~April 2015 (Fixed 64 bugs and user requests)

Devices:

- BSIM6 version 6.1.0
- MEXTRAM version 504.11.0
- TEAM memristor model
- Power grid models (Branch, Bus Shunt, Transformer and Generator Bus)

Solvers/Analysis:

- Multi-tone HB (unlimited # of tones)
- Small-signal noise analysis
- Auto-detection/application of MOR to linear subcircuits
- DC operating point solution strategy now includes SPICE-like source stepping if Newton or GMIN stepping fail.

Interace Improvements:

- Improved support for .MEASURE
- Significant reduction in memory footprint during setup phase.
- ADMS back-end extended to produce analytic parameter derivatives
- ADMS back-end improved to more correctly support Verilog-A ternary operators.

Open Source Releases

Xyce v6.4 ~ December 2015 (Fixed 88 bugs and user requests)

Devices:

- VBIC version 1.3 (3- and 4-terminal variants)
- MEXTRAM version 504.11 with self-heating
- Yakopcic memristor model
- Improved Digital behavioral models (better compatibility with Pspice)

Solvers:

- Enhanced Kundert Sparse solver
- Netlist parser refactored to improve memory and parsing speeds for big circuits.
- Improved Harmonic Balance (HB) robustness during the initial guess.
- New Local Truncation Error (LTE) criterions using history (improve time stepping)
- Oversampling capability for Harmonic Balance time domain output.
- Arclength continuation is now much more useful and robust.
- Sensitivity analysis can now allow multiple objective functions.

Interface Improvements:

- Power calculations supported for controlled-source devices (B,E,F,G and H).
- Support for additional .MEASURE statement syntaxes.
- Improved error handling during netlist parsing.
- Improved Harmonic Balance Output.
- Support for DIGINITSTATE; sets initial state of Digital Flip-Flip and Latch devices.

Future Work

Xyce v6.5 ~ April 2016

- Adjoint transient parameter sensitivities
- New direct linear solver (BASKER*) [alternative to KLU]
  - serial version (completed)
  - threaded version (in progress, done by fall 2015)
- ModSpec model compiler support
- ROL optimization library
- Dakota UQ library integration.

BASKER = BASic Sparse KERnels
ROL = Rapid Optimization Library

Longer Term: Flexible support for threading

(Most of Xyce's parallelism based on message-passing)

- Need to accommodate modern computing architectures
- Cuda, TBB, etc
- Kokkos/Tpetra and other threaded-enabled parts of trilinos.

Xyce Summary

- Mature code; under development for 14 years
  - Large regression test suite
  - Regular, formal code releases
- Under active development
- Open source GPL v3.
- Modular object-oriented design
  - DAE form: $\frac{d}{dt}q(x,t) + f(x,t) = b(t)$
  - Quick, independent development of models and algorithms
- Model support
  - Legacy spice models
  - Non-electrical: neuron, reaction networks
  - CMC models
  - ADMS integration
  - Mod-Spec integration

Acknowledgements

Xyce team

xyce.sandia.gov

- Scott Hutchinson
- Tom Russo
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- Ting Mei
- Dave Baur
- Sivasankaran Rajamanickam

Trilinos team

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Dakota team

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