FinFET SPICE Modeling

Synopsys Solutions to Simulation Challenges of Advanced Technology Nodes

Joddy Wang

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Outline

• SPICE Model for IC Design

• FinFET Modeling Challenges

• Solutions

• Summary
SPICE Models for IC Design

- The bridge between fabrication and IC design
- Key component of PDK
BSIM-CMG: Industry Standard Compact Model

• Various device structures

• Technology
  – Bulk and SOI
  – Channel materials: Si, SiGe, Ge, and InGaAs

• Production adoption for 16/14/10/7nm

Extension and customization are required
Self Heating and MOS Reliability in FinFET

- FinFET has more pronounced self heating effect (SHE)
- Increased temperature exacerbates reliability degradation
  - Device aging effect: BTI (Bias Temperature Instability) and HCI (Hot Carrier Injection)
- Concurrent SHE and reliability analysis

\[ \Delta V_t \sim \exp(-n \frac{E_a}{k_B T}) \]

<table>
<thead>
<tr>
<th>Aging simulation</th>
<th>$\Delta T = 20^\circ C$</th>
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<tr>
<td>EM Imax rule reduced to</td>
<td>0.26x</td>
</tr>
<tr>
<td>BTI $\Delta V_t$ increased to</td>
<td>1.30x</td>
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<tr>
<td>HCI $\Delta V_t$ increased to</td>
<td>1.36x</td>
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Conventional Aging and Self-Heating Modeling is Insufficient

**Auxiliary thermal network**

- **Performance and convergence**
  - One additional node (T) added for each MOSFET, and solved by SPICE
  - Device temperature is updated for every time point in simulation - expensive and prone to convergence issues

- **Lack of good aging models simulation solutions**
  - Lack of accurate and efficient aging models
  - Incompatible aging simulation solutions
Self-Heating and EM Analysis Integration

• The accuracy of EM rule depends heavily on wire temperatures (5-degree difference may result in ~30% difference)

• Having an uniform temperature for all wire is “convenient” but leads to over design

• Device self heating requires the capability of evaluating the wire temperatures locally

\[ -\Delta T_{METAL} = \Delta T_{joule} + \Delta T_{coupling} = \Delta T_{joule} + a \cdot b \cdot \Delta T_{od} \]
Parasitic RC in FinFET

- Many Rs and Cs
- Complicated to model and challenge to manage accuracy gap between pre-vs. post-layout

\[ R_{\text{total}} = R_{\text{intrinsic}} + R_{\text{ext}} + MEOL\_R \]

- Increasing parasitic RC impact on circuit characteristics

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Different Extraction Methods for Runtime and Accuracy Trade-off

- **Schematic**
  - VDD
  - SIG1 inside transistor model
  - SIG2
  - Parasitics inside model

- **Full RCC Extraction**
  - VDD
  - SIG1 inside transistor model
  - SIG2
  - Parasitics Extracted
  - No Parasitics

- **Signals RCC Power CC extraction**
  - VDD
  - SIG1 inside transistor model
  - SIG2
  - Double Counting Parasitics
Variability and PVT Corners

• Every thing increasing with geometry scaling down
  – FEOL issues, BEOL issues, # of operation Voltages, temperatures, …
Customization and Extension to BSIM-CMG

- Complex layout dependence (STI, WPE, OSE, PLE …)
- DFM rules
- Statistical and parametric variability
- Self heating effects
- Device aging effects
- Additional geometrical scaling – half node …

Foundry and Process specific. Difficult to be standardized into compact models
Synopsys Modeling Solutions for FinFET

- TSMC Modeling Interface (TMI)
- CustomCMI API (CMI)
- MOS Reliability Aging API (MOSRA)
- Efficient Subckt Macro Modeling

**TMI**: TSMC Modeling Interface  
**OMI**: CMC Modeling Interface
BSIM-CMG Performance Optimization

BSIMCMG Model Speedup

- Org. C code: 1
- Optimized C code: 2.04

BSIMCMG MT Scalability

- 1 CPU: 1
- 2 CPUs: 2
- 4 CPUs: 4
- 8 CPUs: 8

Number of CPUs
New Challenge on Compiled Model Validation

• Software engineering PURIFY sign off is a must for any compiled model release
  • TMI, OMI, CMI, …
• Conventional PURIFY check flow can not be applied

**Ideal PURIFY check flow**

A two-step TMI PURIFY check mechanism developed and deployed in TSMC for TMI production releases
Collaboration With Foundries on FinFET SPICE Library Sign Off

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<td>• Conductance (G)</td>
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<td>Model cards</td>
<td>• Capacitance (C)</td>
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- Accurate
- Scalable
- Robust
- SWE

OP/DC/TRAN
AC/Noise
Monte Carlo
HF/RF
MT

SPICE model validation and regression system established with eco-system partners
Summary

• SPICE model is the critical link between foundry and IC design

• FinFET requires more features into SPICE library
  – LDE, self heating, aging, variations …
  – Standard compact model is not enough and customization is required

• Synopsys provides comprehensive FinFET modeling solutions for performance, accuracy, and customization