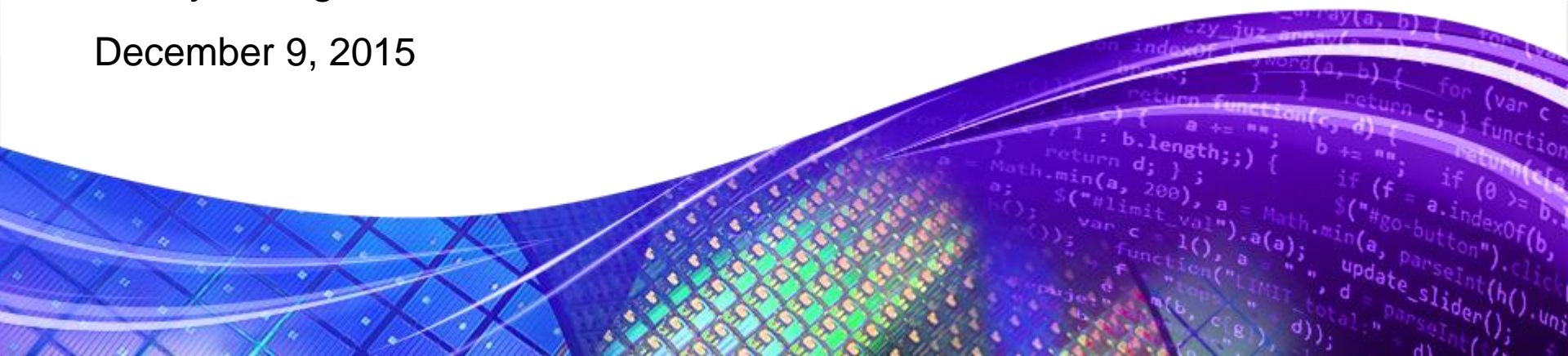


FinFET SPICE Modeling

Synopsys Solutions to Simulation Challenges of Advanced Technology Nodes

Joddy Wang

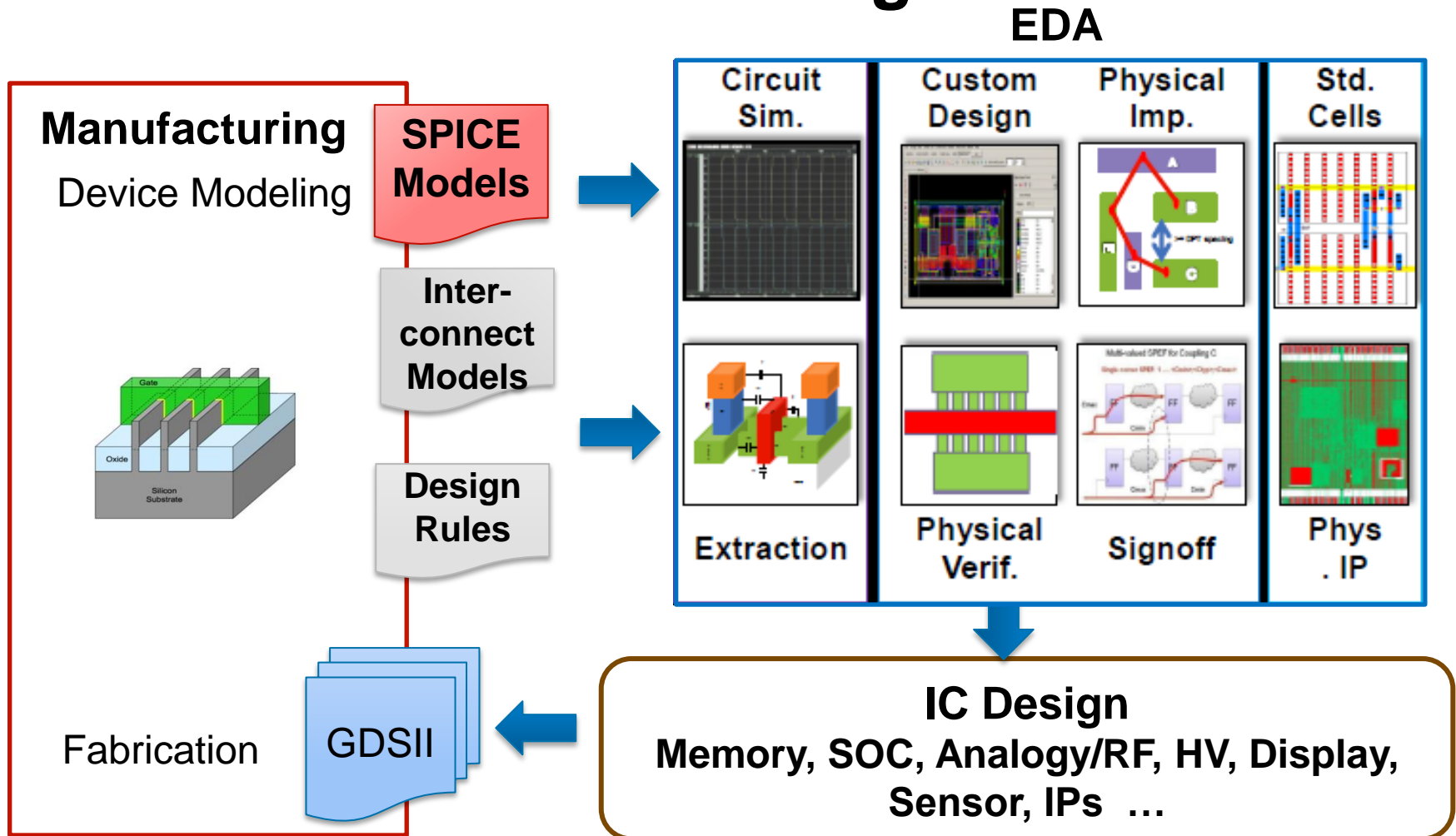
December 9, 2015



Outline

- SPICE Model for IC Design
- FinFET Modeling Challenges
- Solutions
- Summary

SPICE Models for IC Design

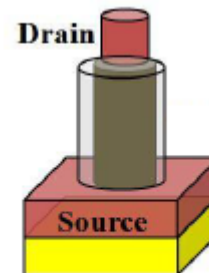
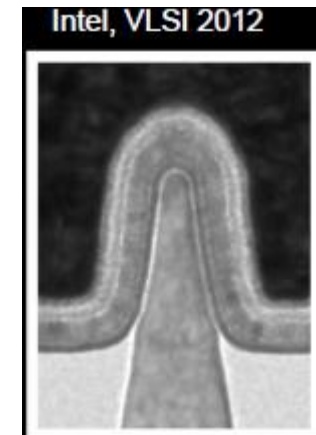
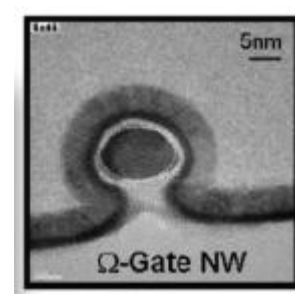
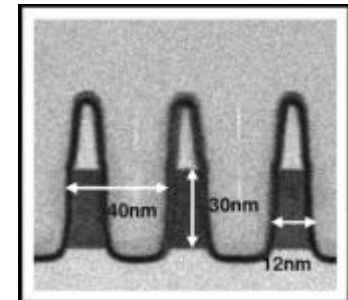
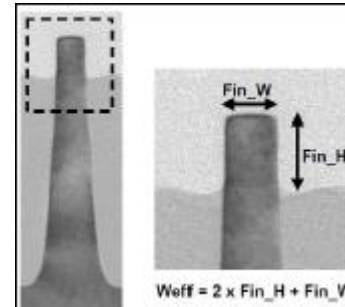


- The bridge between fabrication and IC design
- Key component of PDK

BSIM-CMG: Industry Standard Compact Model

- Various device structures
- Technology
 - Bulk and SOI
 - Channel materials: Si, SiGe, Ge, and InGaAs
- Production adoption for 16/14/10/7nm

Extension and customization are required



Vertical Pillar FET



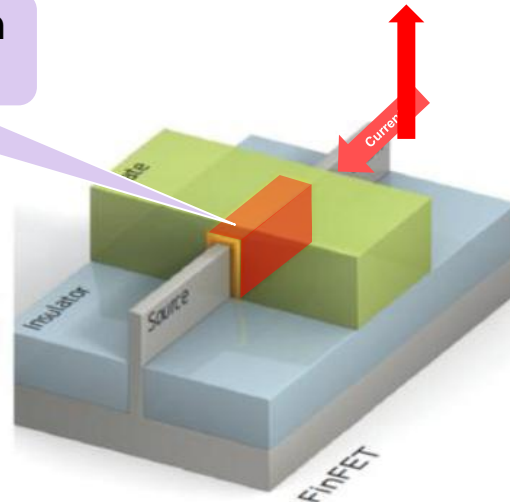
Horizontal Nanowire FET

Self Heating and MOS Reliability in FinFET

- FinFET has more pronounced self heating effect (SHE)
- Increased temperature exacerbates reliability degradation
 - Device aging effect:
BTI (Bias Temperature Instability) and HCI (Hot Carrier Injection)
- Concurrent SHE and reliability analysis

$$\Delta V_t \sim \exp(-n E_a / k_B T)$$

BTI & HCI degradation increased

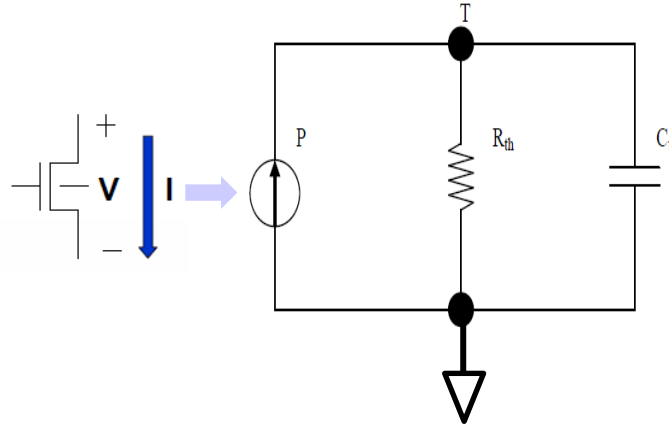


	$\Delta T = 20^\circ\text{C}$
EM I _{max} rule reduced to	0.26x
BTI ΔV_t increased to	1.30x
HCI ΔV_t increased to	1.36x

Aging simulation

Conventional Aging and Self-Heating Modeling is Insufficient

Auxiliary thermal network

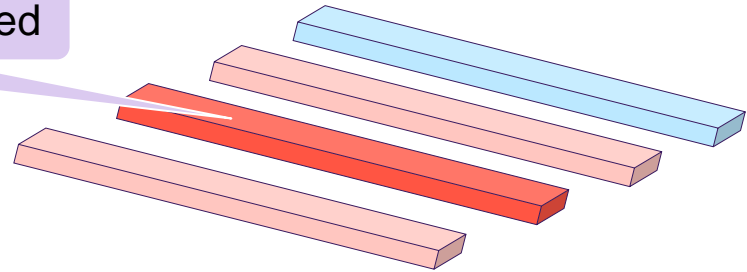


- Performance and convergence
 - One additional node (T) added for each MOSFET, and solved by SPICE
 - Device temperature is updated for every time point in simulation - expensive and prone to convergence issues
- Lack of good aging models simulation solutions
 - Lack of accurate and efficient aging models
 - Incompatible aging simulation solutions

Self-Heating and EM Analysis Integration

EM I_{max} (Maximum allowed I) reduced

$$I_{max} \sim \exp(E_a / k_B T)$$

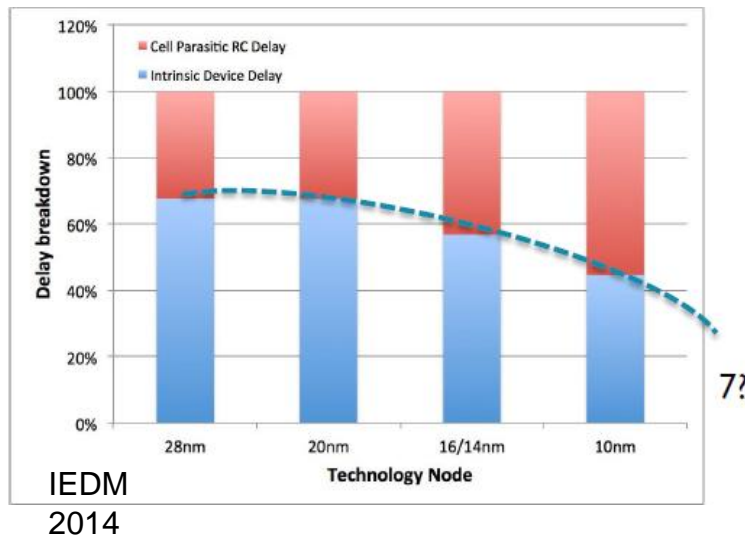
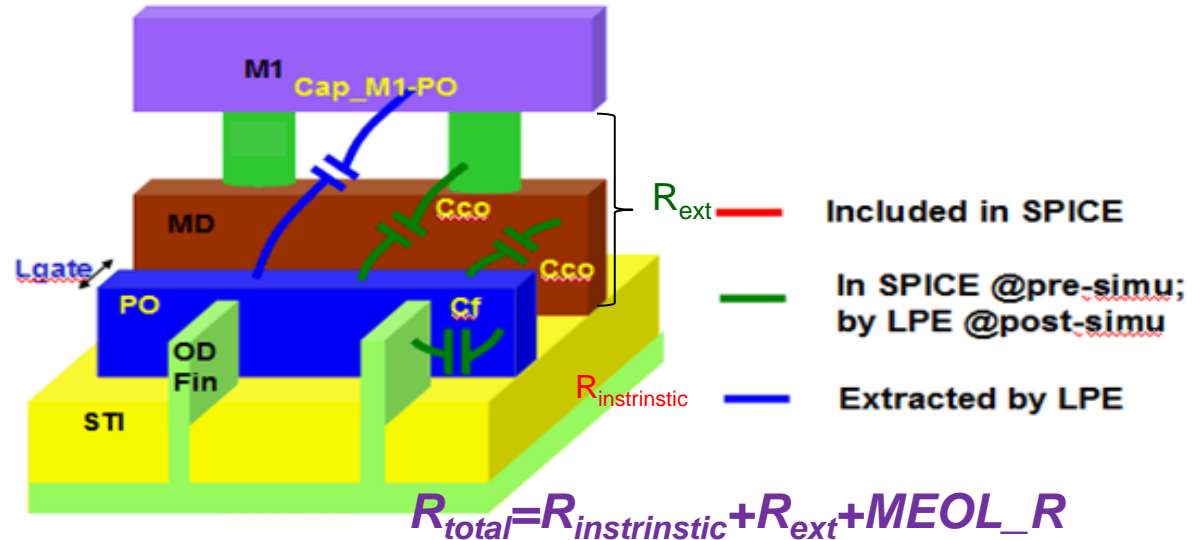


- The accuracy of EM rule depends heavily on wire temperatures (5-degree difference may result in ~30% difference)
- Having an uniform temperature for all wire is “convenient” but leads to over design
- Device self heating requires the capability of evaluating the wire temperatures locally

$$-\Delta T_{METAL} = \Delta T_{joule} + \Delta T_{coupling} = \Delta T_{joule} + a \cdot b \cdot \Delta T_{od}$$

Parasitic RC in FinFET

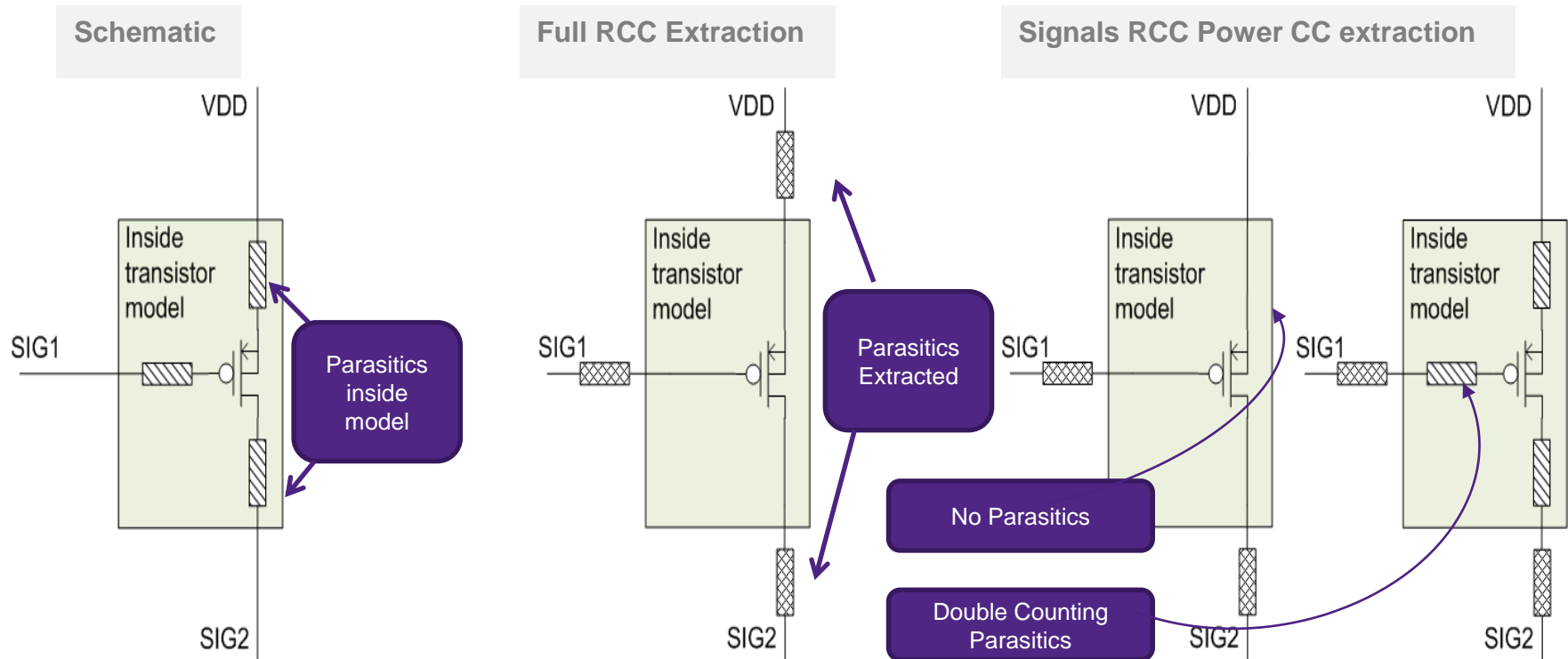
- Many Rs and Cs
- Complicated to model and challenge to manage accuracy gap between pre- vs. post- layout



- Increasing parasitic RC impact on circuit characteristics

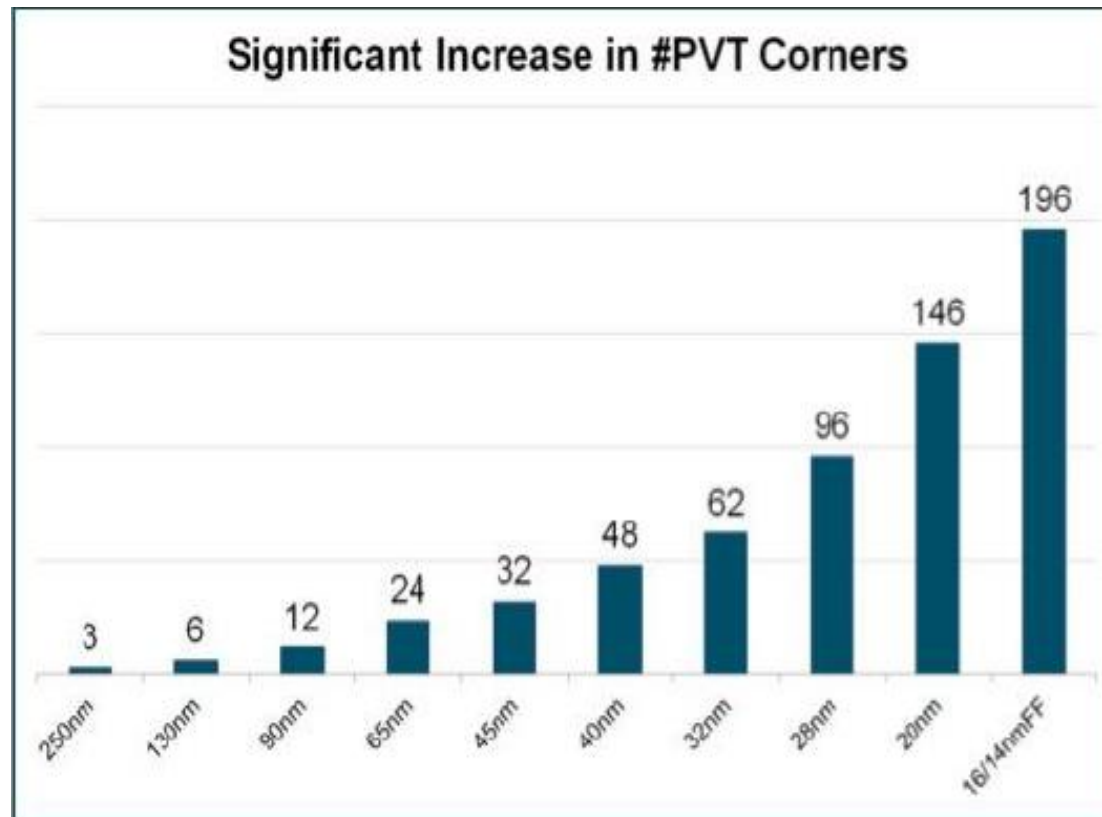
IEDM
2014

Different Extraction Methods for Runtime and Accuracy Trade-off



Variability and PVT Corners

- Every thing increasing with geometry scaling down
 - FEOL issues, BEOL issues, # of operation Voltages, temperatures, ...

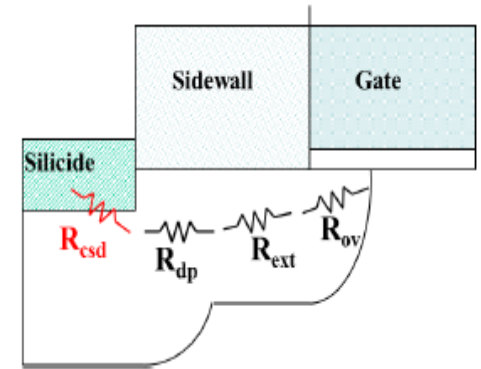
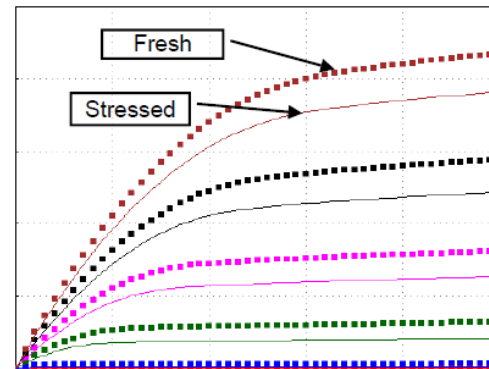
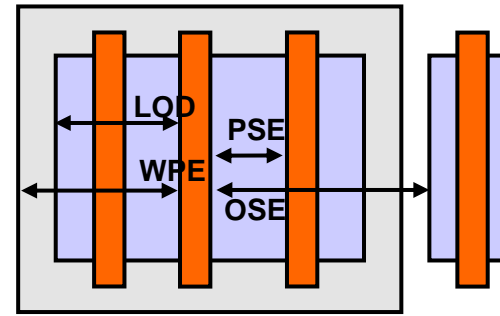


Daniel Payne, semiwiki

<https://www.semiwiki.com/forum/content/2814-spectre-cadence-goes-fastspice.html>

Customization and Extension to BSIM-CMG

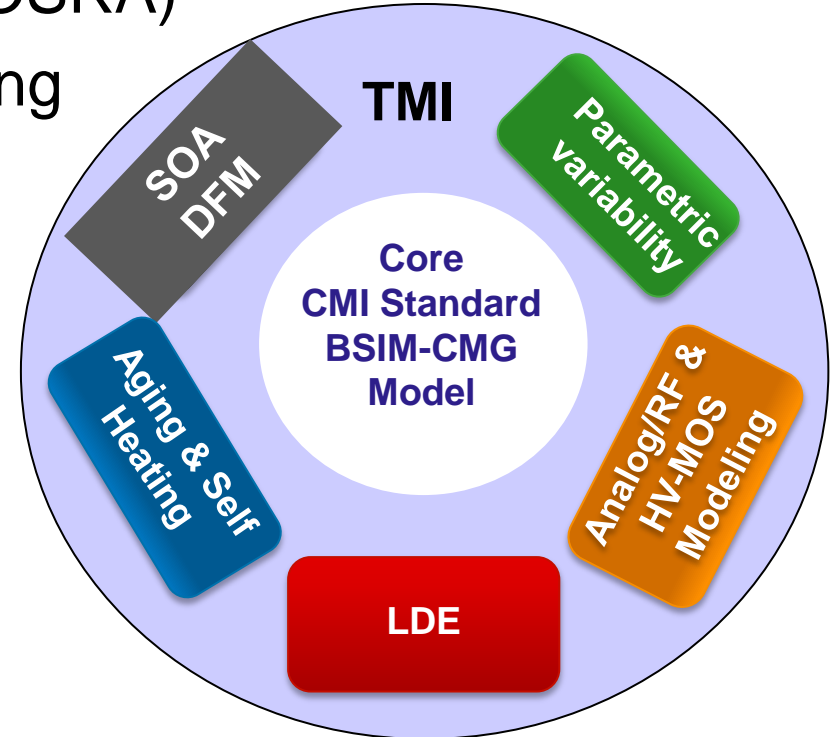
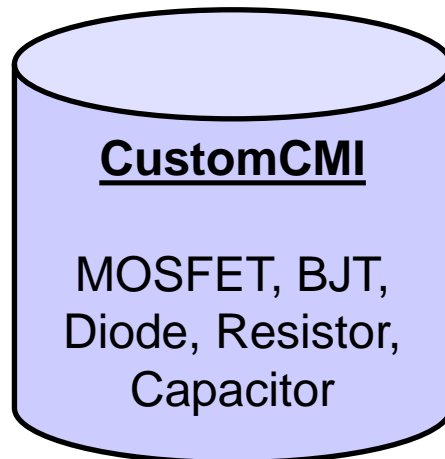
- Complex layout dependence (STI, WPE, OSE, PLE ...)
- DFM rules
- Statistical and parametric variability
- Self heating effects
- Device aging effects
- Additional geometrical scaling – half node ...



Foundry and Process specific. Difficult to be standardized into compact models

Synopsys Modeling Solutions for FinFET

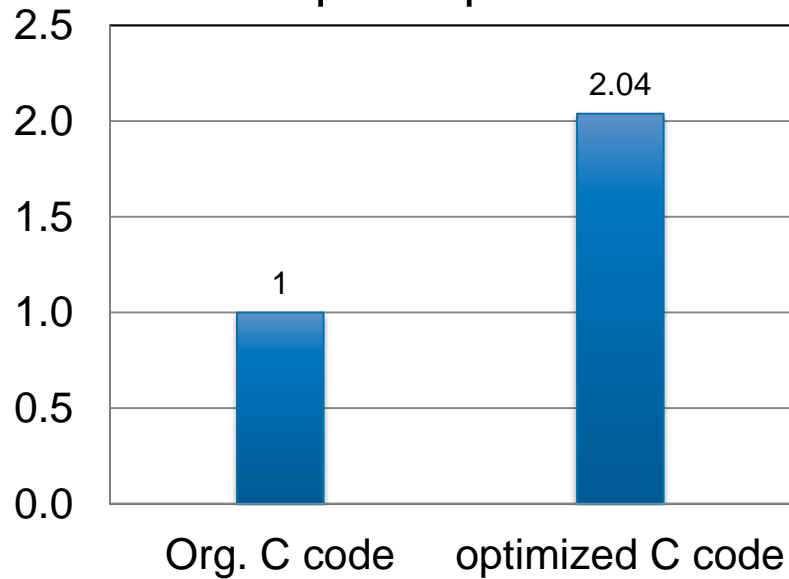
- TSMC Modeling Interface (TMI)
- CustomCMI API (CMI)
- MOS Reliability Aging API (MOSRA)
- Efficient Subckt Macro Modeling



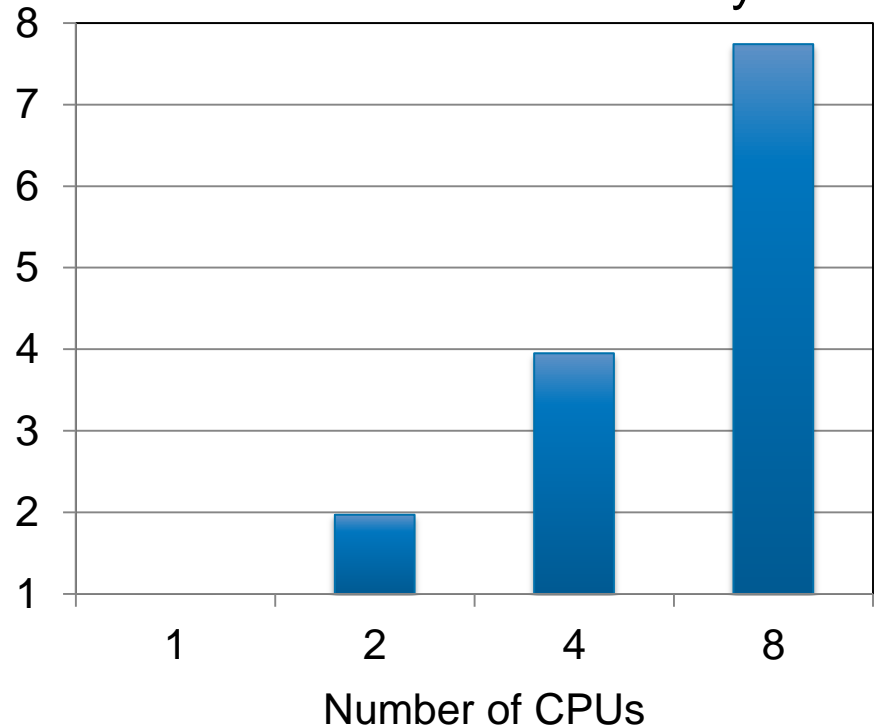
TMI: TSMC Modeling Interface
OMI: CMC Modeling Interface

BSIM-CMG Performance Optimization

BSIMCMG Model Speedup



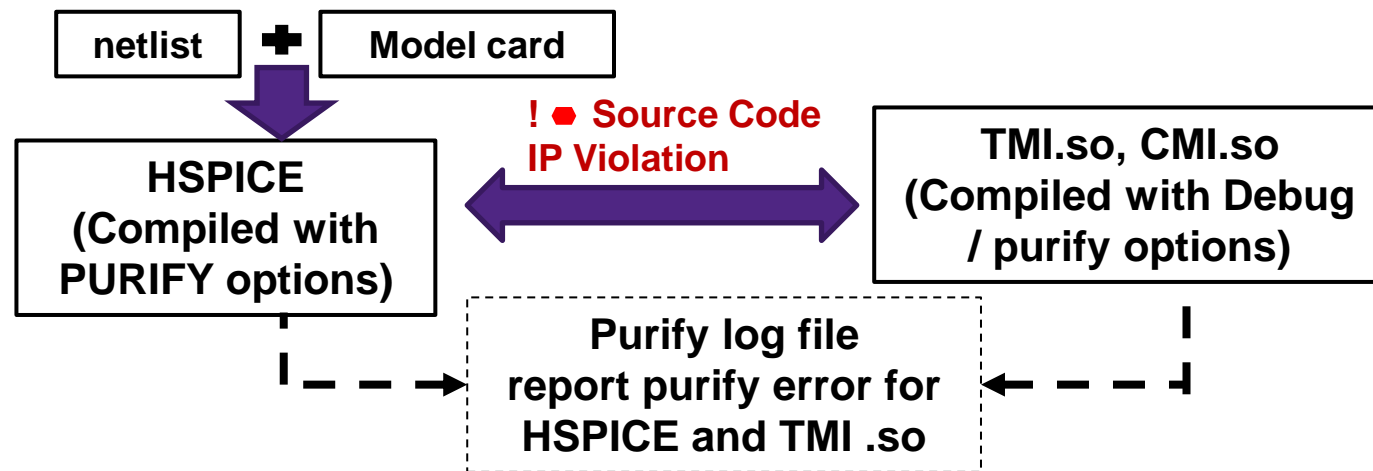
BSIMCMG MT Scalability



New Challenge on Compiled Model Validation

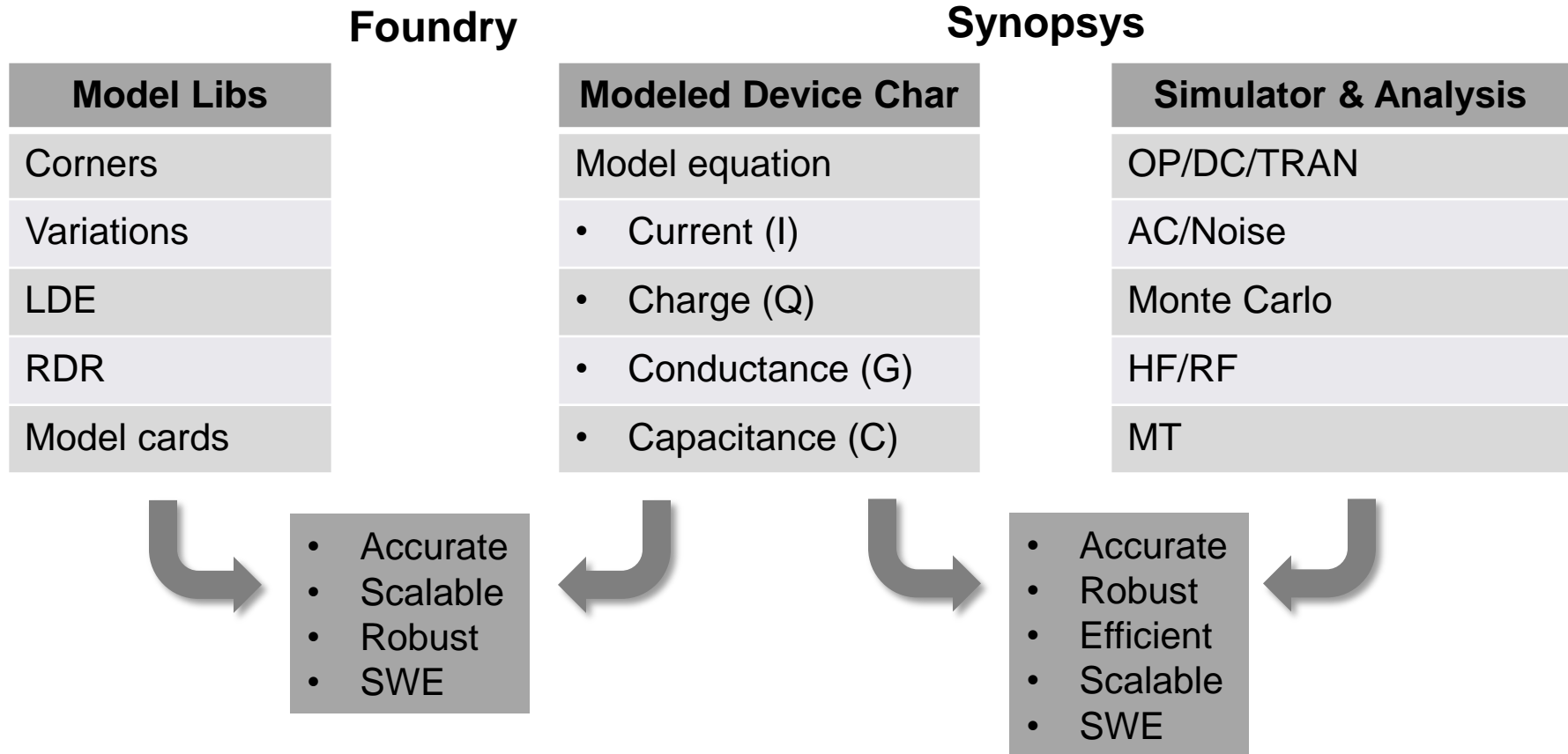
- Software engineering PURIFY sign off is a must for any compiled model release
 - TMI, OMI, CMI, ...
- Conventional PURIFY check flow can not be applied

Ideal PURIFY check flow



A two-step TMI PURIFY check mechanism developed and deployed in TSMC for TMI production releases

Collaboration With Foundries on FinFET SPICE Library Sign Off



SPICE model validation and regression system established with eco-system partners

Summary

- SPICE model is the critical link between foundry and IC design
- FinFET requires more features into SPICE library
 - LDE, self heating, aging, variations ...
 - Standard compact model is not enough and customization is required
- Synopsys provides comprehensive FinFET modeling solutions for performance, accuracy, and customization