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Silicon to Software™

FinFET SPICE Modeling

Synopsys Solutions to Simulation Challenges of Advanced Technology Nodes

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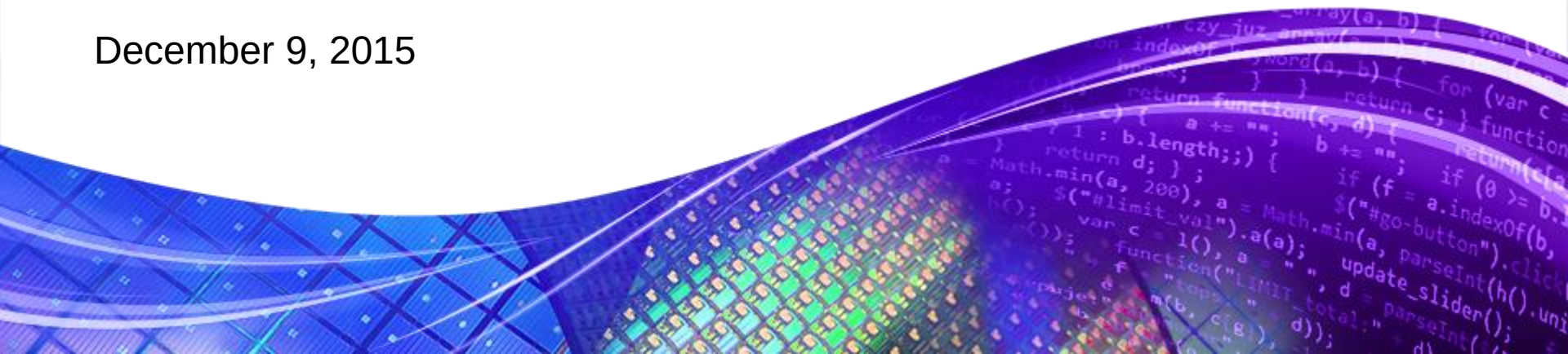
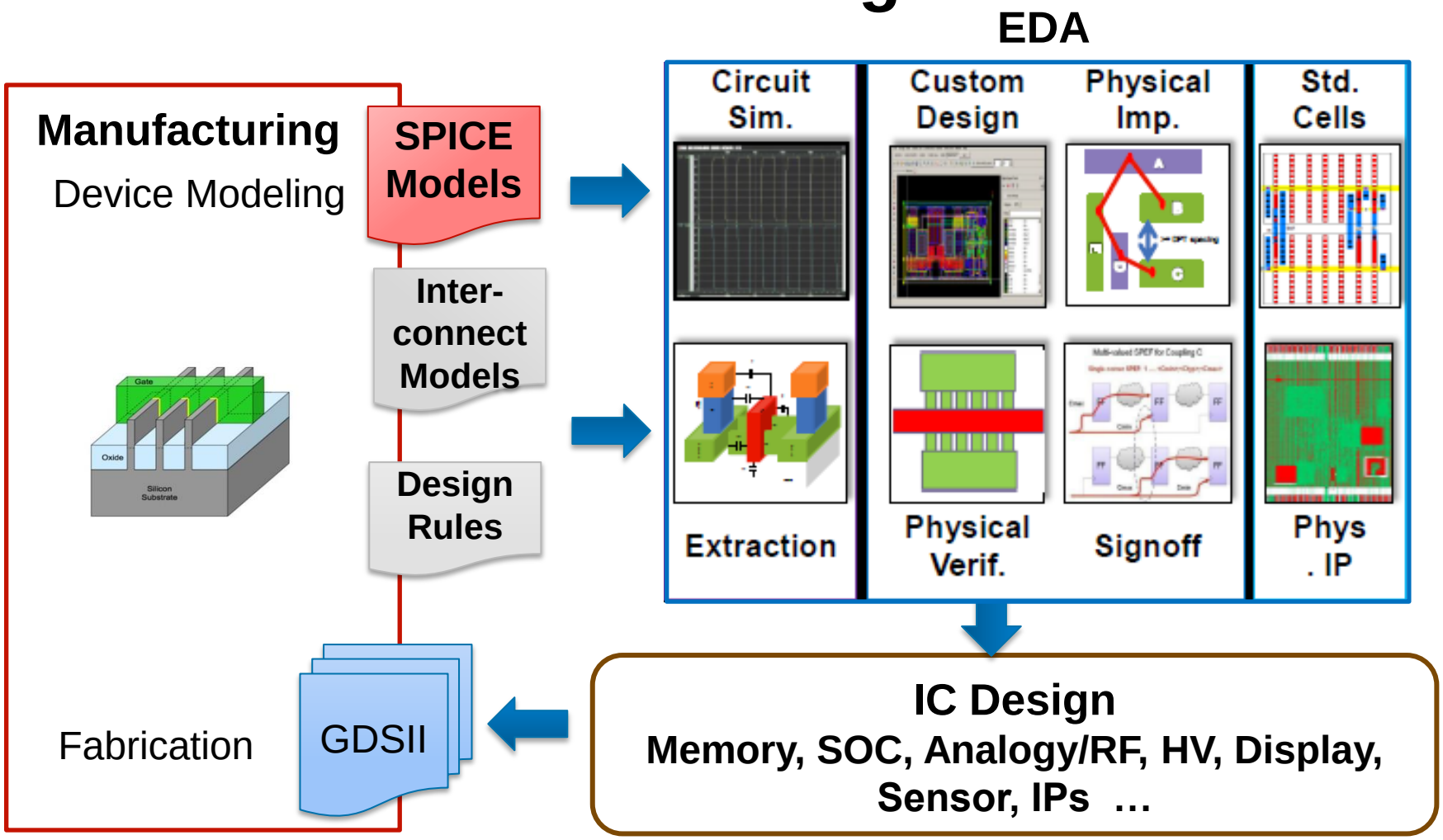
December 9, 2015



Outline

- SPICE Model for IC Design
- FinFET Modeling Challenges
- Solutions
- Summary

SPICE Models for IC Design



- The bridge between fabrication and IC design
- Key component of PDK

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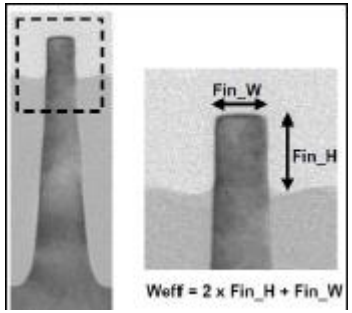
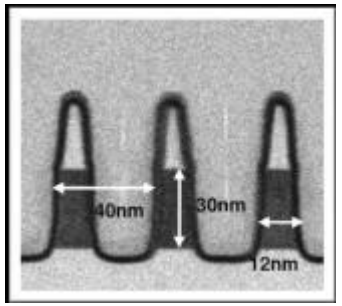
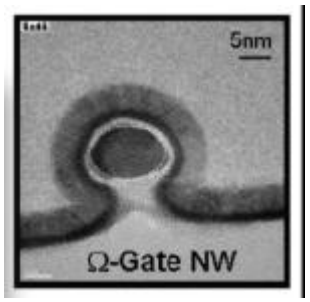
BSIM-CMG: Industry Standard Compact Model

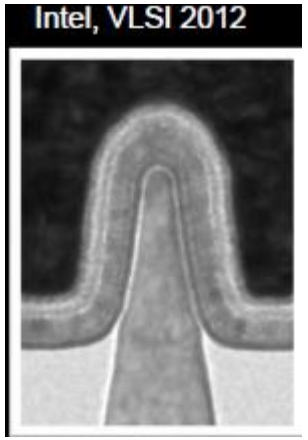
- Various device structures
- Technology
  - Bulk and SOI
  - Channel materials: Si, SiGe, Ge, and InGaAs
- Production adoption for 16/14/10/7nm

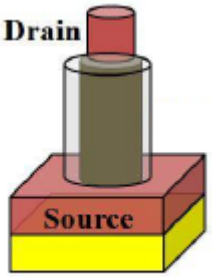
Extension and customization are required











Vertical Pillar FET

Horizontal Nanowire FET

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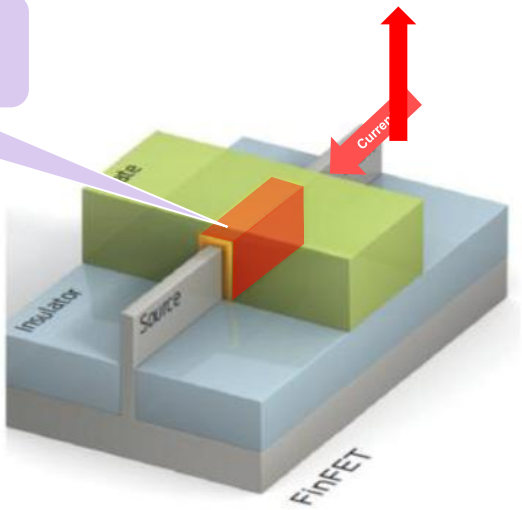
Self Heating and MOS Reliability in FinFET

- FinFET has more pronounced self heating effect (SHE)
- Increased temperature exacerbates reliability degradation
  - Device aging effect:
    BTI (Bias Temperature Instability) and HCI (Hot Carrier Injection)
- Concurrent SHE and reliability analysis

$$\Delta Vt \sim \exp(-n\,E_a / k_B T)$$

BTI & HCI degradation increased



	ΔT = 20°C
EM Imax rule reduced to	0.26x
BTI ΔVt increased to	1.30x
HCI ΔVt increased to	1.36x

Aging simulation

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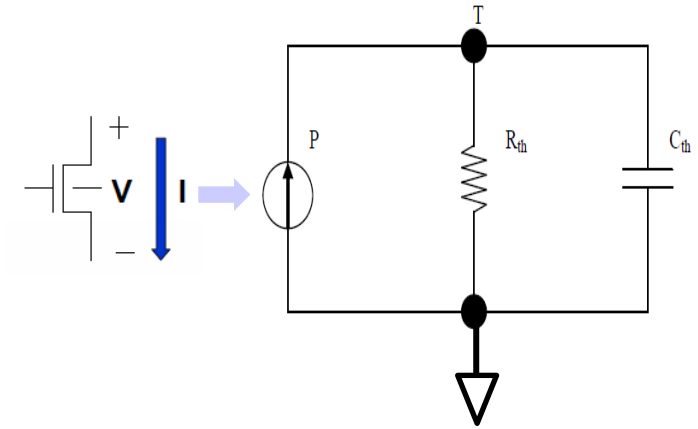
Conventional Aging and Self-Heating Modeling is Insufficient

Auxiliary thermal network



- Performance and convergence
  - One additional node (T) added for each MOSFET, and solved by SPICE
  - Device temperature is updated for every time point in simulation - expensive and prone to convergence issues
- Lack of good aging models simulation solutions
  - Lack of accurate and efficient aging models
  - Incompatible aging simulation solutions

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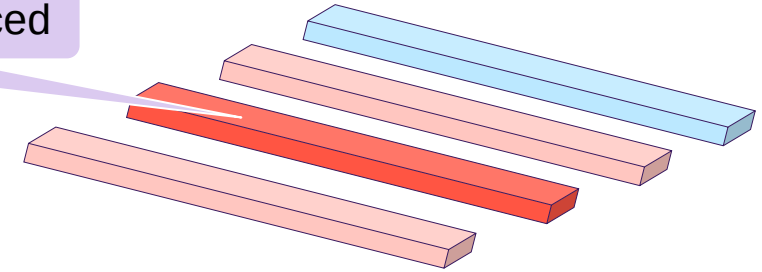
Self-Heating and EM Analysis Integration

EM Imax (Maximum allowed I) reduced

$$I_{max} \sim \exp(E_a / k_B T)$$

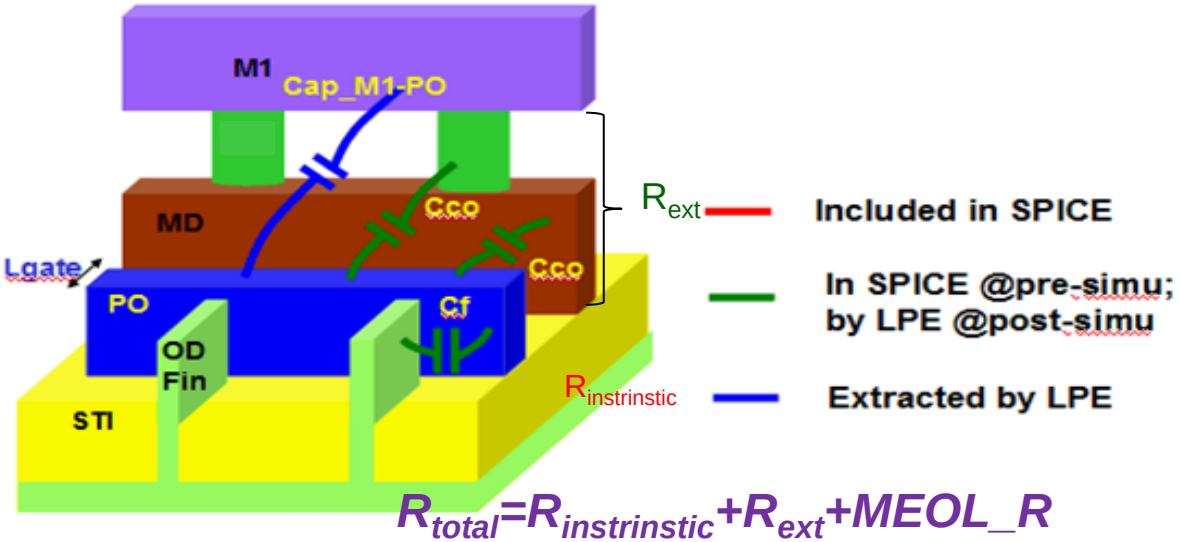


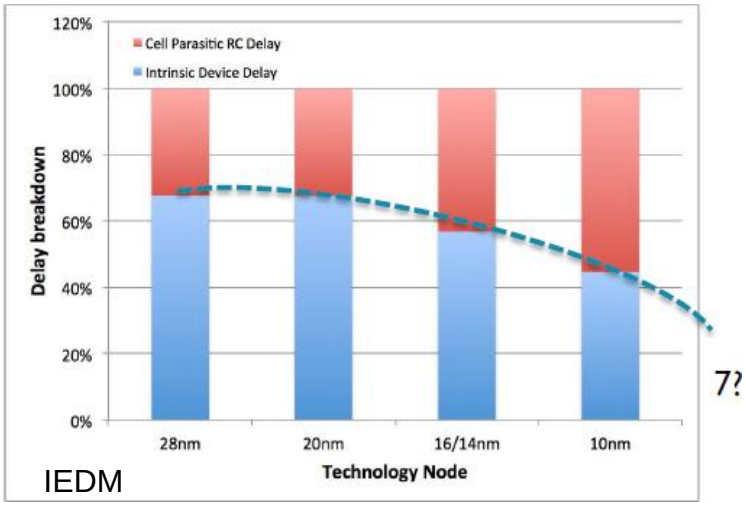
- The accuracy of EM rule depends heavily on wire temperatures (5-degree difference may result in ~30% difference)
- Having an uniform temperature for all wire is “convenient” but leads to over design
- Device self heating requires the capability of evaluating the wire temperatures locally

$$-\Delta T_{METAL} = \Delta T_{joule} + \Delta T_{coupling} = \Delta T_{joule} + a \cdot b \cdot \Delta T_{od}$$

Parasitic RC in FinFET

- Many Rs and Cs
- Complicated to model and challenge to manage accuracy gap between pre- vs. post- layout





IEDM 2014

- Increasing parasitic RC impact on circuit characteristics

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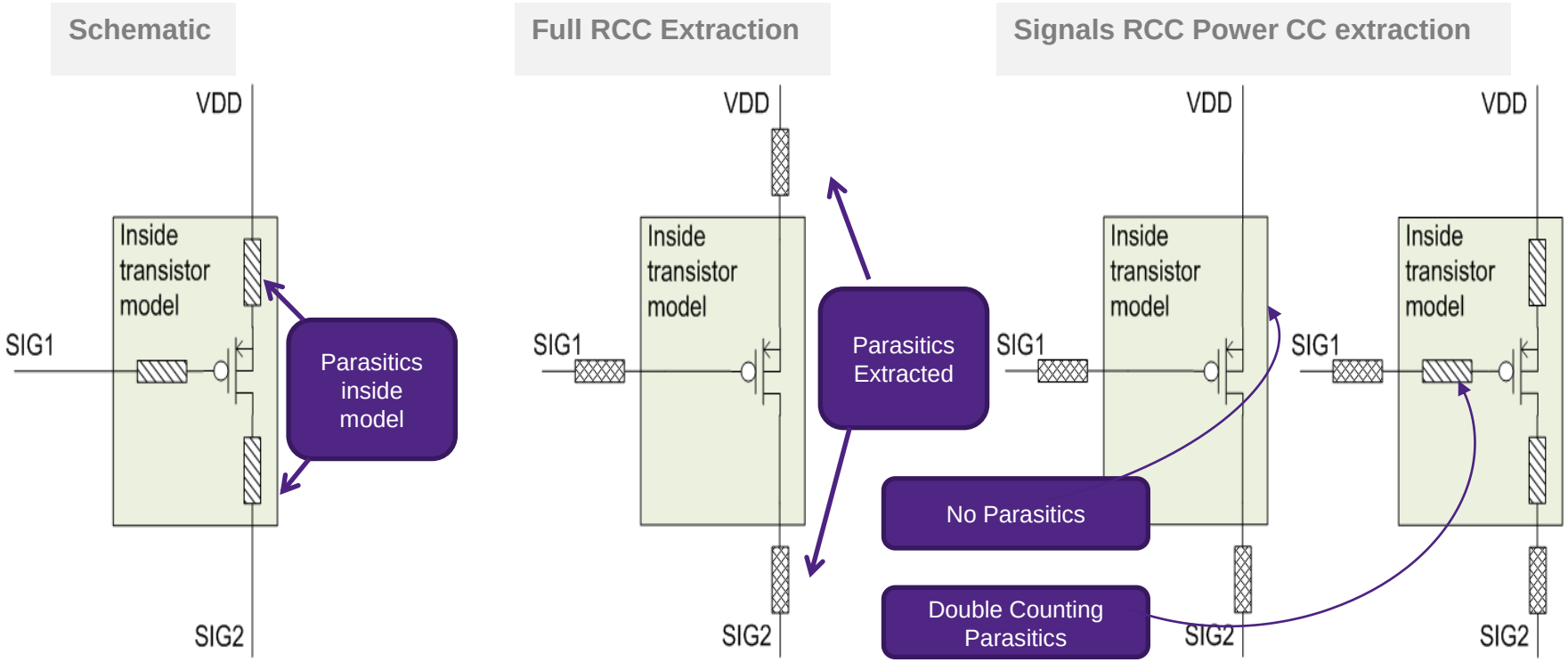
Different Extraction Methods for Runtime and Accuracy Trade-off



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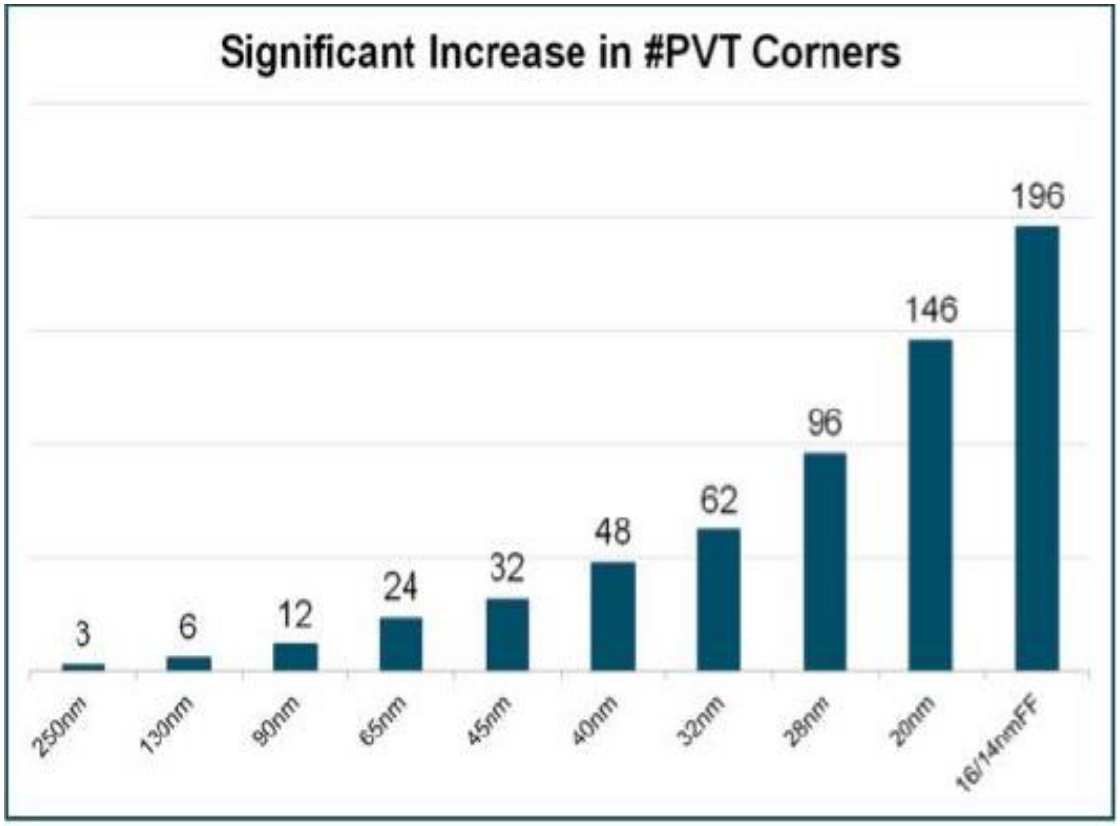
Variability and PVT Corners

- Every thing increasing with geometry scaling down
  - FEOL issues, BEOL issues, # of operation Voltages, temperatures, …



Daniel Payne, semiwiki
https://www.semiwiki.com/forum/content/2814-spectre-cadence-goes-fastspice.html

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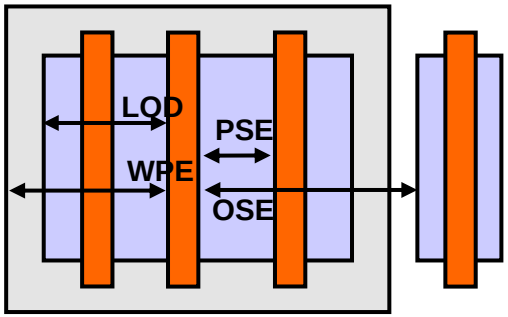
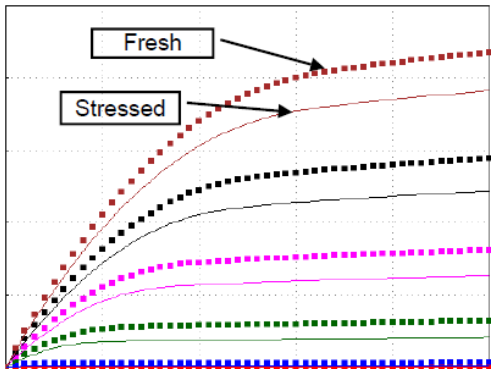
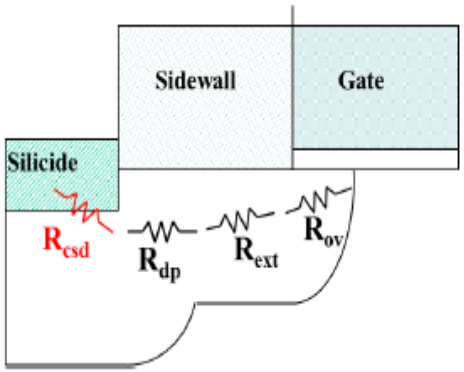
Customization and Extension to BSIM-CMG

- Complex layout dependence (STI, WPE, OSE, PLE …)
- DFM rules
- Statistical and parametric variability
- Self heating effects
- Device aging effects
- Additional geometrical scaling – half node …







Foundry and Process specific. Difficult to be standardized into compact models

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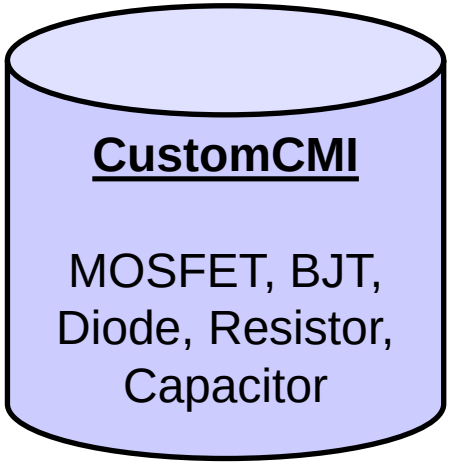
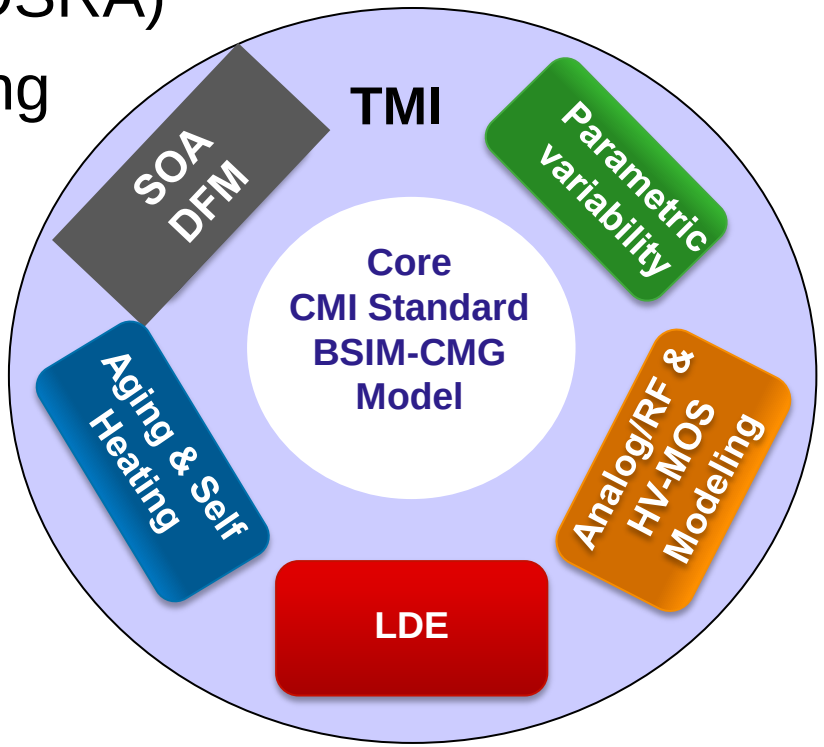
Synopsys Modeling Solutions for FinFET

- TSMC Modeling Interface (TMI)
- CustomCMI API (CMI)
- MOS Reliability Aging API (MOSRA)
- Efficient Subckt Macro Modeling





TMI: TSMC Modeling Interface
OMI: CMC Modeling Interface

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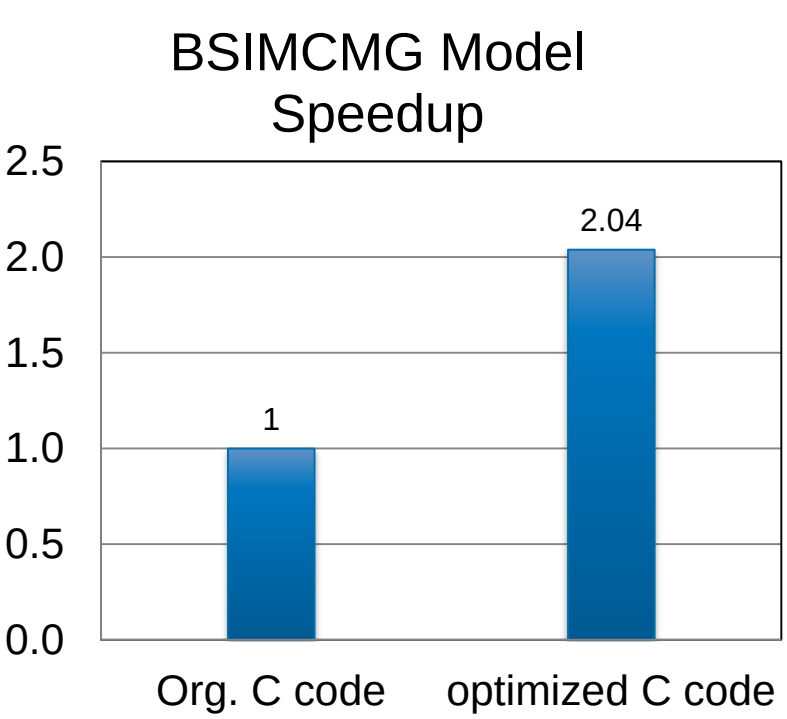
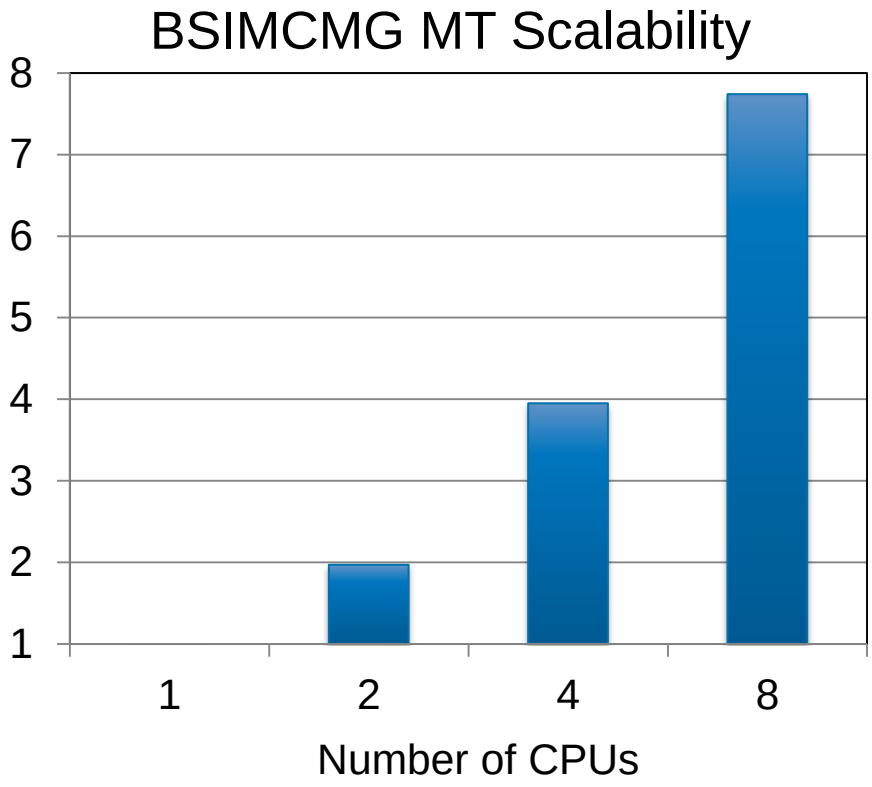
BSIM-CMG Performance Optimization





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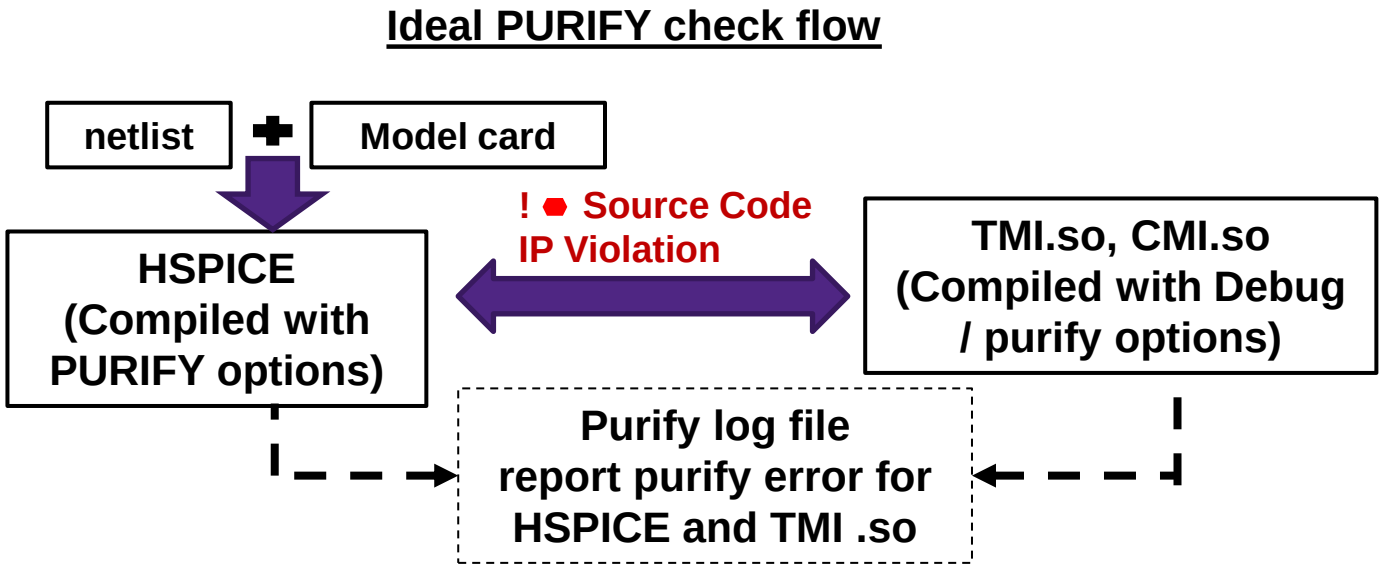
New Challenge on Compiled Model Validation

- Software engineering PURIFY sign off is a must for any compiled model release
  - TMI, OMI, CMI, …
- Conventional PURIFY check flow can not be applied



A two-step TMI PURIFY check mechanism developed and deployed in TSMC for TMI production releases

Collaboration With Foundries on FinFET SPICE Library Sign Off

Foundry

Model Libs
Corners
Variations
LDE
RDR
Model cards

- Accurate
- Scalable
- Robust
- SWE

Synopsys

Modeled Device Char
Model equation
• Current (I)
• Charge (Q)
• Conductance (G)
• Capacitance (C)

Simulator & Analysis
OP/DC/TRAN
AC/Noise
Monte Carlo
HF/RF
MT

- Accurate
- Robust
- Efficient
- Scalable
- SWE

SPICE model validation and regression system established with eco-system partners

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Summary

- SPICE model is the critical link between foundry and IC design

- FinFET requires more features into SPICE library
  - LDE, self heating, aging, variations …
  - Standard compact model is not enough and customization is required

- Synopsys provides comprehensive FinFET modeling solutions for performance, accuracy, and customization

