ANALYTICAL SOI MOSFET MODEL VALID FOR GRADED-CHANNEL DEVICES

Benjamín Iñíguez[1] , Marcelo Antonio Pavanello[2,3], João Antonio Martino[3] and Denis Flandre[4]

[3]Escola Tècnica Superior d`Engenyeria
Universitat Rovira I Virgili, Tarragona, Spain

[2]Center for Semiconductor Components
State University of Campinas, Campinas, Brazil

[3]Laboratório de Sistemas Integráveis
Escola Politécnica da Universidade de São Paulo

[4]Laboratoire de Microéletronique
Université Catholique de Louvain, Louvain-la-Neuve, Belgium

Outline:

- Introduction
- Analytical Model Formulation
- Results and Discussion
- Fabrication Process and Experimental Results
- Conclusion

The advantages of Fully-depleted SOI nMOSFETs over Partially-Depleted (PD) and bulk MOSFETs are well known

1) Lower subthreshold ideality factor
2) Reduced short-channel effects
3) Better analog performance
4) Better microwave performance (gain, speed and cutoff frequency)
5) Lower 1/f and thermal noise

As a consequence, FD SOI MOSFET is a very good candidate for low-power and low-noise microwave circuits

However, Fully-Depleted SOI nMOSFETs suffer from some Parasitic Bipolar Effects due to the Floating Body

Premature Drain Breakdown

Parasitic Bipolar Transistor Action:

- Emitter – Source
- Base – Body (floating)
- Collector – Drain

Some of the proposed solutions:

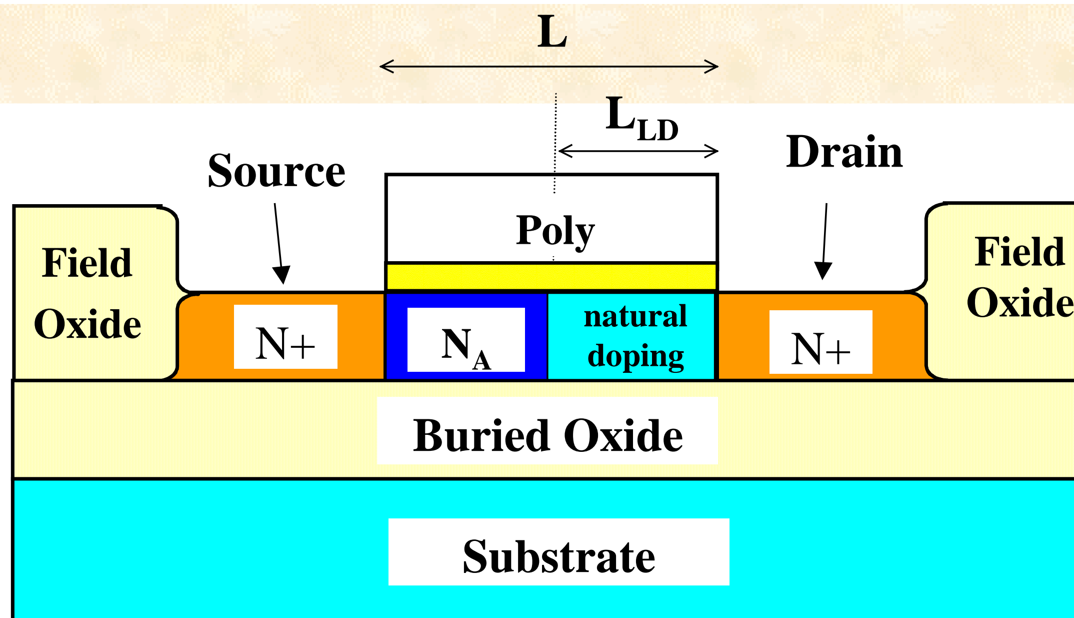
➔ Bandgap Engineering (Ge implanted) [M. Yoshimi et al., IEDM 94, p. 429]

➔ Source-Body Contact [IEDM 94, p. 657]

➔ Asymmetric Channel Profile using tilt implantation [B. Cheng et al., IEEE Int. SOI Conference, p. 113, 1998]

⇒ THE GRADED-CHANNEL (GC) SOI nMOSFET

- FD SOI CMOS technology fully compatible processing
- One photolitographic step is used to adjust the threshold voltage ionic implantation position
- This photolithographic step is the same used to mask the p-type transistor
NO additional photolithographic step has to be included in the CMOS processing.
- The effective channel length is about $L\text{-}L_{LD}$



Reported results indicate:

Increase in the breakdown voltage

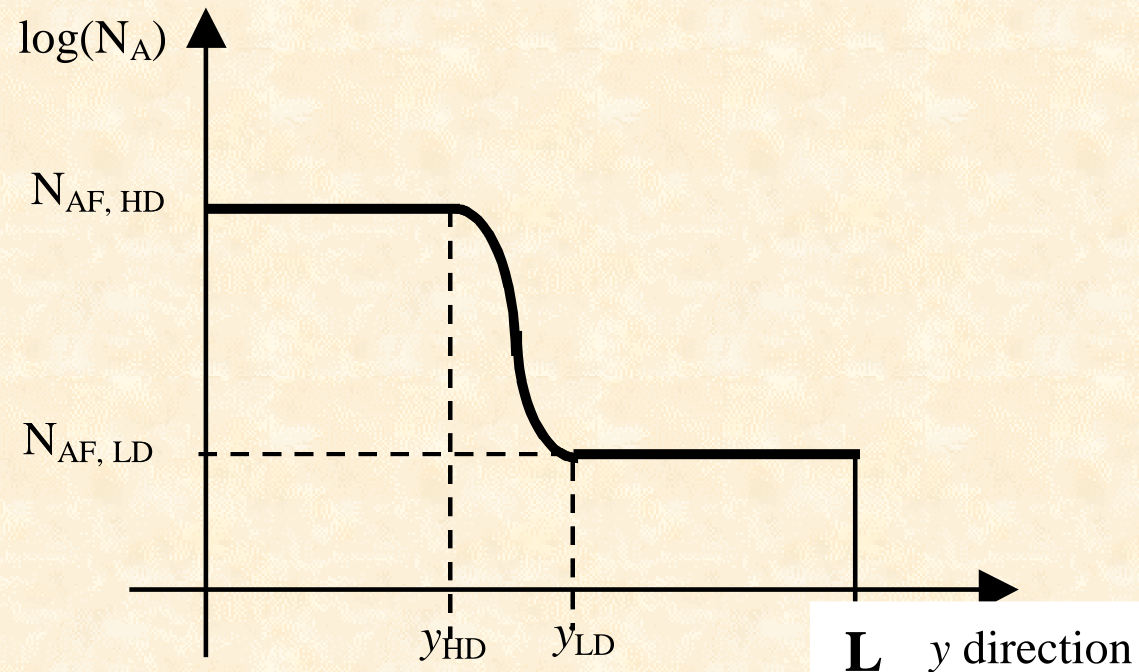
Tremendous reduction in the drain output conductance

Increase in the transconductance

The Graded-Channel SOI MOSFET is a great candidate for analog circuits resulting in improved amplifiers and current mirrors

Our goal: Development of a continuos model for GC transistor to allow reliable simulation of analog circuits

Schematic doping profile along channel



In the interval $y_{HD} \leq y \leq y_{LD}$

$$N_A = N_{AF,HD} \exp\left[\frac{-(y - y_{HD})^2}{2 10^{-4}}\right]$$

Based on physical principles, an analytical FD SOI MOSFET model was developed by B. Iñiguez et al.

For a conventional fully-depleted SOI nMOSFET:

$$I_{DS} = -W\mu\left(Q_{nf}\frac{d\phi_{sf}}{dy} - v_T\frac{dQ_{nf}}{dy} \right)$$

There is a linear relation between the surface potential, ϕ_{sf}, and the inversion charge density, Q_{nf}:

$$Q_{nf} = -C_{oxf}\left(V_{GF} - V_{FBf} - \frac{Q_b}{2C_{oxf}} - \frac{C_{bb}}{C_{oxf}}\left(V_{GB} - V_{FBb} + \frac{Q_b}{2C_{oxb}} \right) - n\phi_{SF} \right)$$

Integrating the inversion charges along channel results:

$$I_{DS} = \frac{\mu W}{L}\left[v_T\left(Q_{nf,D} - Q_{nf,S}\right) - \frac{Q_{nf,D}^{\;2} - Q_{nf,S}^{\;2}}{2\,n\,C_{oxf}}\right]$$

$Q_{nf,D}$ and $Q_{nf,S}$ are the inversion charge densities at the drain and source, respectively

An explicit and unified expression for Q_{nf} is used in the I_{DS} equation (proposed by Iñiguez *et al*): .

$$Q_{nf} = -C_{oxf}\,n v_T S_{NT}\,\log\left[1 + \frac{-Q_0 / C_{oxf}}{n\,v_T\,S_{NT}}\exp\left(\frac{V_{GF} - Vth_{Fi} - nV(y)}{n\,v_T}\right) + \exp\left(\frac{V_{GF} - Vth_F - nV(y)}{n\,v_T\,S_{NT}}\right)\right]$$

This model is continuous, valid from weak to strong inversion regimes

These physical principles allow to develop a complete CAD model and to adapt it to many conditions

1- Short-channel effects included

DIBL and charge sharing

Velocity saturation

Channel length modulation

2- Complete charge model

3- Scalability down to 0.16 µm

4- Temperature dependencies included. Model validated up to 300 ^{o}C :

5-Macro-model developed to extend the model to the microwave range. Accuracy demonstrated up to 40 GHz..

For long-channel transistors, the transition region into the channel (from $y_{HD} \leq y \leq y_{LD}$) can be considered negligible:

With this assumption, there will be two explicit equations for the inversion charges in the low doped ($Q_{nf,\,LD}$) and conventionally doped ($Q_{nf,\,HD}$) parts of the channel

$$Q_{nf,LD} = -C_{oxf}\, n v_T S_{NT} \log\left[1 + \frac{-Q_{0,LD}/C_{oxf}}{n\, v_T\, S_{NT}} \exp\left(\frac{V_{GF} - Vth_{Fi,LD} - nV(y)}{n\, v_T}\right) + \exp\left(\frac{V_{GF} - Vth_{F,LD} - nV(y)}{n\, v_T\, S_{NT}}\right)\right]$$

$$Q_{nf,HD} = -C_{oxf}\, n v_T S_{NT} \log\left[1 + \frac{-Q_{0,HD}/C_{oxf}}{n\, v_T\, S_{NT}} \exp\left(\frac{V_{GF} - Vth_{Fi,HD} - nV(y)}{n\, v_T}\right) + \exp\left(\frac{V_{GF} - Vth_{F,HD} - nV(y)}{n\, v_T\, S_{NT}}\right)\right]$$

V(y) is the potential variation along channel

Integrating the inversion charges along channel results:

$$I_{DS} = -\mu_{HD} W \left[\int_{0}^{L-L_{LD}} \frac{Q_{nf,HD}}{n\,C_{oxf}} \frac{dQ_{nf,HD}}{dy} - v_T \frac{dQ_{nf,HD}}{dy} \right] = -\mu_{LD} W \left[\int_{L-L_{LD}}^{L} \frac{Q_{nf,LD}}{n\,C_{oxf}} \frac{dQ_{nf,LD}}{dy} - v_T \frac{dQ_{nf,LD}}{dy} \right]$$

$$I_{DS} = \frac{\mu_{HD} W}{L - L_{LD}} \left[v_T \left(Q_{nf,HD_{L-L_{LD}}} - Q_{nf,HD_0} \right) - \frac{Q_{nf,HD_{L-L_{LD}}}^{\;2} - Q_{nf,HD_0}^{\;2}}{2\,n\,C_{oxf}} \right]$$

$$I_{DS} = \frac{\mu_{LD} W}{L_{LD}} \left[v_T \left(Q_{nf,LD_L} - Q_{nf,LD_{L-L_{LD}}} \right) - \frac{Q_{nf,LD_L}^{\;2} - Q_{nf,LD_{L-L_{LD}}}^{\;2}}{2\,n\,C_{oxf}} \right]$$

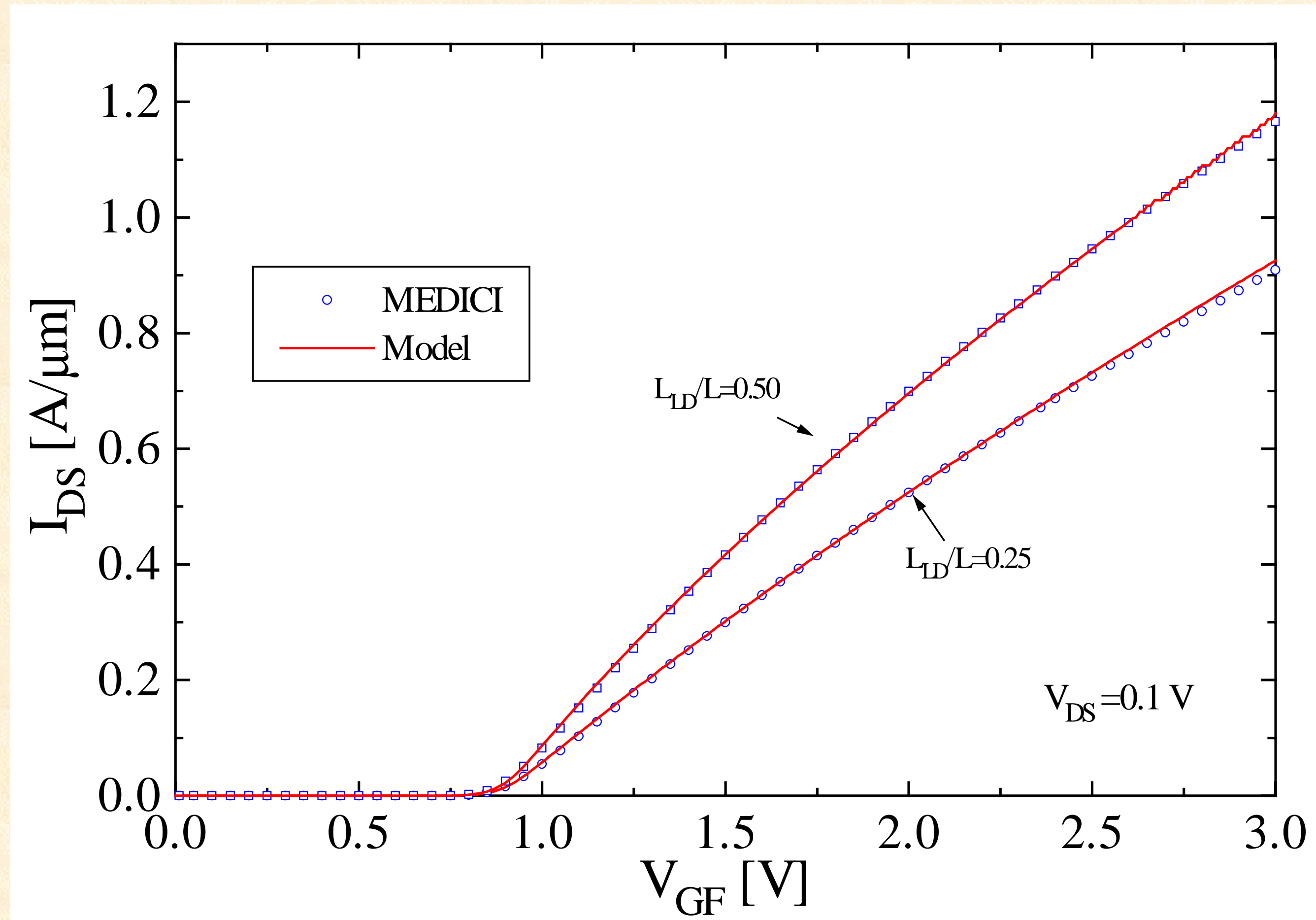
The GC SOI nMOSFET is therefore interpreted as a series association of two conventional transistors, each one representing a part of the channel region

Comparison between MEDICI numerical two-dimensional simulations and model equations solution

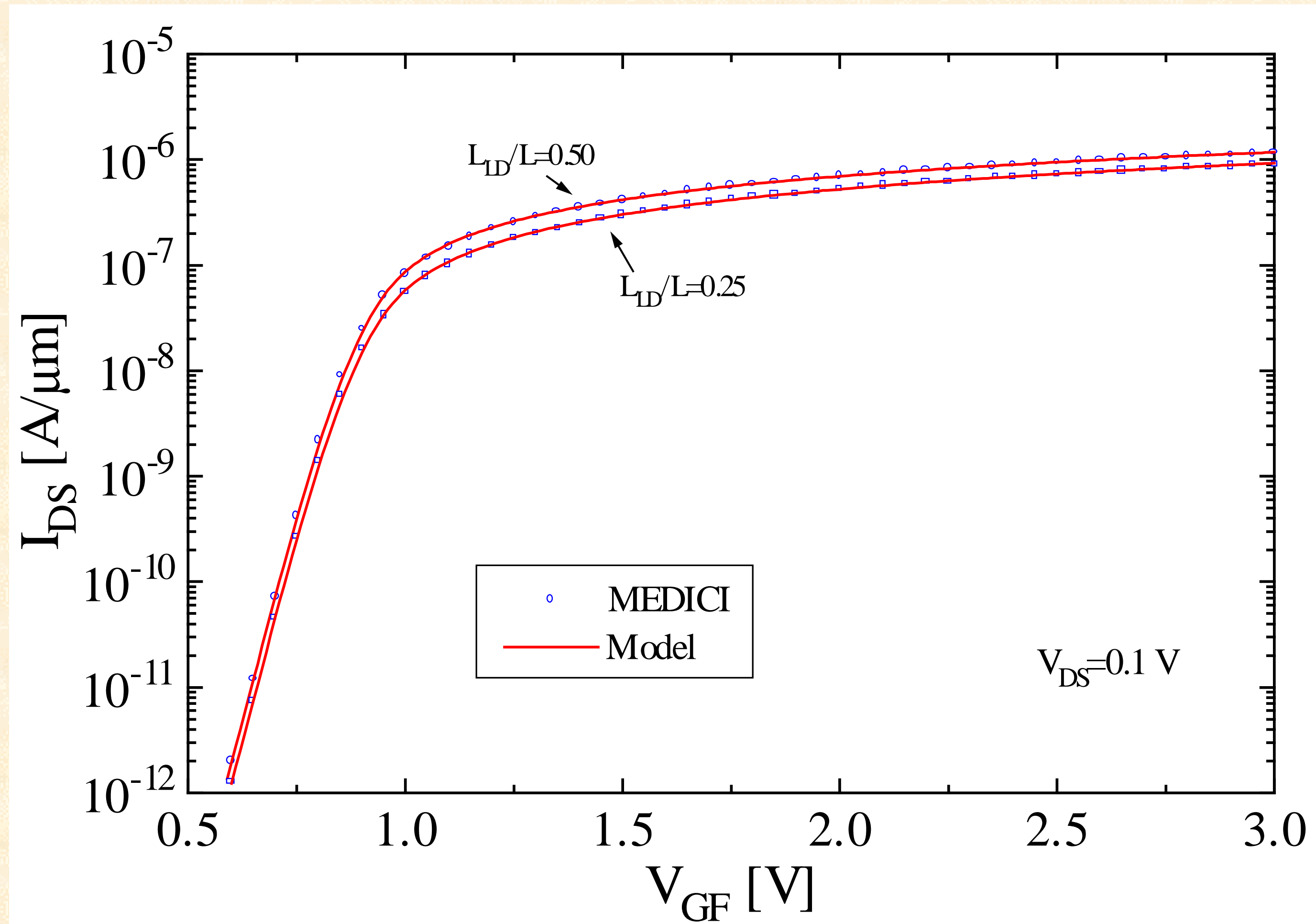
Device characteristics:

t_{oxf}=30 nm, t_{Si}=80 nm, t_{oxb}=400 nm, $Q_{ox1}/q = Q_{ox2}/q = 5 \times 10^{10}$ cm^{-2}, $N_{AF,\ HD} = 10^{17}$ cm^{-3} and $N_{AF,\ LD} = 10^{15}$ cm^{-3}. L=10 µm

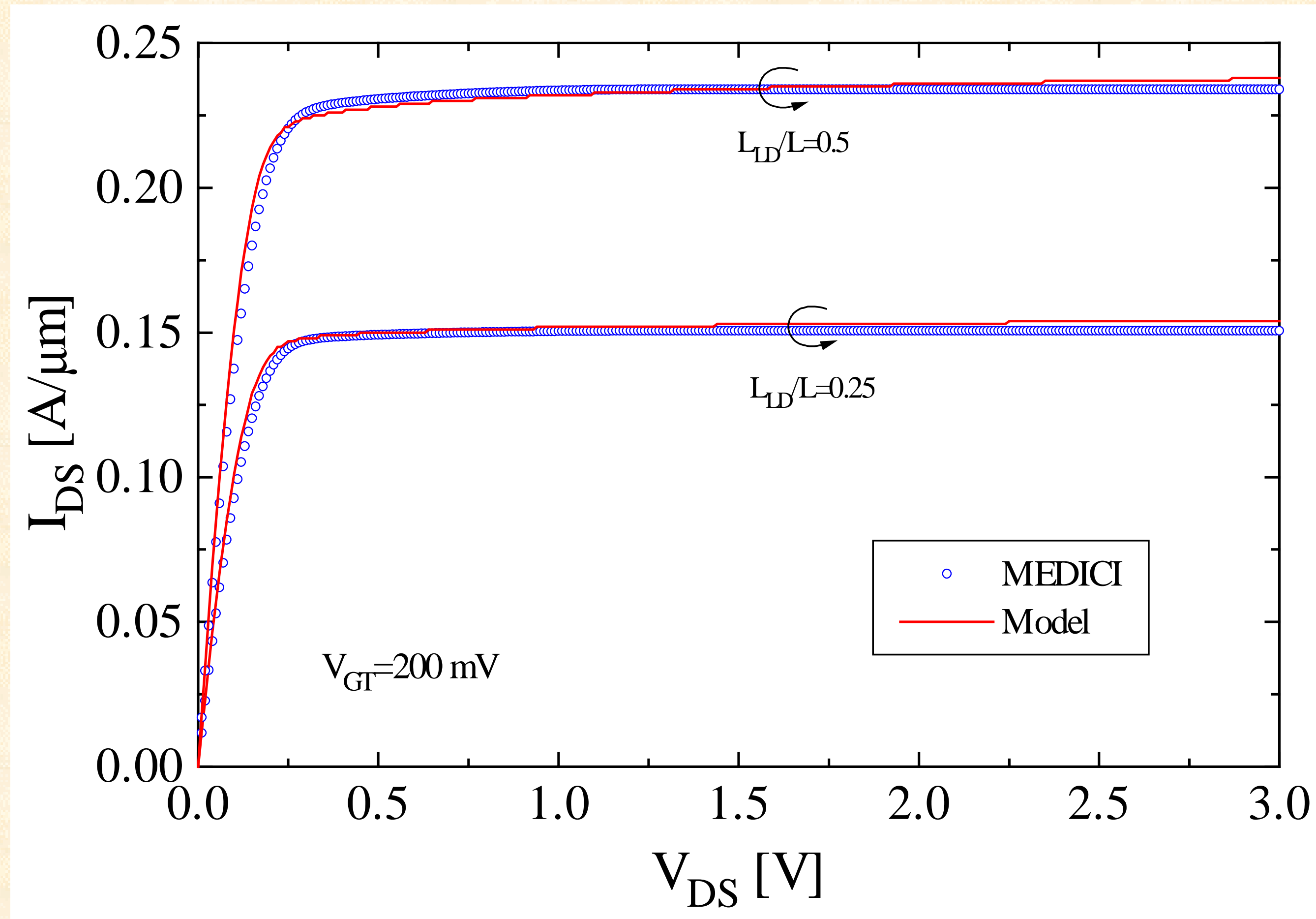
Gate characteristics in the linear regime



Gate characteristics in linear regime



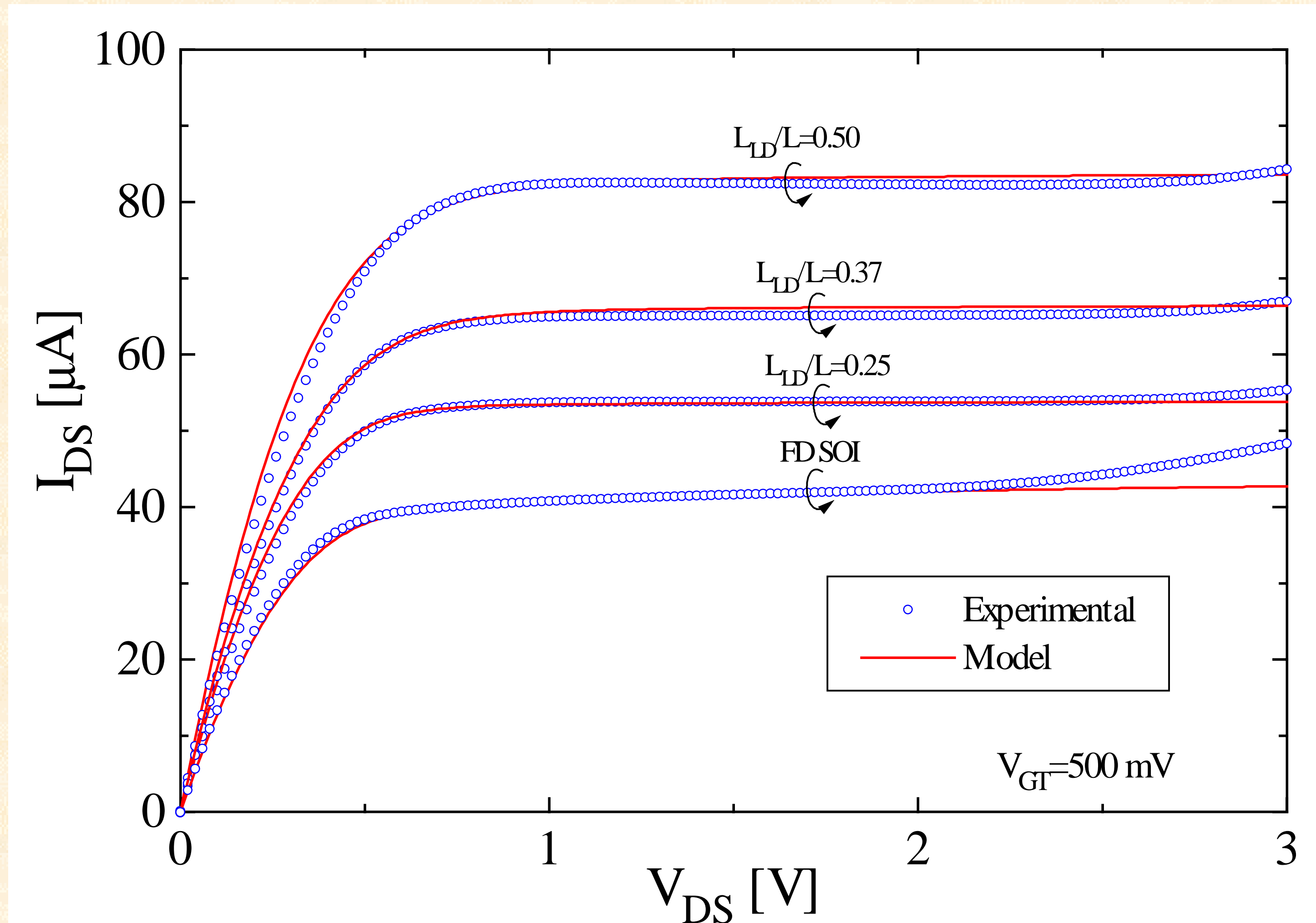
Drain characteristics



Excellent agreement between the model and MEDICI simulations

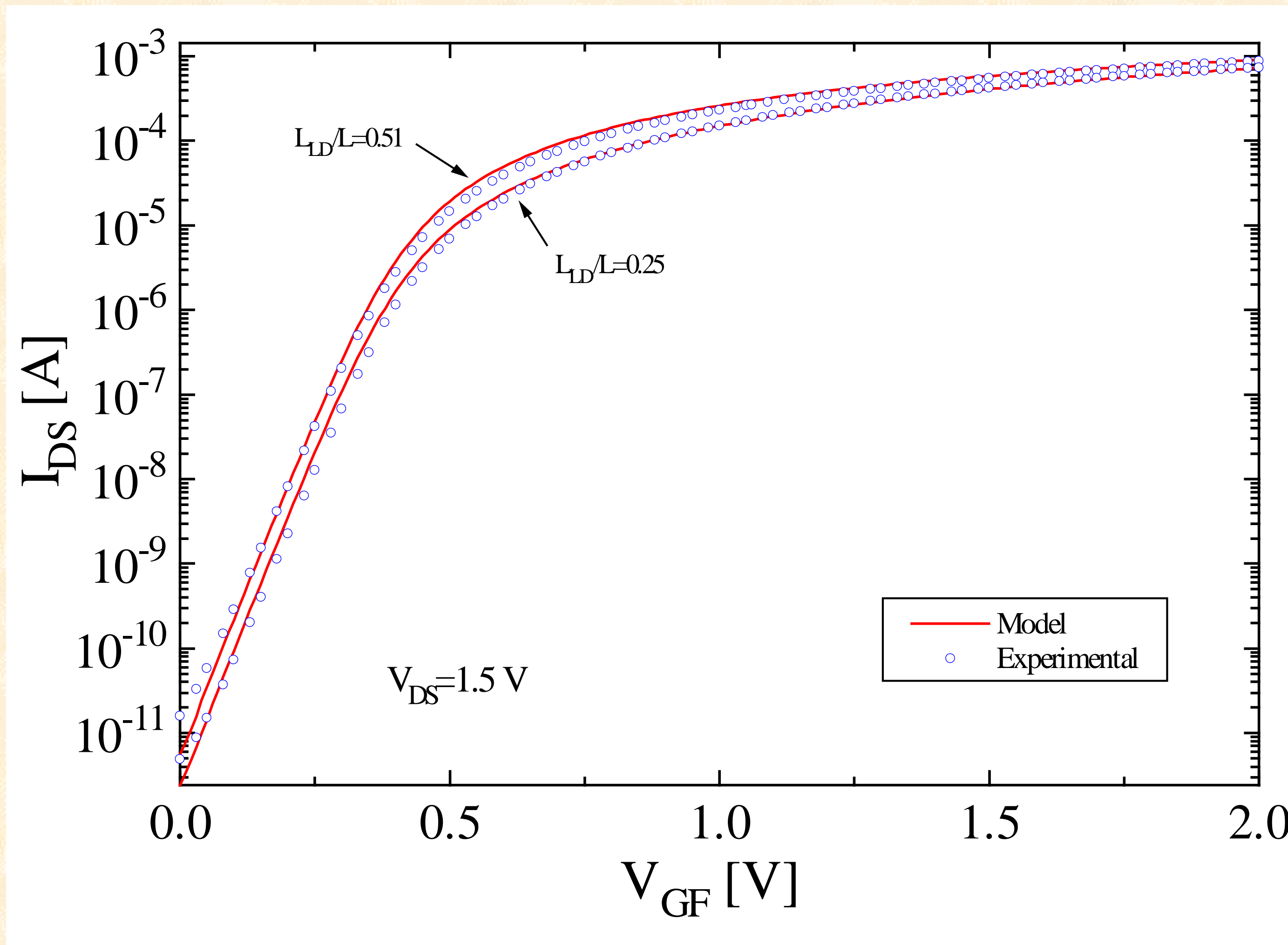
The increase of I_{DS} with L_{LD}/L (L_{eff} reduction) is greatly modeled

Drain characteristics - L = 4μm

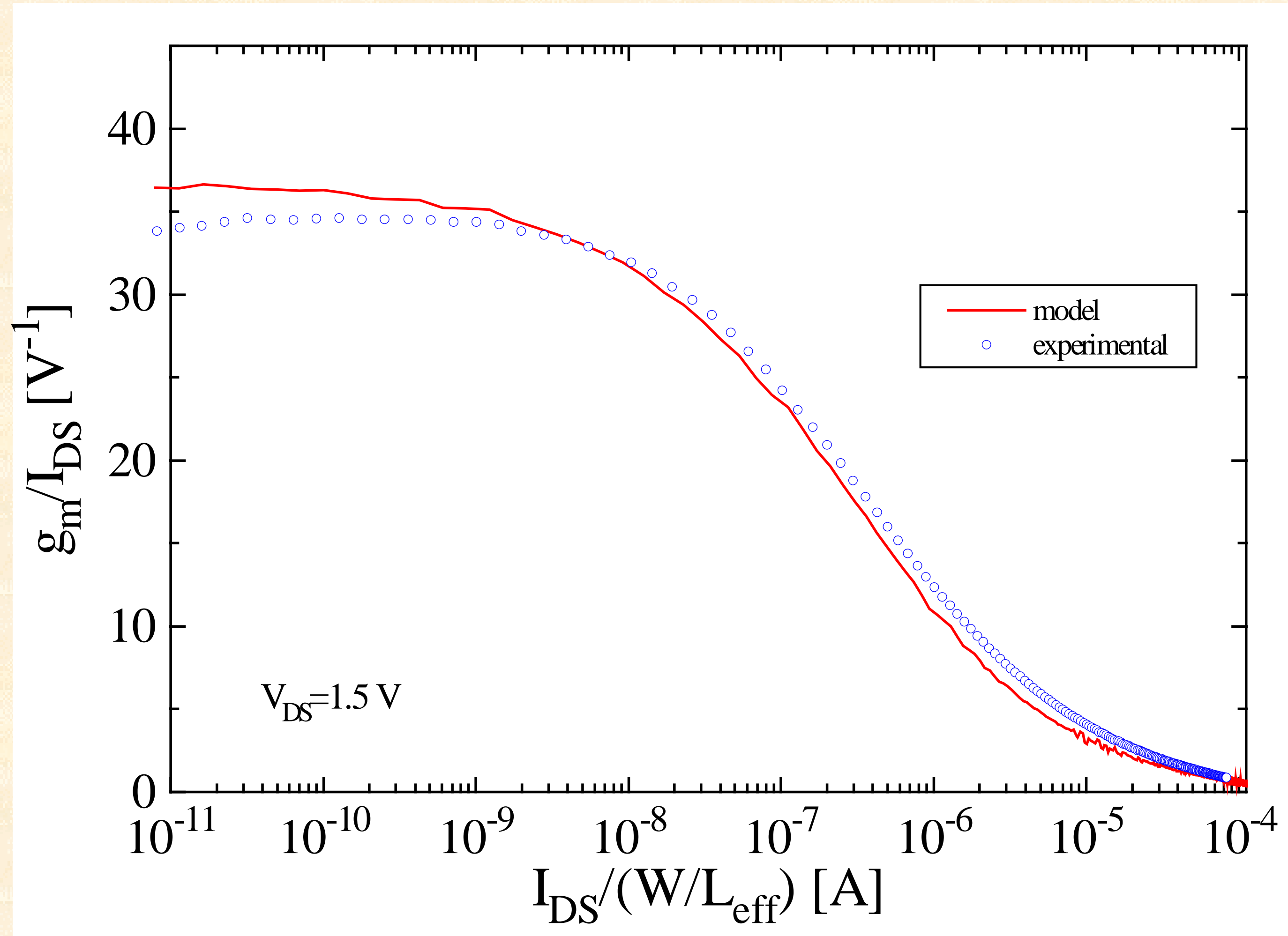


The tremendous increase in the Early voltage is adequately reproduced by the model

Gate characteristics in saturation - L = 2μm



Transconductance over drain current *vs* scaled drain current
L = 2μm



Our unified FD SOI MOSFET model has been adapted to long-channel Graded-Channel SOI nMOSFET based on a series association of transistors to represent the channel doping profile

The validity of the proposed model has been verified by both numerical simulations and experimental results

An excellent agreement has been found in both cases

Acknowledgements

Brazilian Federal Agency CNPq for the financial support

UCL Microelectronics Laboratory Staff for the device processing