g_m/I_d-Based MOSFET Modeling and Modern Analog Design

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Advancing Technology

- "Simple" MOSFET becomes complicated
  - Smaller geometries imply higher fields, or force true scaling of the power supply voltage
  - However, biggest change is MOSFET *usage*
- Analog design still uses old-style methods
  - Oversimplified descriptions of the MOSFET
- Analog "design gap"
  - Trying to make old methods work
  - Not getting full benefits of deep submicron technology

Analog Design – Hand Calcs.

- Good analog design is an art, not a science
- Best work still done on napkins, not EDA tools
- Use hand calculations…
- However, in most cases, equations which were once valid are now inadequate
- Only have this ability in certain limited cases

Limited Case – "Square Law"

- Old warhorse for strong inversion, saturation

$$I_{ds} = \frac{\mu \cdot W \cdot C_{ox}}{2 \cdot L} \cdot \left(V_{gs} - V_t\right)^2$$

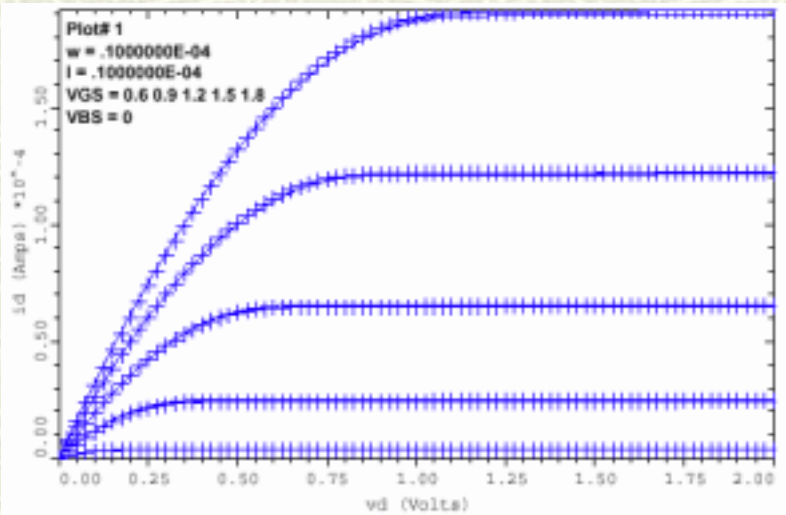
- Only vaguely valid now in large devices
  - Charge sharing is significant!
- Use of λ (Early voltage) now very questionable
- "Square law" becomes linear in short-channel limit
- (N.b. – weak inversion I_d α exp(V_g) still okay)

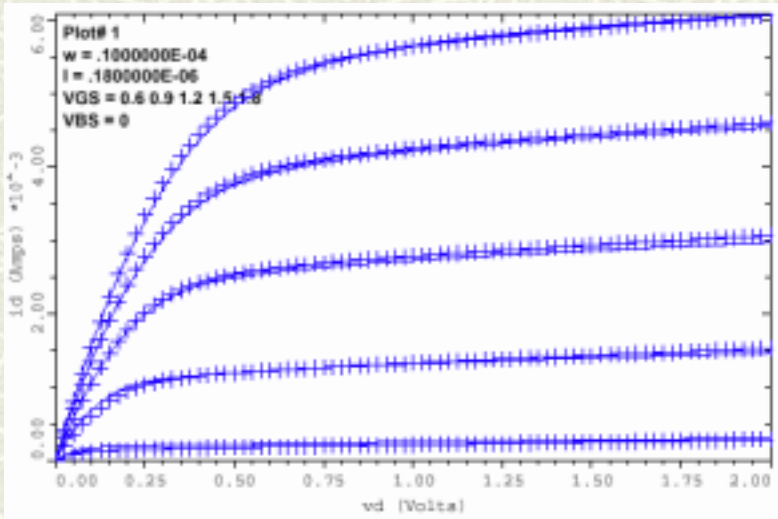
Present Situation

- In most cases, no good hand calculations possible
- Typical coping strategy? Just ignore this!
  - Assume basic square law is valid and just proceed
- Why has this not been a disaster? (Yet!)
  - Assumptions err on the cautious side
- E.g., square law uses $V_{dsat} = (V_{gs} - V_t)$
  - Over-predicts V_{dsat}, but keeps transistors in saturation
  - With $V_{dd} = 5V$, lots of margin for error

Deep Submicron Technology

- Square law calculation fails badly
- E.g., predicts 1.4V here, reality is c. 1.0V/0.5V





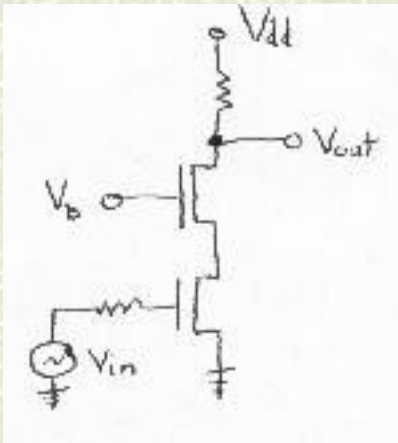
Deep Submicron Technology

- Collision of square law with decreasing V_{dd}
  - Difference is ridiculously large in both absolute and percentage terms
- This is only getting worse!

Technology	**V_{dd}**
0.18 μm	1.8V
0.13 μm	1.2V
0.09 μm	1.0V

Deep Submicron Technology

- Example: Simple cascode - tight “voltage budget”
- Want both transistors in saturation
- Need sufficient voltage across load for gain



Deep Submicron Technology

- No "voltage budget" to waste
- Square law V_{dsat} is unworkable
- Need low V_{dsat}, so DC gate biases are forced low
- Transistors biased in moderate inversion!
  - Hand calculations here?
- Thus, *proper* modeling of MOSFET over inversion range becomes critical
- Key information here! Need modern methods

Level of Inversion

- New design basis – level of inversion or "inversion coefficient" (IC)
- Work with both region of MOSFET operation **and** the level of inversion
- Use level of inversion as design variable
  - Replaces conventional approaches involving the bias current and the MOSFET channel width

Level of Inversion

- Define inversion coefficient as

$$IC = \frac{I_D}{2n\mu_o C_{OX}(W_{eff}/L_{eff})U_T^2} = \frac{I_D}{2nk_o(W_{eff}/L_{eff})U_T^2}$$

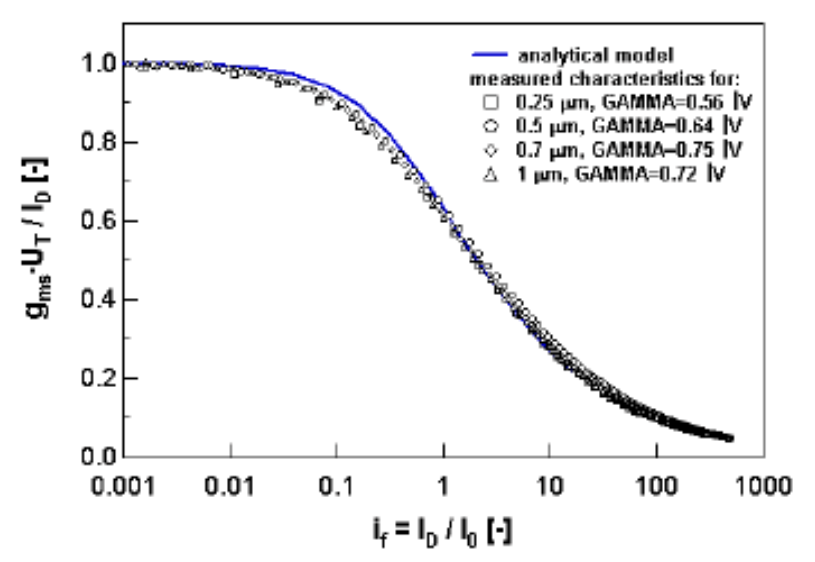
- Can simplify to (allowing graphical definition)

$$IC = \frac{I_D}{I_O(W_{eff}/L_{eff})}$$

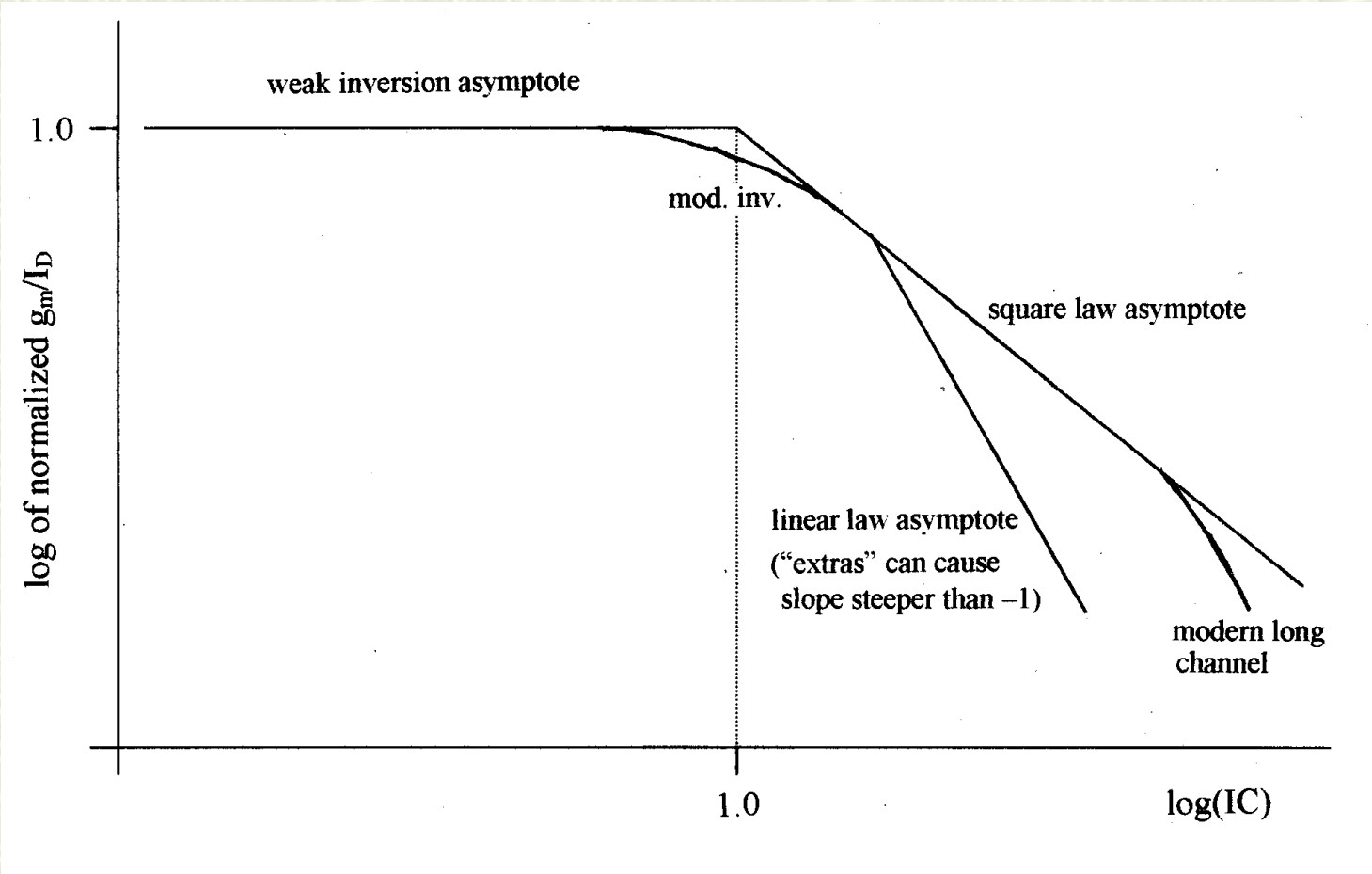
- IC = 1 defines center of moderate inversion

Interpreting IC

- Use normalized transconductance efficiency g_m/I_D
  - Fundamental to MOSFET
  - Direct guide to op-amp gain



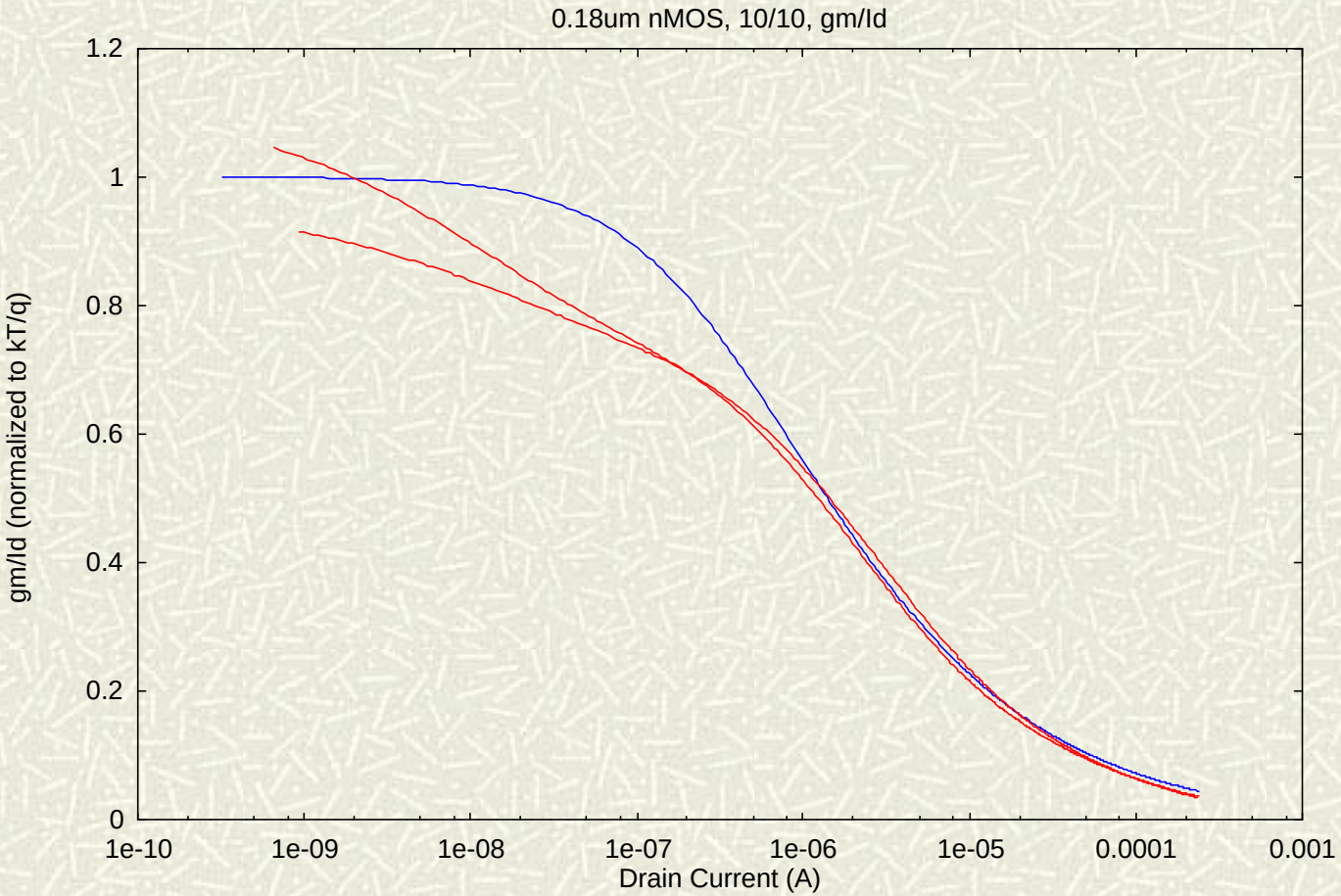
Interpreting MOSFET via g_m/I_D



Modeling g_m/I_D

- g_m/I_D is clearly fundamental to the MOSFET
- However, not a priority in model development
- Nearly all "popular" models fail here
- Presently, only the EKV model succeeds
  - Model is structured to do this right
  - Key "raison d'être" of EKV approach!
- (Some emerging models are finally starting to realize the importance of this)

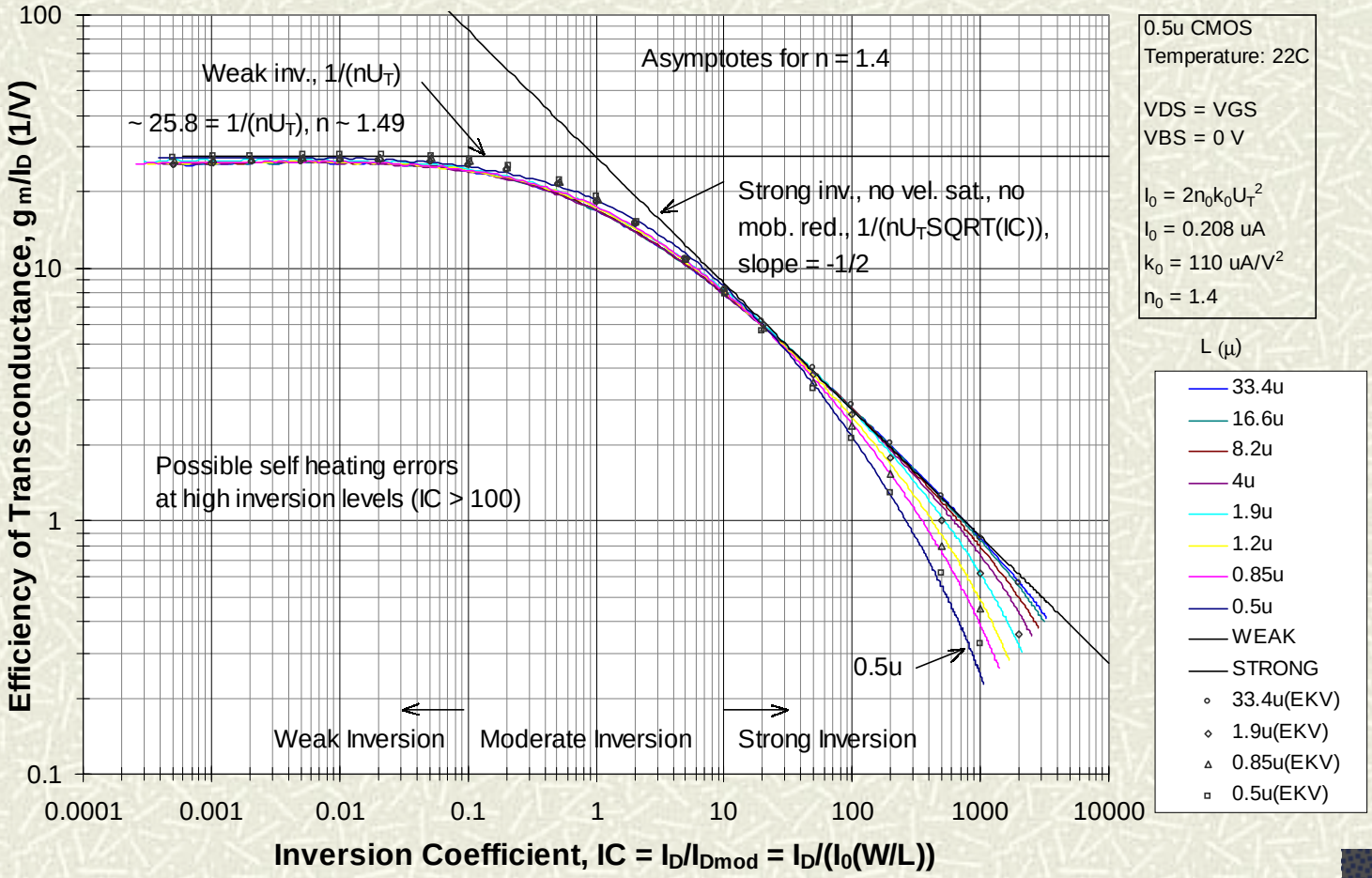
Modeling g_m/I_d – BSIM3?



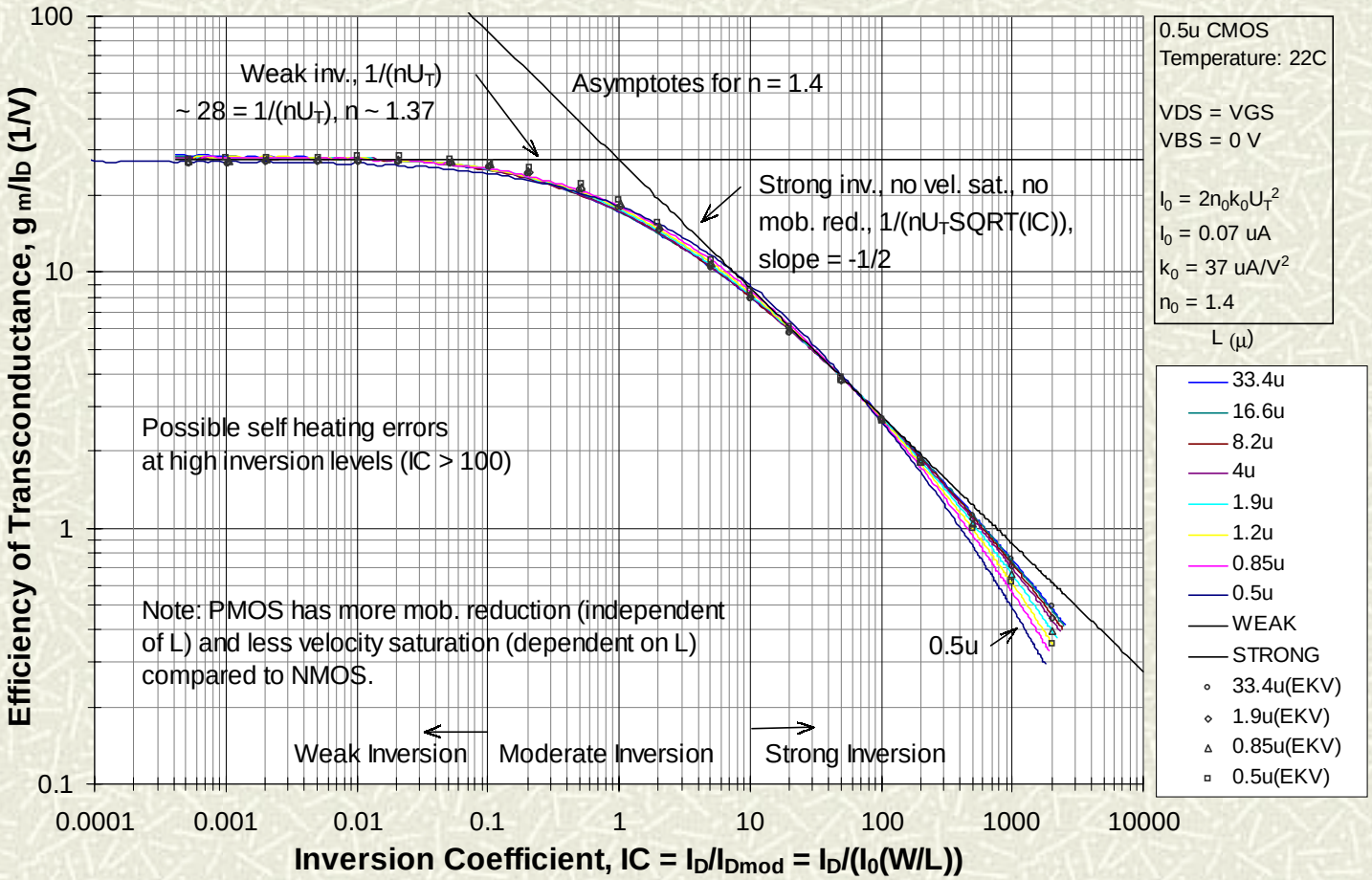
Characterizing g_m/I_D

- Since g_m/I_D is fundamental to the MOSFET, how can we extend that to characterization and design?
- Two connected items here:
  - Provide measurements and characterization for a particular MOS technology
  - Link that information across to design usage

Characterizing g_m/I_D - nMOS



Characterizing g_m/I_d - pMOS



Characterizing g_m/I_D

- New and different way of looking at MOSFET
- Universal across technologies
  - Have verified to 0.13μm
- Requires proper measurements
- Requires properly structured MOS model
- Doesn't get bogged down in overdone device physics
- Links nicely to modern analog design

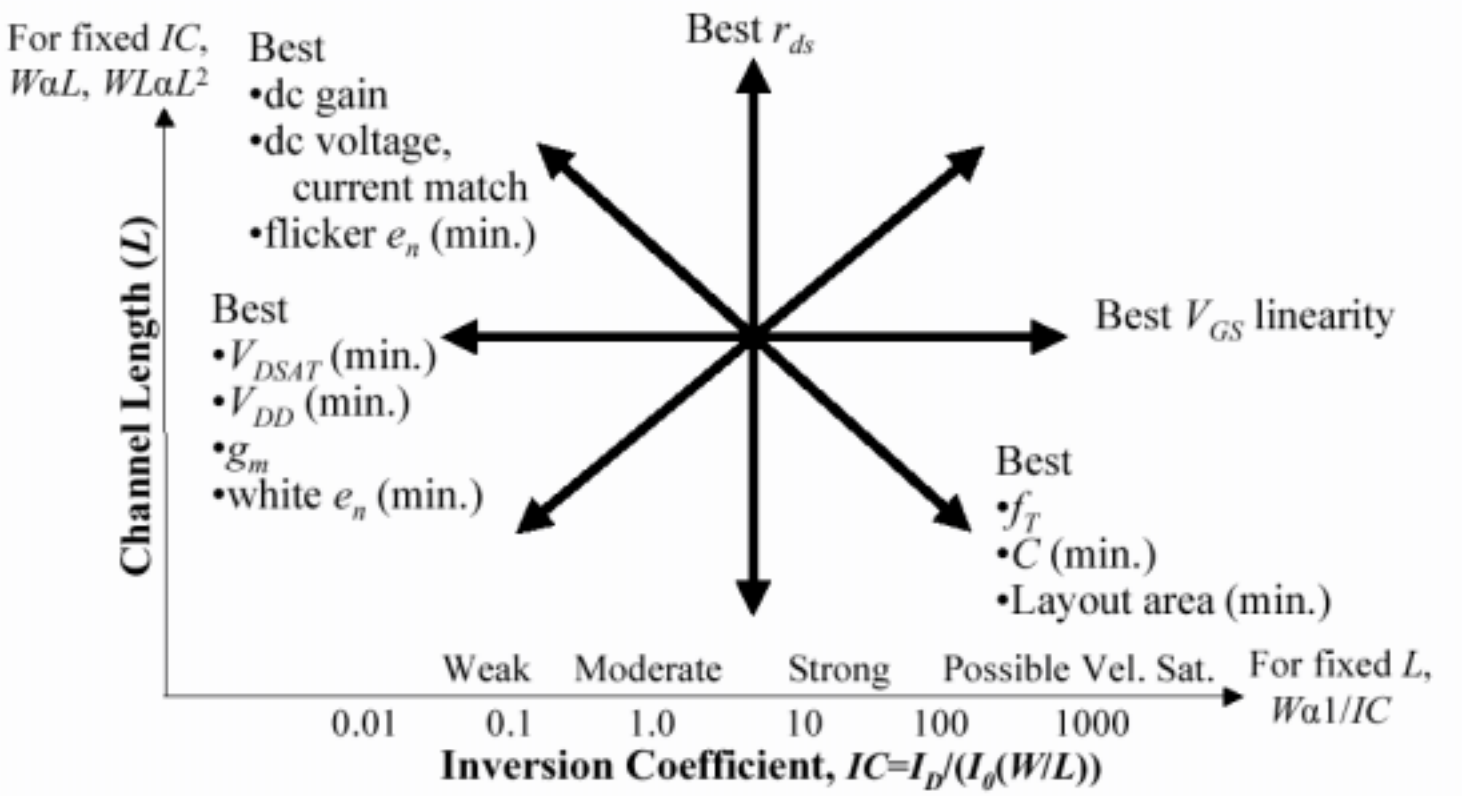
Analog Design Practice

- "Traditional" design guideposts are very weak
- "Traditional" design practices are also obsolescent
- Typical approach
  - Select bias current, back-find device width, iterate-iterate-iterate on currents and dimensions
- Obvious danger – process is neither controlled nor coherent
  - Time-consuming
  - *Ad hoc* journey to ????

Analog Design Practice

- Used to be more tolerable, due to slack constraints
- Present situation is much more difficult
  - Much lower supply voltages
  - More demanding design goals
  - Net: Much less margin for error
- Can run in circles, turning “knobs” and hoping…
  - Example: tight “voltage budget” in cascode
- Need a more modern, systematic approach

Use of IC in Design



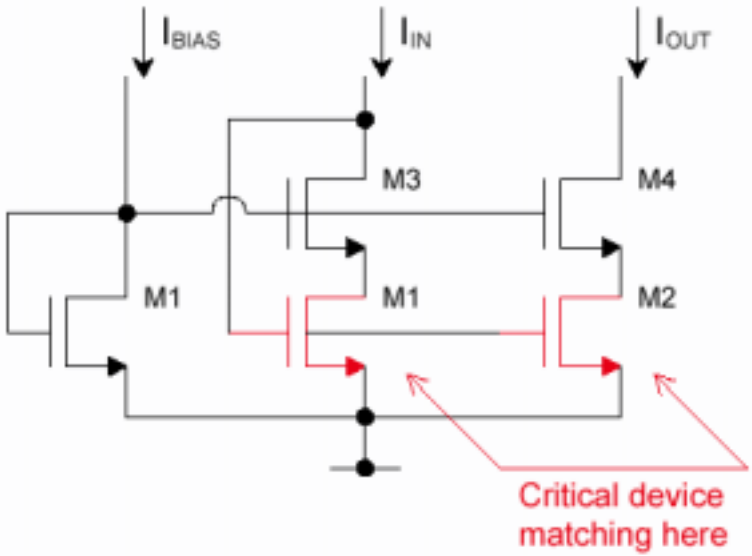
Use of IC in Design

- New and better basis for design
  - "Traditional" variables are I_D,L,W
  - Here, use I_D,L,IC
  - W follows as a *consequence* of the design
- Inversion level covers fundamental trade-offs
  - Strong inversion favors bandwidth
  - Weak inversion favors gain
  - Moderate inversion has emerged as mediator
- Circuit design that is *coherent* and *timely*

Design Methodology Illustration

Bandwidth, DC Matching, V_{DSAT} Tradeoffs

Current Mirror (100 µA)



- Bottom devices normally dominate bandwidth and dc matching.
- Bandwidth important in op amp signal path; bandwidth less than ½ intrinsic bandwidth (2 devices).
- DC current matching important in op amp signal path as mismatch reflects back as op amp input offset voltage.
- Low V_{DSAT} important for low voltage design.

Design Methodology Illustration

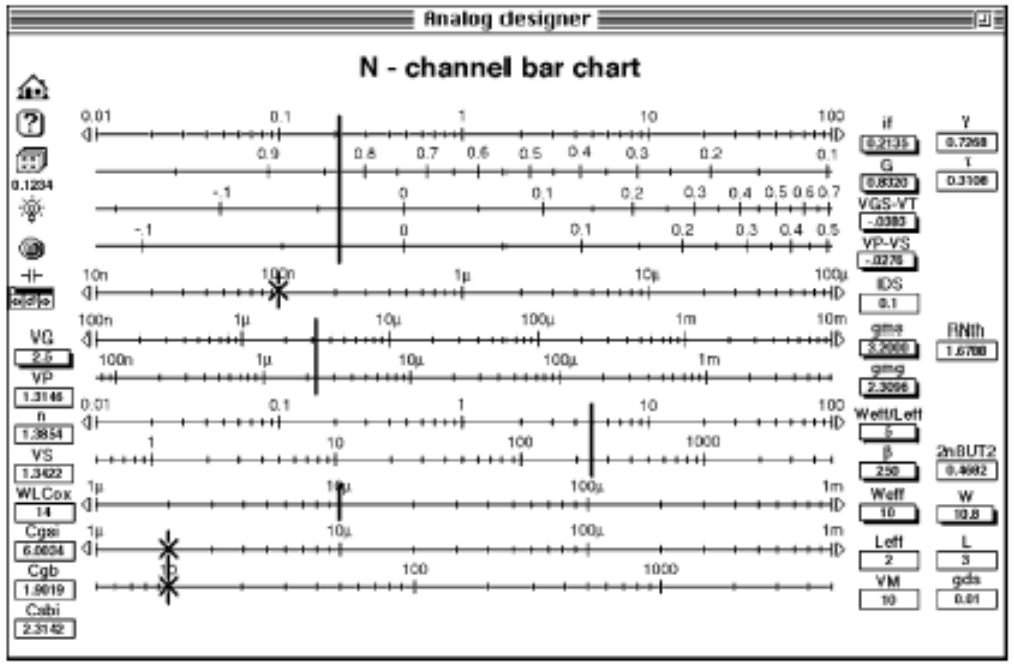
	IC	L (μm)	W (μm)	f_{Ti} (MHz)	$\Delta I_D/I_D$, 1σ, (%)	V_{DSAT} (V)
Best dc:	1	1.2	576	294	0.66	0.14
	2	1.2	288	445	0.78	0.16
	5	1.2	116	741	0.92	0.20
Balanced:	10	1.2	58	1,050	0.99	0.23
	20	1.2	29	1,450	1.03	0.33
	50	1.2	11.6	2,170	1.09	0.52
Best ac:	100	1.2	5.8	2,900	1.18	0.73

Design Methodology Illustration

	IC	*L* (μm)	*W* (μm)	f_{Ti} (MHz)	$\Delta I_D/I_D$, 1σ, (%)	V_{DSAT} (V)
Best ac:	10	0.5	24	5,710	2.24	0.23
	10	0.85	41	2,060	1.37	0.23
Balanced:	10	1.2	58	1,050	0.99	0.23
	10	1.9	91	426	0.63	0.23
	10	4.0	192	98	0.30	0.23
Best dc:	10	8.2	394	23	0.15	0.23

Use of IC in Design

- Ultimately, use a circuit simulator for “final polish,” not for the real design effort
- Future: Can conceive of simple GUI basis



(Courtesy of C. Enz)

Summary/Conclusion

- "Traditional" approaches to analog CMOS design are obsolete and are now dangerous
- "Traditional" hand calculation approaches are of very limited usefulness
- Constraints associated with deep submicron CMOS make situation very difficult
- Need to "re-think" methods from scratch – not just append a few "tweaks"

Summary/Conclusions

- Briefly illustrated design usage of the approach
- Is very simple yet very powerful!
  - Allows proper evaluation of design trade-offs
  - Coherent and encompassing – not "deconstructionist"
  - Allows for *thinking*, not just endless simulations which may or may not reach the goal
  - Exploit full analog potential of deep submicron CMOS
- Requires *properly structured* MOS model
- EKV structure is built for this purpose!

Summary/Conclusions

- Need to re-think and re-interpret the MOSFET for modern (deep submicron) analog design
  - "Design-driven modeling," "deterministic design"
- Need to develop modern design practices based around those interpretations
- Level of inversion (IC) and g_m/I_D provide this for MOSFET interpretation and design use
- This opens the door to coherent methods for analog design in deep submicron CMOS