MOS Transistor Modeling for HV Processes

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21.06.2002

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Overview

Process description

Device Description

- Finite element device simulation

Modeling the HV CMOS Transistor

- BSIM3v3 subcircuit
- BSIM4
- Parameter Extraction

Parasitic Modelling

- Safe Operating Area Check (SOAC)

The 50V or 90V HV Prozess (What's the use of it?)

High voltage ASIC applications up to 50 V or 90V

• Automotive, Industrial and Display markets.

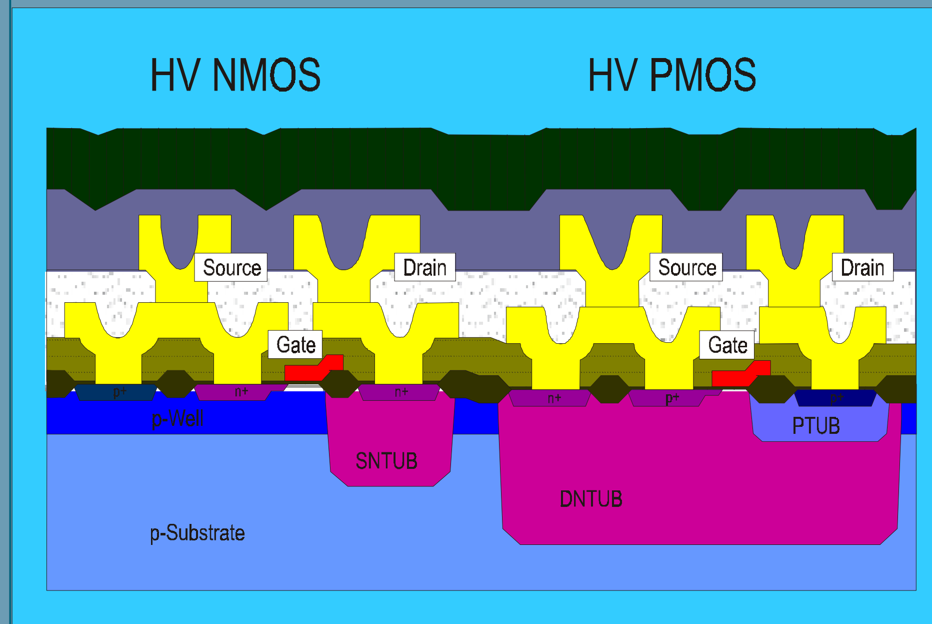
•The applications include, power management, liquid crystal display (LCD) drivers, automotive electronics, motion control (brushless DC motor controllers) and micro electro-mechanical (MEM) IC's.

•N(P)MOS transistors, HV-NMOS, HV-PMOS, HV-DMOS transistors, N-junction FETS, isolated NPN bipolar transistors, isolated LV-MOS Transistors.

Parameter	Characteristics
Drawn Leff Low Voltage	0.8 µm
Drawn Leff High Voltage	3.0 µm (PMOS) and 2.0 µm (DMOS)
Metal composition	TiSi2/TiN/AlSiCuTi
Isolation method	Semi recessed oxide isolation
Gate oxide thickness	Dual gate: 17 nm / 51 nm
Field oxide thickness	0.4 µm
Polysilicon pitch	1.7 µm
Diffusion pitch	2.2 µm
Metal 1/ Metal 2 pitch	2.1 µm / 2.3 µm
Metal 1 / Metal 2 thickness	600 nm /1050 nm
P substrate resistivity	20 Ωcm

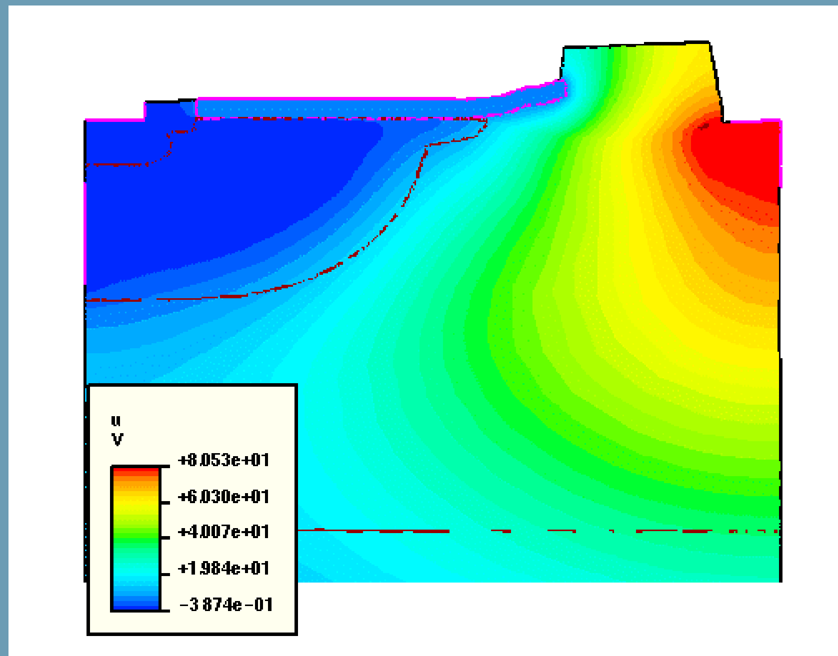
Structural Process Characteristics

The 50V or 90V HV Prozess



- SVX technology
- low cost BCD technology
- reduced number of masks
- no buried layer or sinker
- double RESURF effect.

Device description



Device simulation (potential distribution) of a HV DMOS transistor @ VG=5V & VD=80V
showing moderate Voltages under the field plate.

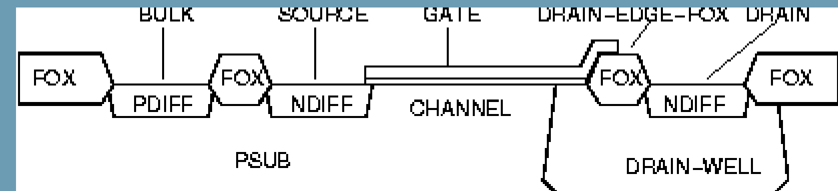
RESURF effect.

With this effect the harmful high surface potential in the PTUB to drain-well junction region (HV NDMOS) is lowered by the gate voltage applied on the field plate extension over the field oxide (FOX).

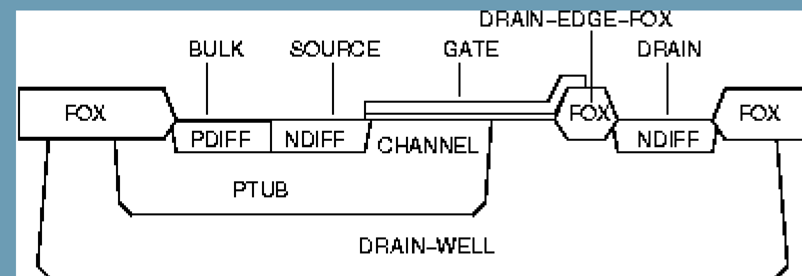
Device description

avoid channel hot carriers effects and eventual avalanche breakdown

- Extending the vertical length
- Reducing the doping concentration of the NWELL at the drain region
- Drain extension
  - Reduces the channel electric field
  - Increasing the channel resistance
  - Increasing the drain to source breakdown voltage.
- A field plate extension
  - Reduction of the surface potential in the "hot" region at the substrate (or PTUB) to drain-well junction region
  - Electron current is forced into the depth of the well.



Single-sided (asymmetrical) HV NMOS transistor available with thin and thick gate oxide



HV DMOS transistors available with thin and thick gate oxide.

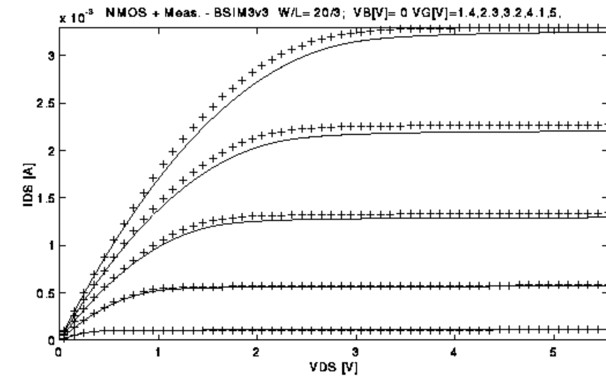
Effects for the HV Transistor Modelling

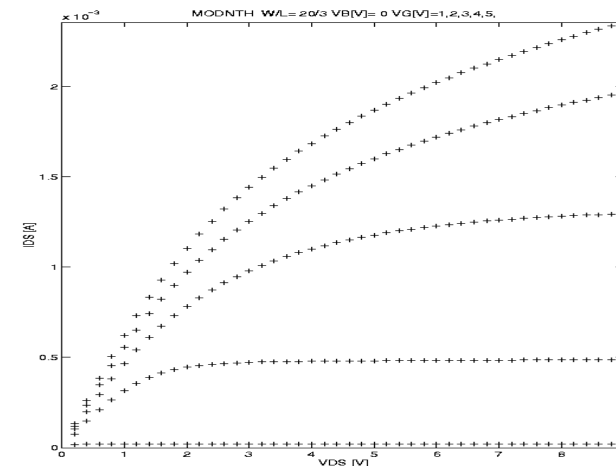
- Increase in the on-resistance RON

- Reduction in the drain capacitance

- Drift region in the drain-well dominates the transistor behaviour at high gate voltages.
(VG>5V for transistors with thick gate oxide).

- Reduction of the transconductance to due the lateral series resistance.





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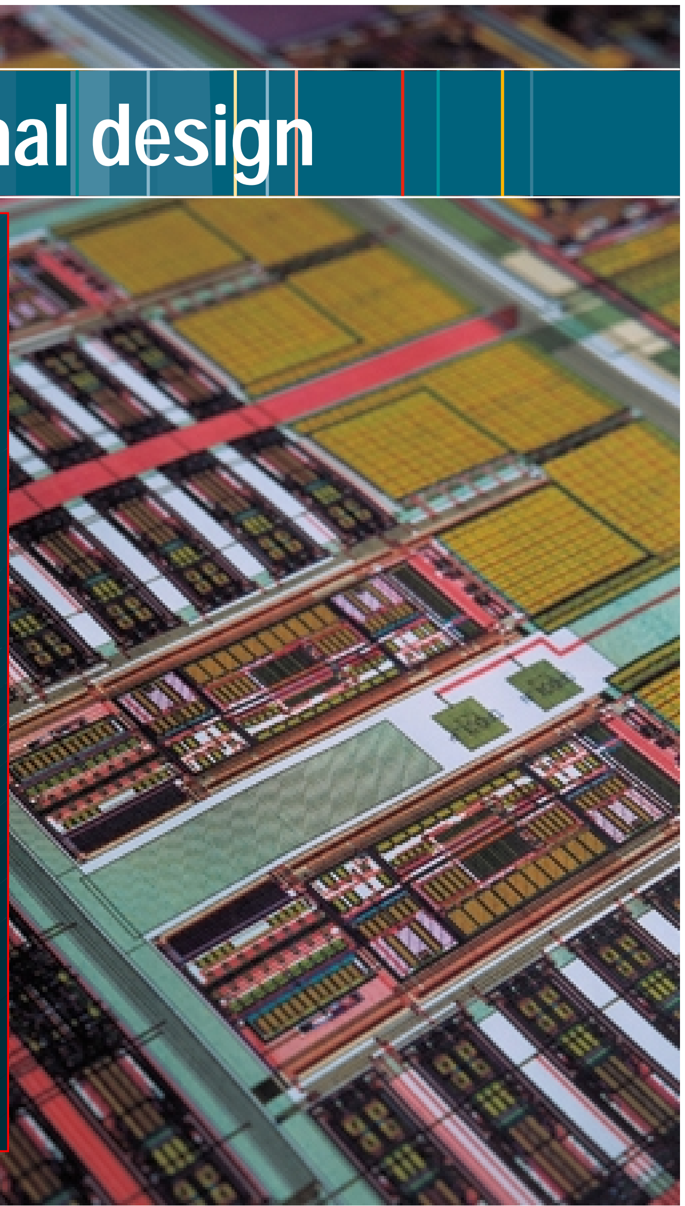
SPICE Modelling for HV mixed/signal design

Goal:

- Scalable models (sub-circuit) valid for any geometry and all specified operating conditions
- Compatibility to all important simulators (Eldo, Spectre, HSPICE, Saber)
- Usable for analog/ms design
  - High accuracy
  - Short simulation time
  - Smooth gm,gds
  - Simulation convergence
  - Accurate parasitic currents and capacitance



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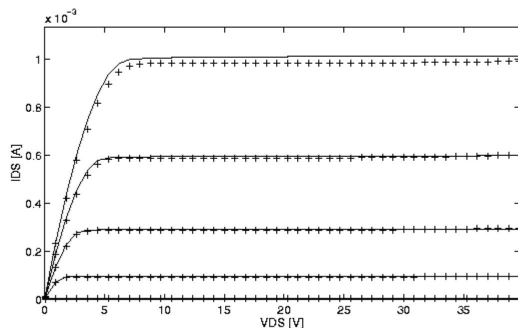
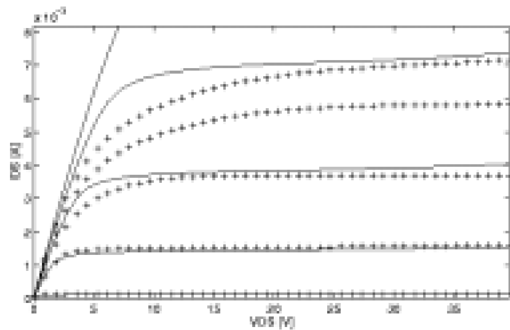
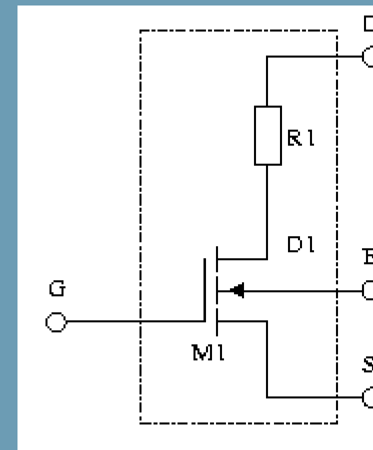
BSIM3v3 for HV CMOS application

BSIM3v3: $$RDS = \frac{RDSW\left(1 + PRWG \cdot VGS\right)}{W}$$





Simple Subcircuit1:



HV NMOS output characteristic
W/L=40/40 ;W/L=40/3
VGS=2.67,5,7.33,9.67,12V;
+= measurements,

solid lines = sub-circuit1.

$$R1 = \frac{RHV \cdot LHV}{W + WHVC}$$

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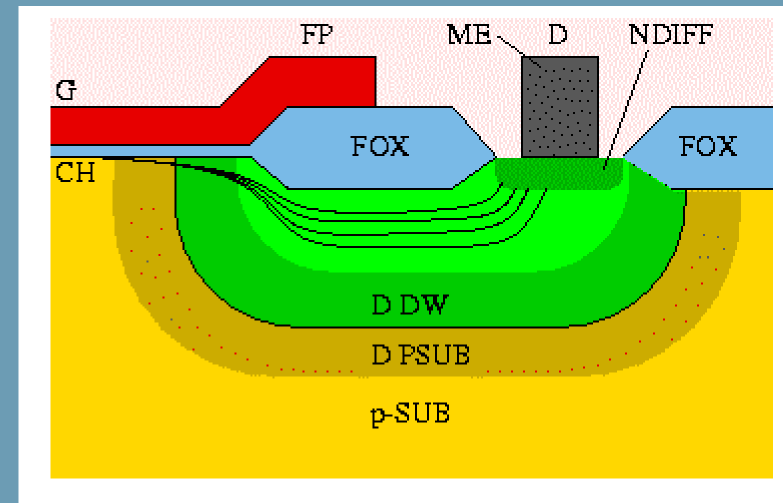
Sub-circuit using JFETs

The behaviour of the drain well is similar to a junction FET device :

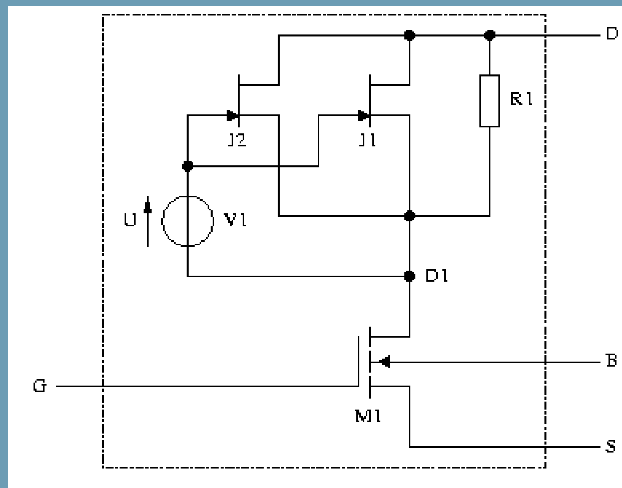
- Effect of the depletion regions
- Effect of the field plate.



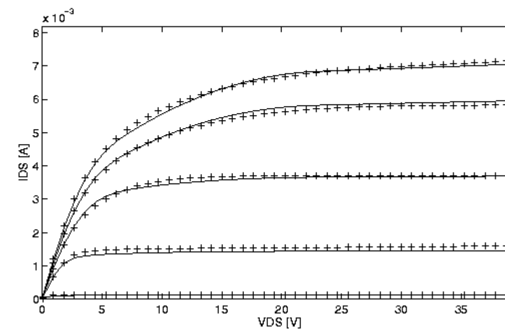
The drain of the HVMOS transistor.
The reverse biasing of the drain well substrate junction reduces the cross-section of the drain well.
The behaviour of the drain well is similar to a junction FET.

BSIM3v3 for HV CMOS application

Subcircuit2:



The two JFETs J1 and J2 are responsible for the quasi-saturation and saturation region modelling.
The resistor R1 models the on-resistor accurately and the voltage controlled voltage source takes the scalability into account.



HV NMOS output characteristic
W/L=40/3 VGS=2.67,5,7.33,9.67,12V;
+= measurements,
solid lines = sub-circuit2.

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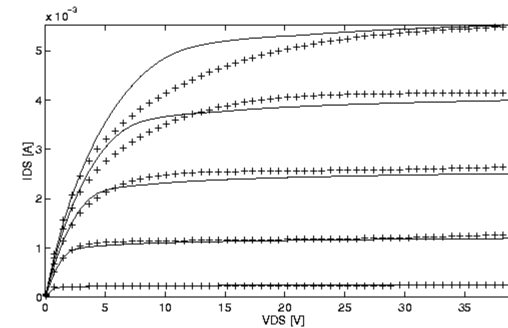
BSIM4

The RS diffusion resistor and the RD well resistor may be external and asymmetrical.
That means RS does not have to be equal to RD.

RDSMOD=1 (External RD(V) and RS(V)):

$$RS(V) = \left\{ \begin{matrix} RSWMIN + RSW \cdot \\ \left[\left[PRWB \cdot VBS + \frac{1}{1 + PRWG \cdot (VGS - VFBSD)} \right] \right] \end{matrix} \right\} \Big/ [1e6 \cdot Weff]^{WR}$$

$$RD(V) = \left\{ \begin{matrix} RDWMIN + RDW \cdot \\ \left[\left[PRWB \cdot VBD + \frac{1}{1 + PRWG \cdot (VGD - VFBSD)} \right] \right] \end{matrix} \right\} \Big/ [1e6 \cdot Weff]^{WR}$$



HV NMOS thin gate oxide output characteristic W/L=40/3 VGS=1.4,2.3,3.2,4.1,5 V; += measurements, solid lines = BSIM4.

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DC Model Parameter extraction

Goal:

•Scalable models valid for all geometries and all specified operating conditions
•Usable for analog/ms design

Local and global parameter extraction strategy:

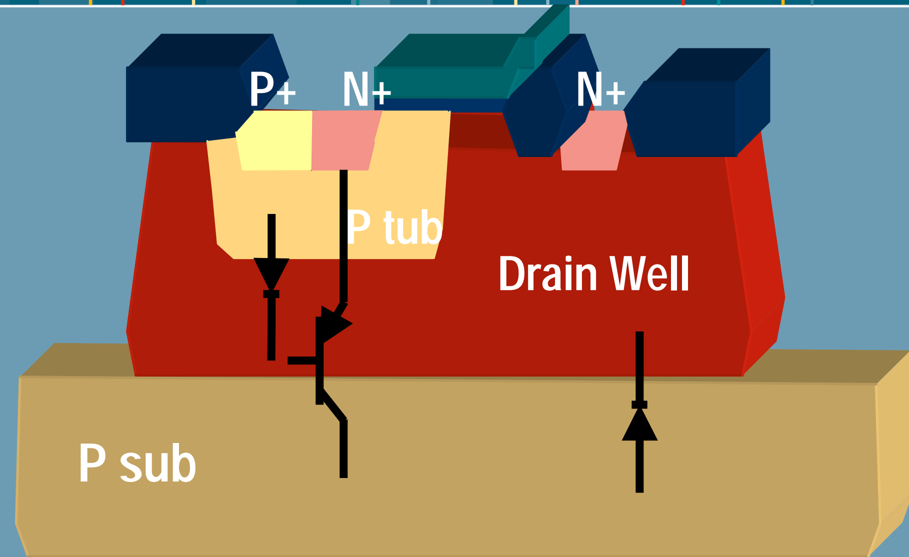
•id/vg,id/vd,gm,gds
•Intrinsic MOS for low vgs and vds below quasi saturation (BSIM3/4)
•Subcircuit1 & 2 JFET and R parameter at high vgs & vds

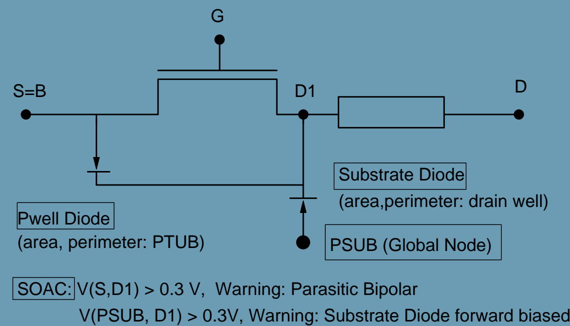
Tool: UTMOST for measurements, Matlab in combination with SPICE simulator

HV CMOS - Parasitic Modelling

Advanced HV parasitic models

- Using standard S/D diodes is not possible
- NDMOS: well-psub and PTUB-drain well
- parasitic pnp transistor (swich off (vds<0.0))
- Diode parameter calculated form W & L & design rule values
- PNP is checked with SOAC





Results: Charge Injection circuit, *simulation of residual offset voltage.*

	Measured	Parasitic Simulation	Standard Simulation
Residual Offset	120 mV	152mV	257 mV

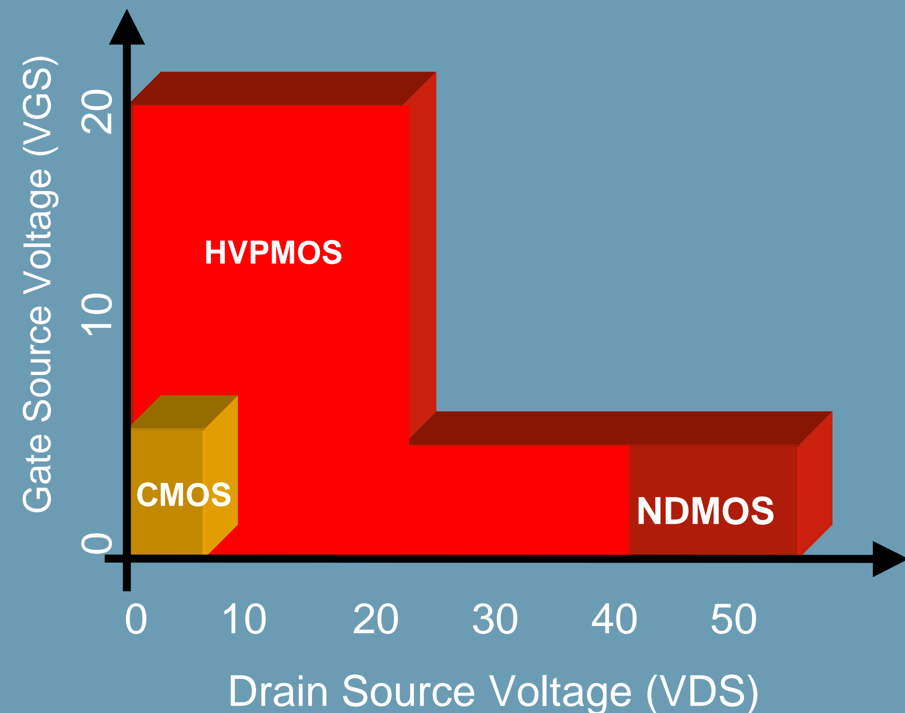
HV CMOS - SOAC Simulation

Advanced HV SOAC models and Simulation Setup

• SOAC simulation checks operating conditions during simulation (also transient).

• Correspondence with process parameter document .

• Implementation: Cadence (AHDL), Mentor (ELDO native).



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Conclusion

-Presented the principles of the austriamicrosystems 50 & 90V HV-CMOS processes

-described the most important HV-MOS transistors and the physical relevant effects

-SPICE modelling with simple sub-circuits

-HV CMOS SPICE modelling with BSIM4

-Parasitic HV CMOS Sub-circuit modelling for pre-layout simulation

-Implementation of the SOAC