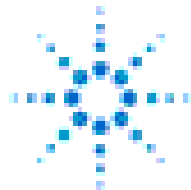


Ewout Vandamme (Agilent Technologies, NMDG),
Wladek Grabinski (Motorola, Geneva),
Dominique Schreurs (K.U.Leuven), and
Thomas Gneiting (ADMOS)

LARGE-SIGNAL NETWORK ANALYZER MEASUREMENTS AND THEIR USE IN DEVICE MODELLING



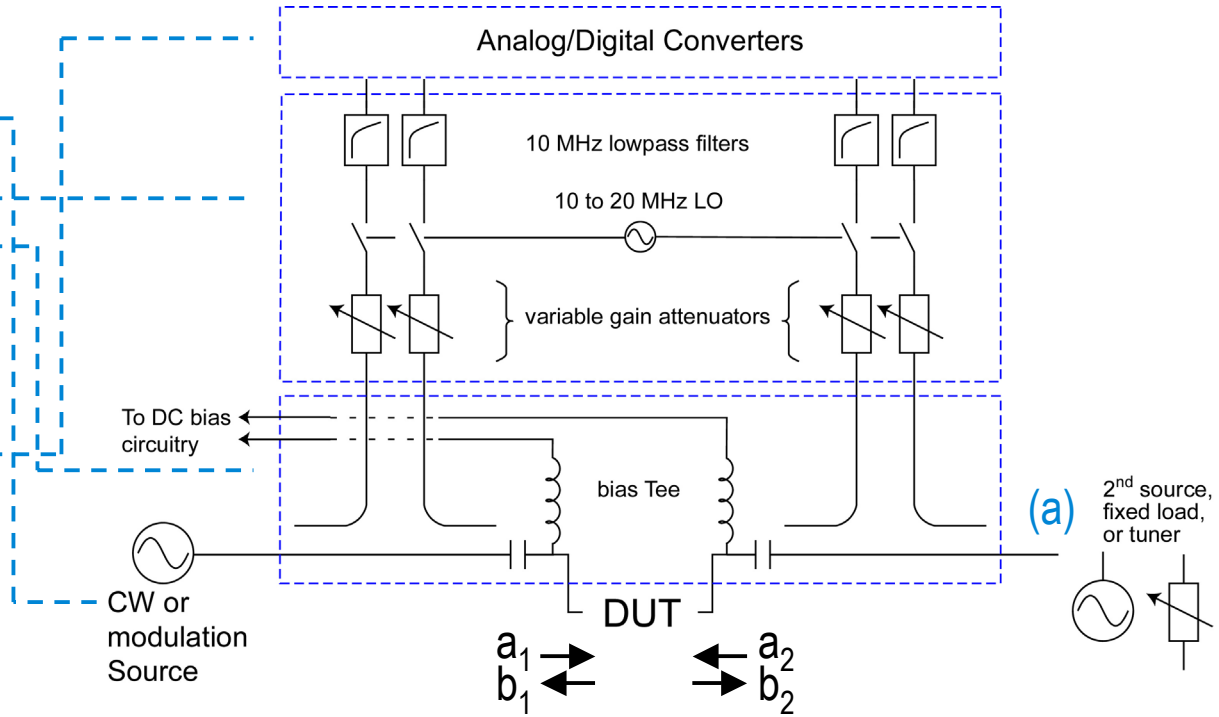
Agilent Technologies

Outline

- **Large-Signal Network Analyzer (LSNA) technology**
- **Advantages of using LSNA for device modelling engineers**
- **LSNA measurements**
 - de-embedding
 - implementation in CAE tool (iccap)
 - measurement and simulation results
 - tuning of model parameter to LSNA measurements
- **Conclusions**

Agilent's Large-Signal Network Analyzer technology

- RF bandwidth: 600 MHz - 20 GHz
- max RF power: 10 Watt
- IF bandwidth: 8 MHz
- Needs CW or periodic modulation

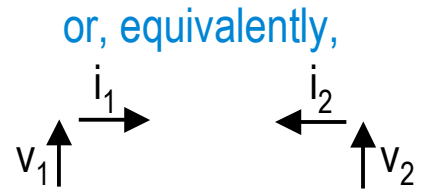


Calibration Standards:

Cal Kit,
e.g. LOS, LRRM, etc.

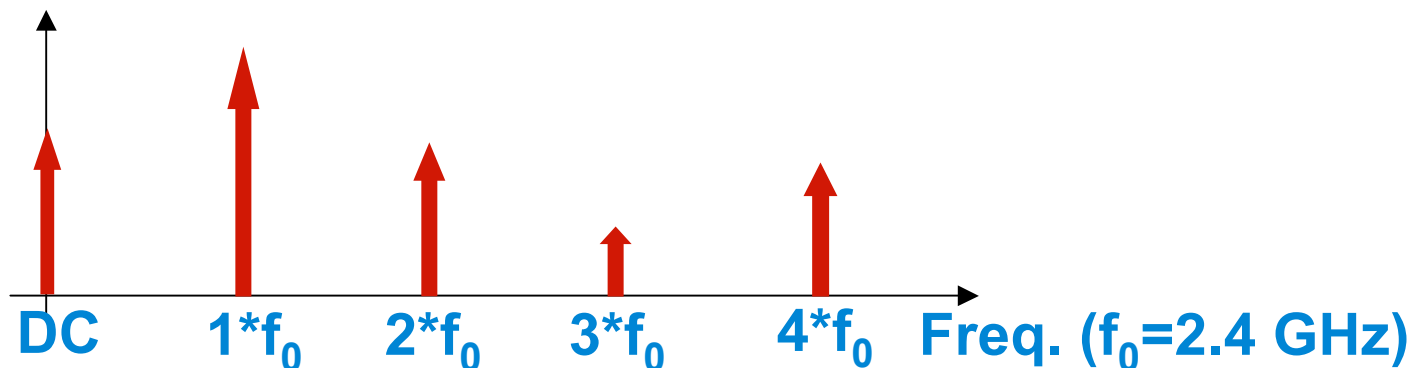
Power Std

Phase Std



CW class of signals measured with LSNA

- **2-port Device-Under-Test (DUT) under periodic excitation**
 - e.g. transistor excited by a 2.4 GHz tone with an arbitrary output termination
- **All current and voltage waveforms are represented by a fundamental and harmonics**



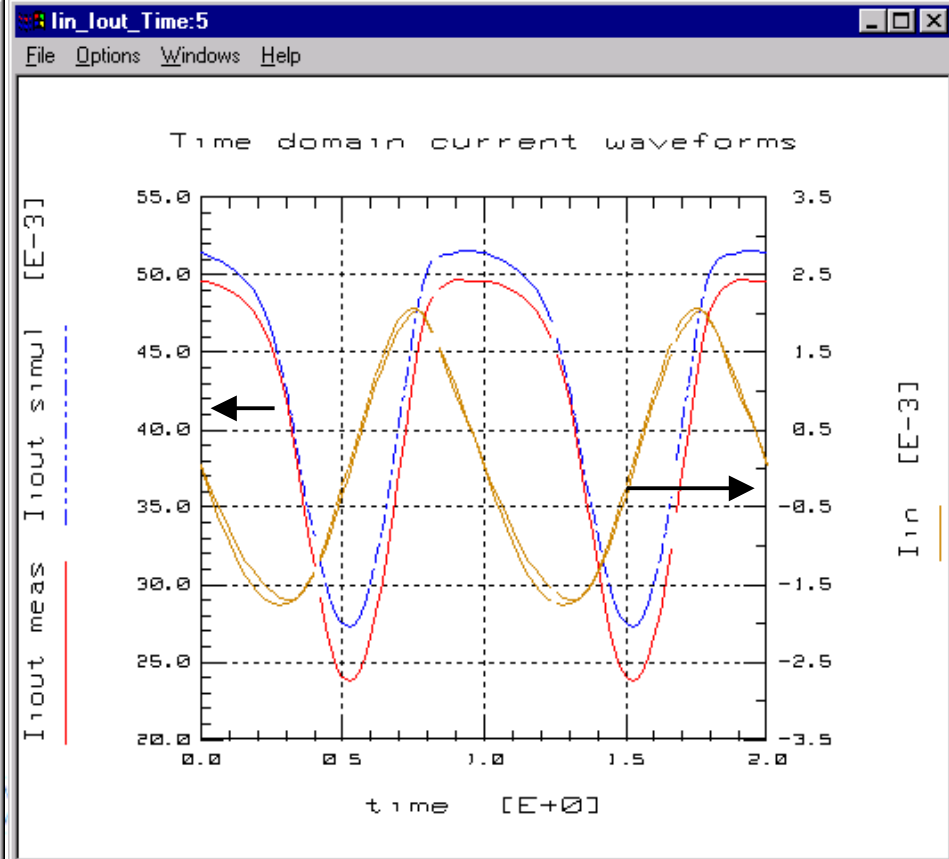
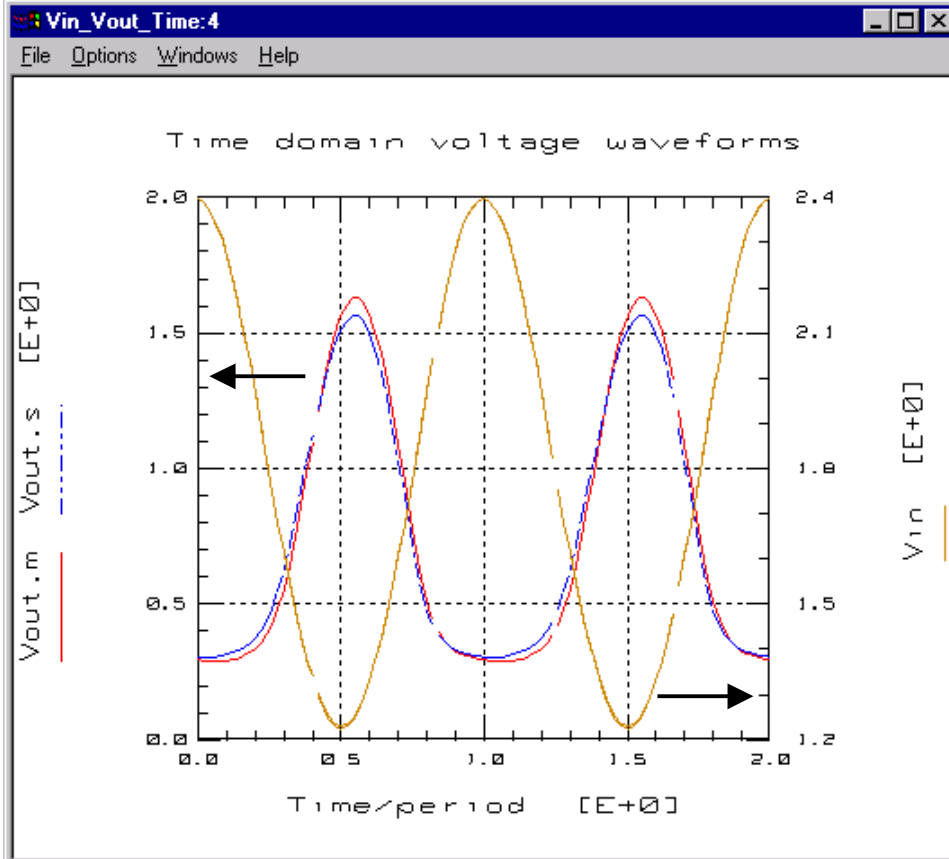
- **Spectral components X_h = complex Fourier Series coefficients of the waveforms**

LSNA measurements: time domain, frequency domain or combination of both (e.g. envelope in modulation)

$$x(t) = \text{Re} \left(\sum_{h=0}^H X_h e^{j 2\pi h f t} \right)$$

$f = 1/\text{period} = \text{fundamental frequency}$

$$X_h = 2f \int_0^{f^{-1}} x(t) e^{-j 2\pi h f t} dt$$



Advantages of using the LSNA in device modelling

- Measure the following characteristics of your DUT making a *single* connection, using *one* measurement setup (the LSNA)
 - DC,
 - Small-signal (Scattering parameters), and
 - Large-signal behaviour
- Verify the model accuracy of your device under *realistic* operation conditions
 - power amplification
 - high-speed switching
- Identify modelling problems at a *single* glance
 - LSNA measurements, e.g., immediately reveal weaknesses in capacitance and charge models

Use of LSNA measurements in CAE tool (iccap)

⇒ model verification, optimisation (and extraction)

The screenshot shows the ICAP software interface. On the left is a netlist window with the following content:

```

define hbsim n1dc n1dcl n1rf n2dc n2dcl n2rf n1 n2 n1dut n2dut drain gate bulk dummy1
: node 1 2 3 4 5 6 7 8 9 10 11 12 13 14

Short_DC_Feed1 n1dc n1dcl Mode = -1
R_RbiasTEE1 n1dcl n1 R=0.001
Short_DC_Block1 n1rf n1 Mode = 1

Short_DC_Feed2 n2dc n2dcl Mode = -1
R_RbiasTEE2 n2dcl n2 R=0.001
Short_DC_Block2 n2rf n2 Mode = 1

: additional gate, drain and bulk resistance
R_Rgate n1dut gate R=6.7
R_Rbulk bulk 0 R=1
R_Rdrain n2dut drain R=3

LSNA_MOSFET_Q1 drain gate 0 bulk
end hbsim

#echo i1=1
#echo i2=1
#echo fundamental=2.4E9
#echo Zo=50

#echo #define usetoken #selib
#echo usetoken "ckt", "DAC"
#echo DAC_DAC1 File="F:\home\ewout\iccap\Pctryout\rf5_c_2_2400MHz_de_vi_dc.cit" Type="citi" InterpMode="index"
#echo v1dc=file(DAC1,"v1dc")
#echo v2dc=file(DAC1,"v2dc")
#echo V_Source:V1DC n1 0 Vdc=v1dc
#echo V_Source:V2DC n4 0 Vdc=v2dc

#echo #define usetoken #selib
#echo usetoken "ckt", "DAC"
#echo DAC_DAC2 File="F:\home\ewout\iccap\Pctryout\rf5_c_2_2400MHz_de_a.cit" Type="citi" InterpMode="index"
#echo a1=file(DAC2,"a1")
#echo Port:Power n3 0 Z=50 P[1]=polar(mag((a1**2)/(2*50)),phase(a1)) FundIndex=1
#echo V_Source:VinRF n333 0 V[1]=0 V_A11=2*a1 Freq[1]=fundamental
#echo R_Rinput n333 n3 R=Zo
#echo R_Rdummy1 n14 0 R=1E4

: following lines provide the link to measured load impedance as a function of different
: bias settings (not really needed) and, most important, FREQUENCY !!
: due to mismatches and nonlinear interaction with the DUT, the load is not exactly 50 Ohm
#echo #define usetoken #selib
#echo usetoken "ckt", "DAC"
#echo DAC_DAC3 File="F:\home\ewout\iccap\Pctryout\rf5_c_2_2400MHz_de_Zout.cit" Type="citi" InterpMode="index"
#echo Z_Port:Z1P1 n5 0 Z[1,1]=Zout
#echo Zout=file(DAC3,"Zout")
    
```

On the right, the simulation setup window shows various components with red arrows pointing from the netlist to them:

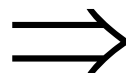
- Input: pindummy**: Mode: W, + Node: dummy1, - Node: GROUND, Resistance: 50.00, Fund: 1, Unit: W, Compliance: 0.000, Sweep Type: LIN, Sweep Order: 1, Start: 1.000, Stop: 21.000, # of Points: 21, Step Size: 1.000.
- Input: v1dummy**: Mode: P, Param Name: I1, Unit: I, Sweep Type: LIN, Sweep Order: 4, Start: 1.000, Stop: 6.000, # of Points: 6, Step Size: 1.000.
- Input: v2dummy**: Mode: P, Param Name: I2, Unit: I, Sweep Type: LIN, Sweep Order: 3, Start: 1.000, Stop: 6.000, # of Points: 6, Step Size: 1.000.
- Input: v1**: Mode: V, + Node: n1d,t, - Node: n1, Unit: V, Compliance: 0.000, Sweep Type: CON, Value: 0.000.
- Input: v2i**: Mode: V, + Node: n2d,t, - Node: n2, Unit: V, Compliance: 0.000, Sweep Type: CON, Value: 0.000.
- Output: vin**: Mode: V, + Node: n1, - Node: GROUND, From Node: n1, Unit: V, Type: B.
- Output: iin**: Mode: I, To Node: n1d,t, From Node: n1, Unit: I, Type: B.
- Output: vout**: Mode: V, + Node: n2, - Node: GROUND, From Node: n2d,t, Unit: V, Type: B.
- Output: iout**: Mode: I, To Node: n2d,t, From Node: n2, Unit: I, Type: B.
- Input: freq**: Mode: F, Sweep Type: HB, Sweep Order: 2, Value: 2.400G, Order: 8.

Red arrows indicate the mapping from the netlist to these simulation components. A large blue bracket on the left side of the netlist is labeled "ICCAP specific input". A blue arrow points from the netlist to the "ADS netlist" text box.

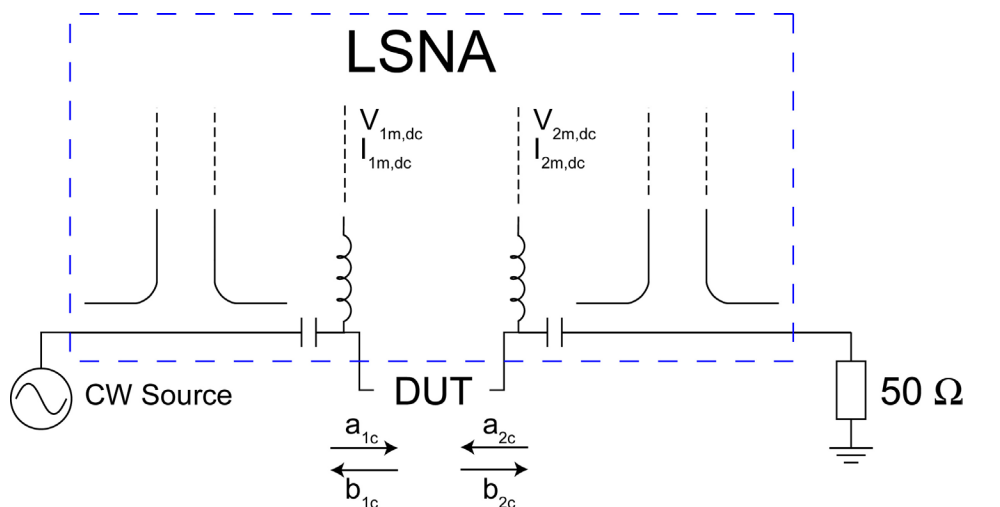
ADS netlist. Used, a.o., to impose the measured impedance to the output of the transistor in simulation

Use of LSNA measurements for simulation (1/2)

Measurements



RF de-embedding

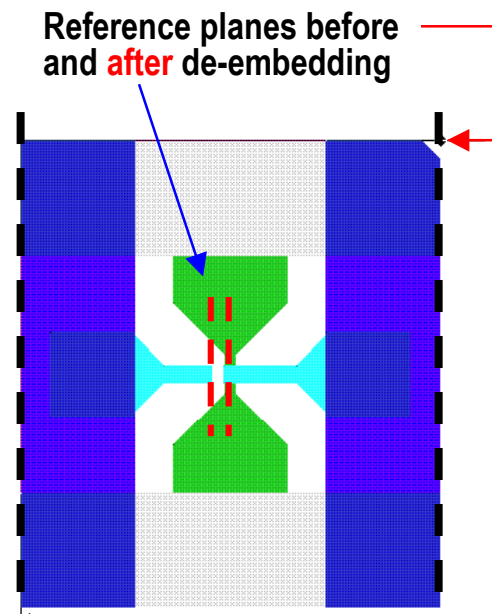


$$\begin{matrix} a_{1c} & b_{1c} \\ a_{2c} & b_{2c} \end{matrix} \iff \begin{matrix} V_{1c} & i_{1c} \\ V_{2c} & i_{2c} \end{matrix} \left. \vphantom{\begin{matrix} a_{1c} & b_{1c} \\ a_{2c} & b_{2c} \end{matrix}} \right\} @ f_0, 2*f_0, \dots$$

calibrated

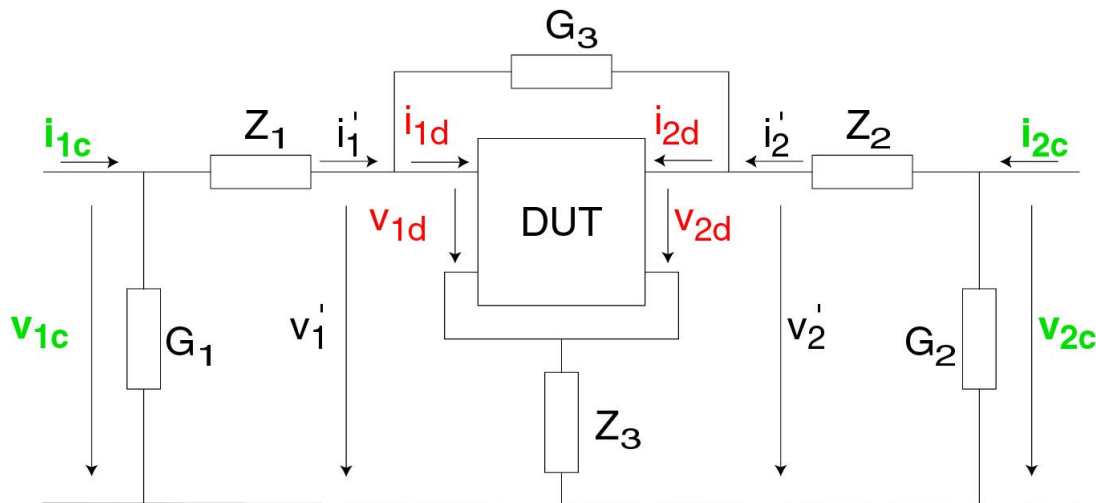
$$\begin{matrix} V_{1m,dc} & I_{1m,dc} \\ V_{2m,dc} & I_{2m,dc} \end{matrix} \implies \begin{matrix} V_{1,dc} & I_{1,dc} \\ V_{2,dc} & I_{2,dc} \end{matrix}$$

LSNA accounts for cable resistances

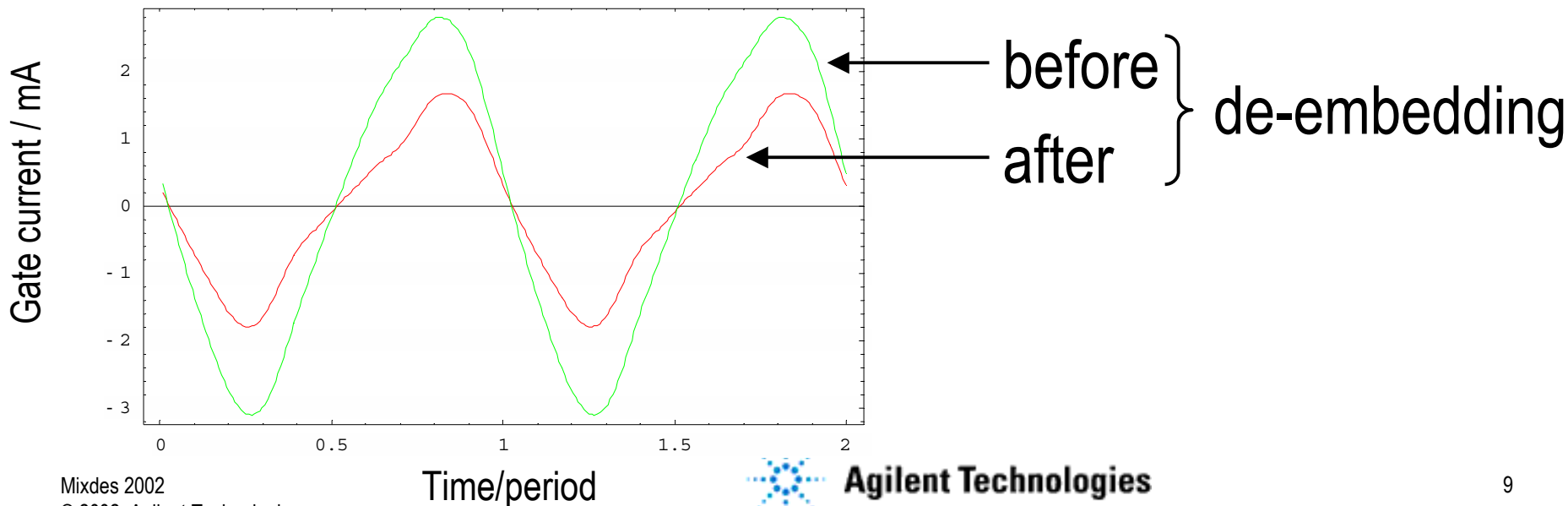


$$\begin{matrix} V_{1c} & i_{1c} \\ V_{2c} & i_{2c} \end{matrix} \implies \begin{matrix} V_{1d} & i_{1d} \\ V_{2d} & i_{2d} \end{matrix}$$

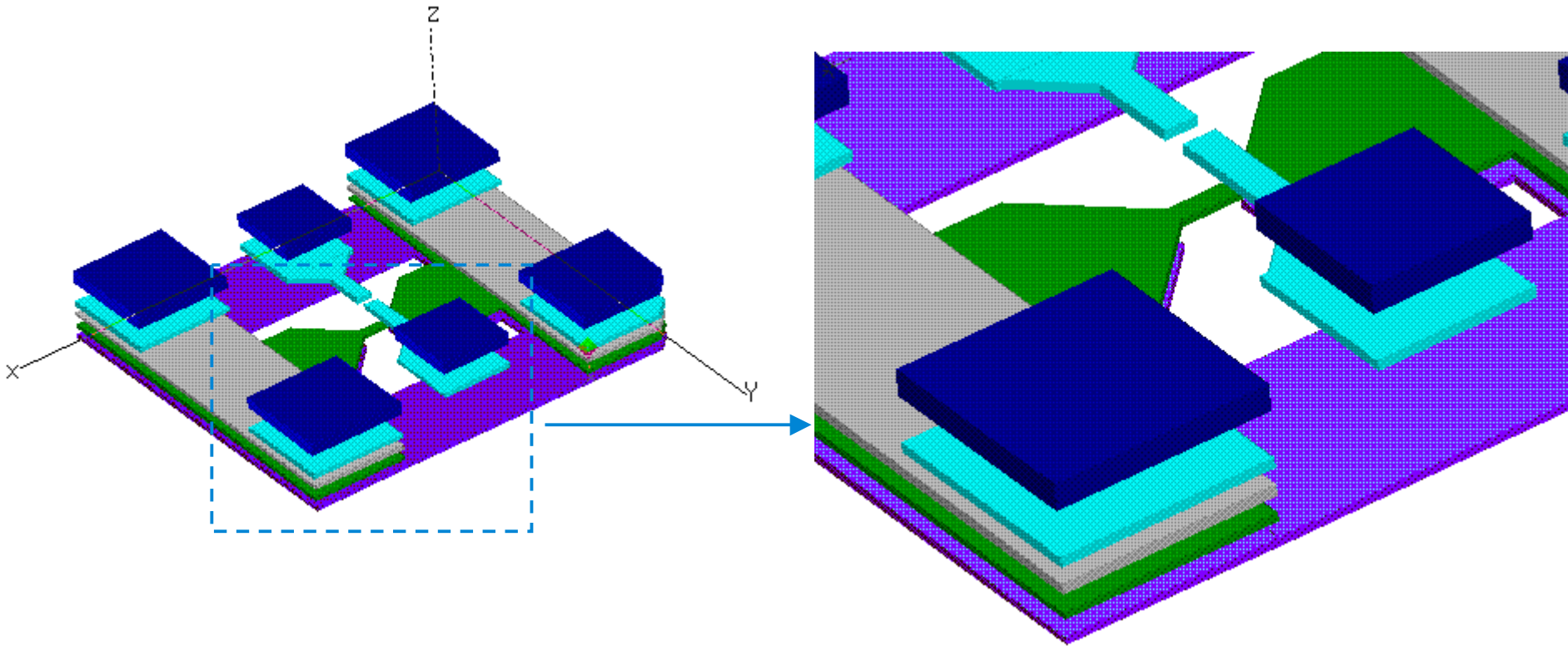
De-embedding intermezzo (1/2)



Equivalent circuit of the RF test-structure, including the DUT and layout parasitics



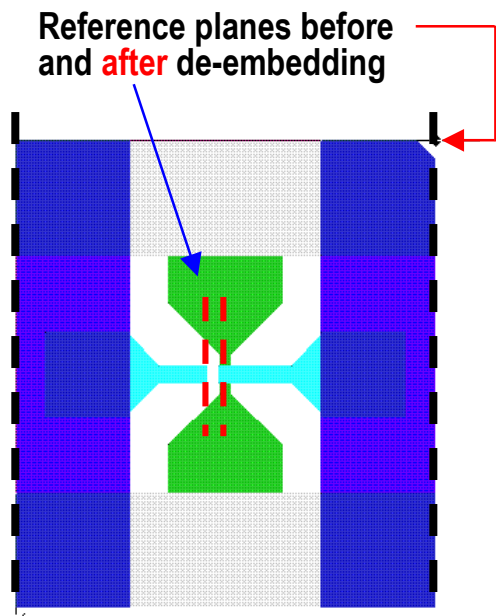
De-embedding intermezzo (2/2)



Detailed view on the layout of the RF MOSFET
for minimum influence of pad parasitics

Use of LSNA measurements for simulation (2/2)

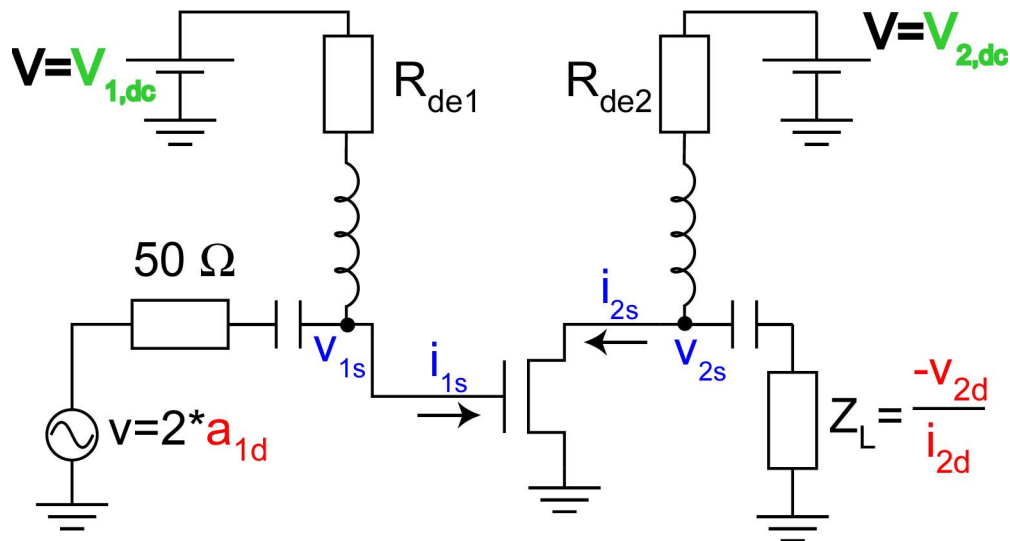
RF de-embedding



$$\begin{matrix} V_{1c} & i_{1c} \\ V_{2c} & i_{2c} \end{matrix} \Rightarrow \begin{matrix} V_{1d} & i_{1d} \\ V_{2d} & i_{2d} \end{matrix}$$



Simulations



Compare measurements:

$$\begin{matrix} V_{1d} & i_{1d} \\ V_{2d} & i_{2d} \end{matrix}$$

with simulations:

$$\begin{matrix} V_{1s} & i_{1s} \\ V_{2s} & i_{2s} \end{matrix}$$

R_{de1} and R_{de2} are de-embedding resistances (in dc path)
The load impedance Z_L at $f=n*f_0$ equals 50Ω if $a_{2n} < -50$ dBm

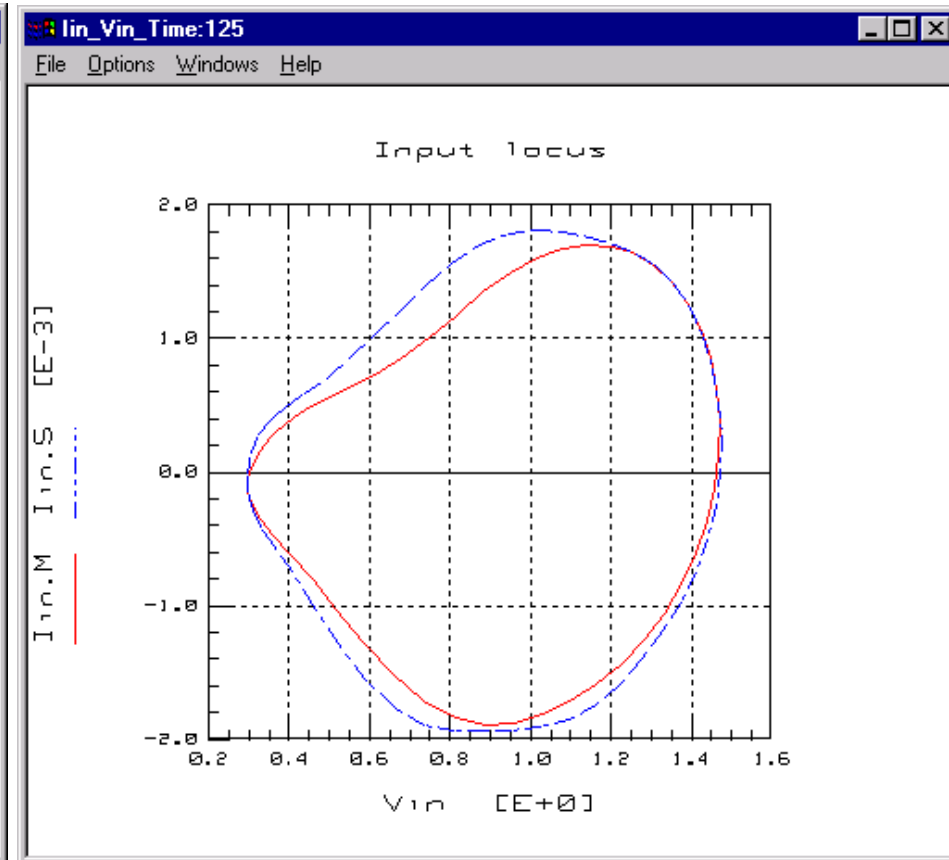
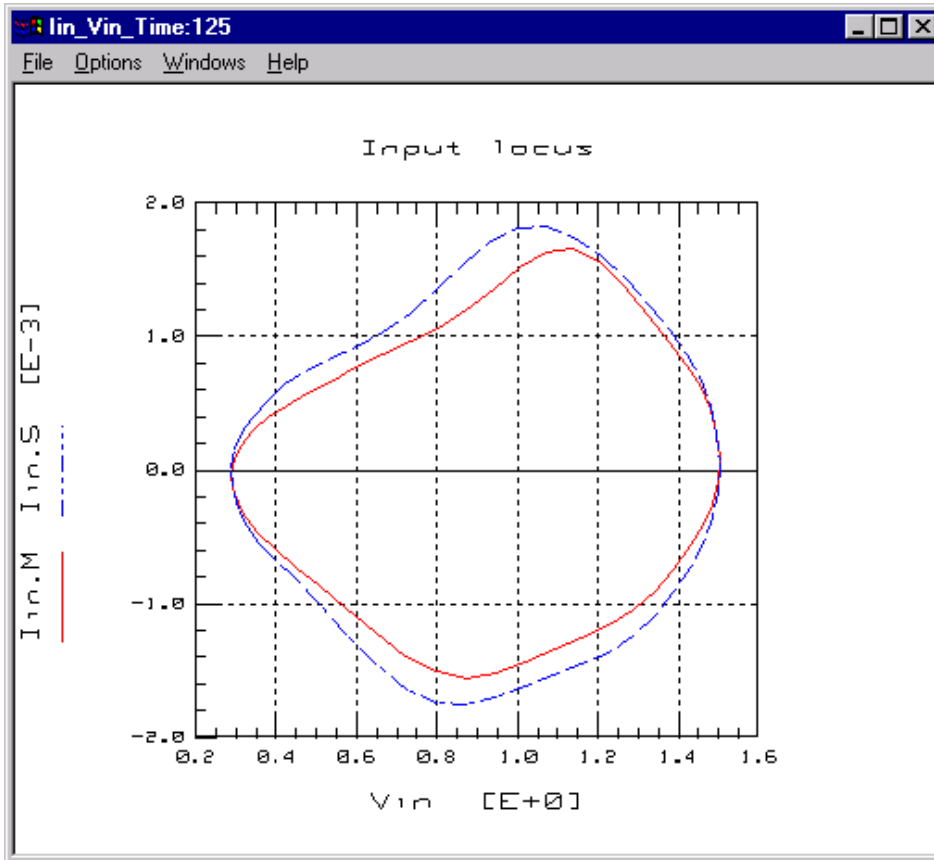


Input capacitance behaviour

$$V_{ds,dc} = 0.3 \text{ V}$$

$$V_{gs,dc} = 0.9 \text{ V}$$

$$V_{ds,dc} = 1.8 \text{ V}$$

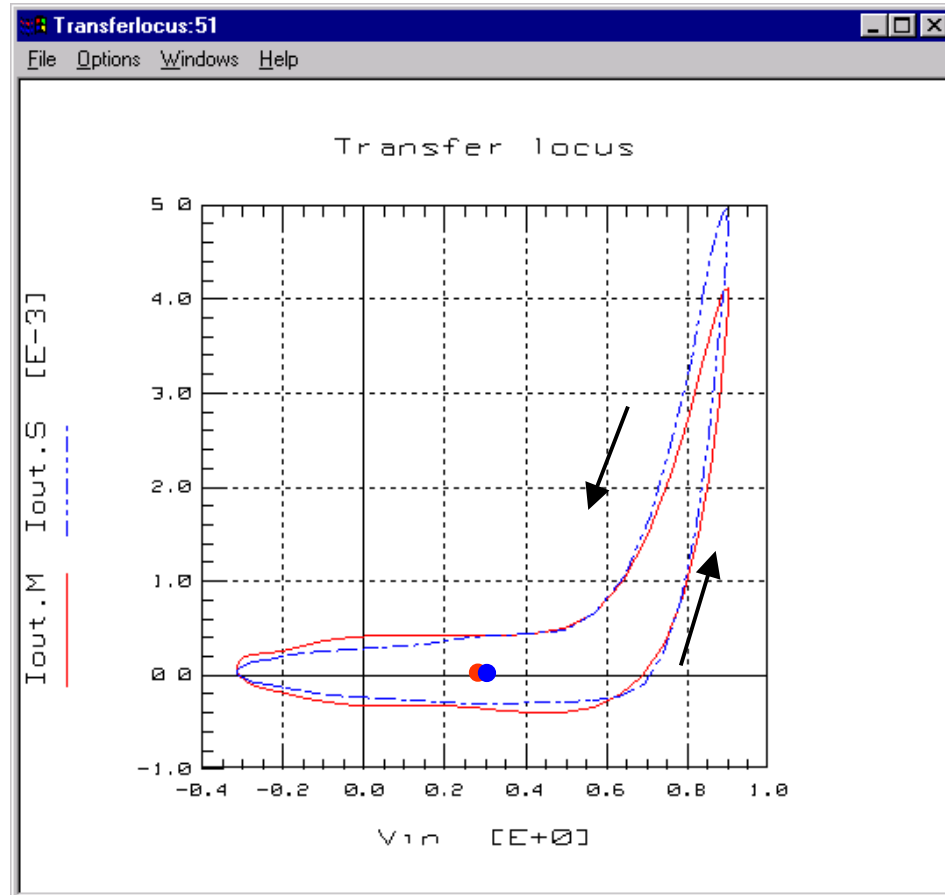
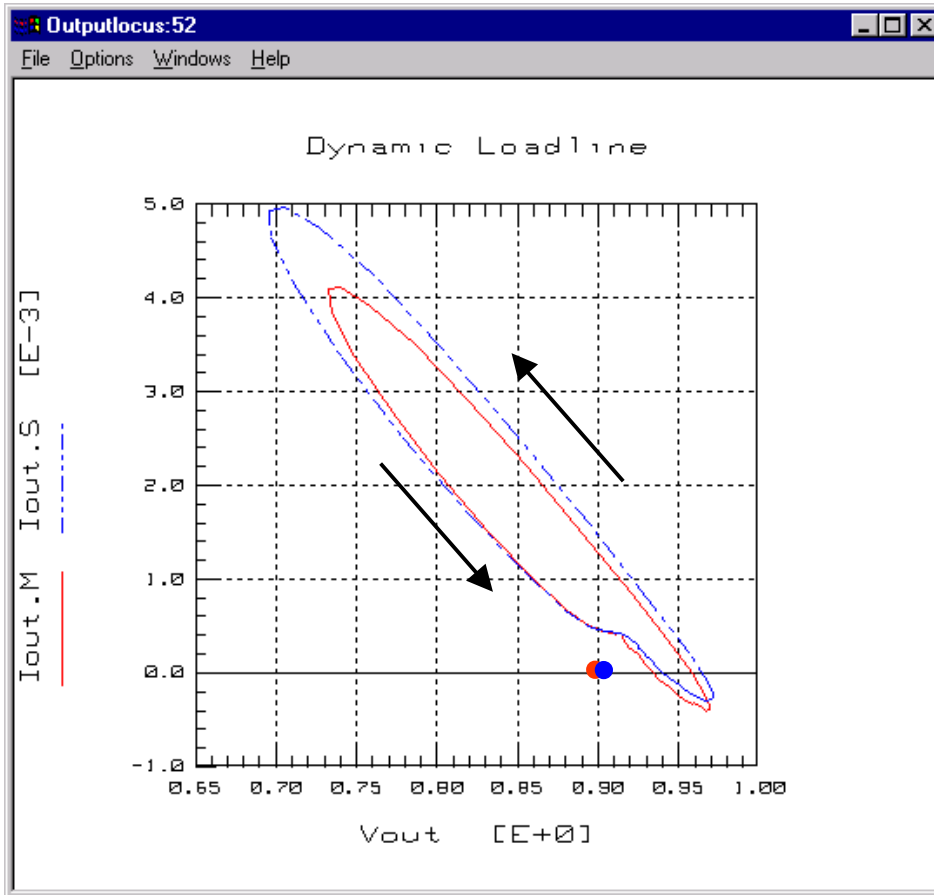


Input loci turn clockwise, conform $i=C \cdot dv/dt$

Dynamic loadline & transfer characteristic

$$V_{ds,dc} = 0.9 \text{ V}$$

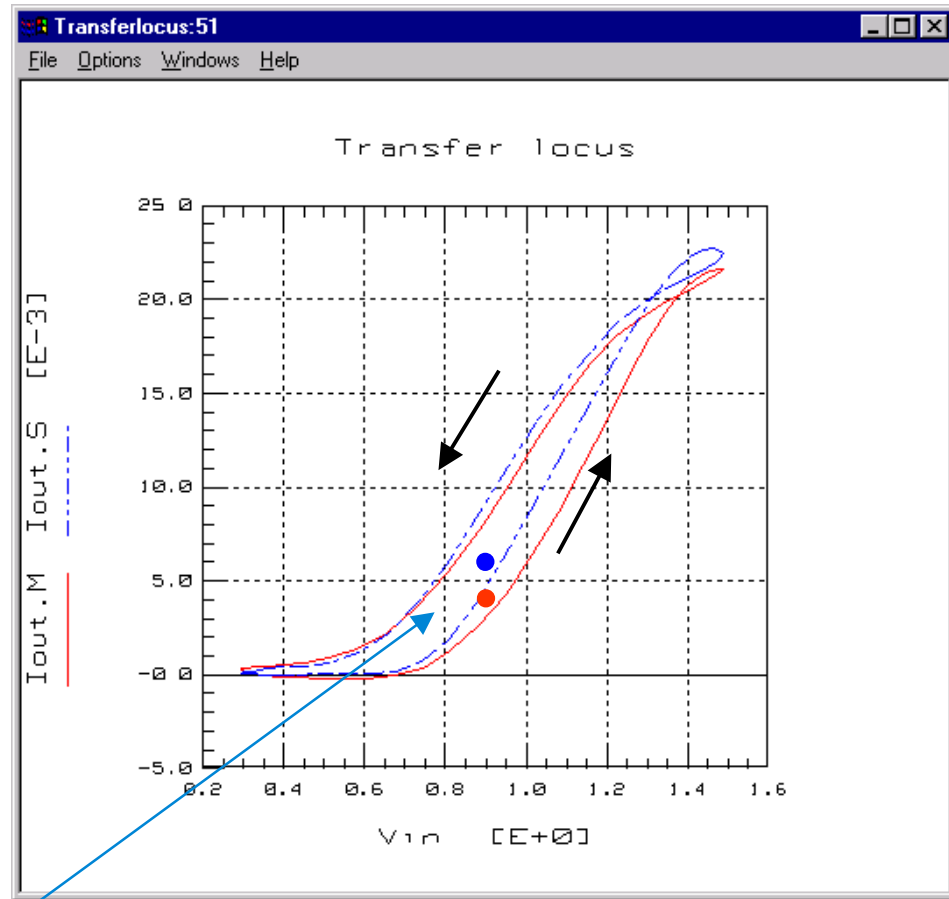
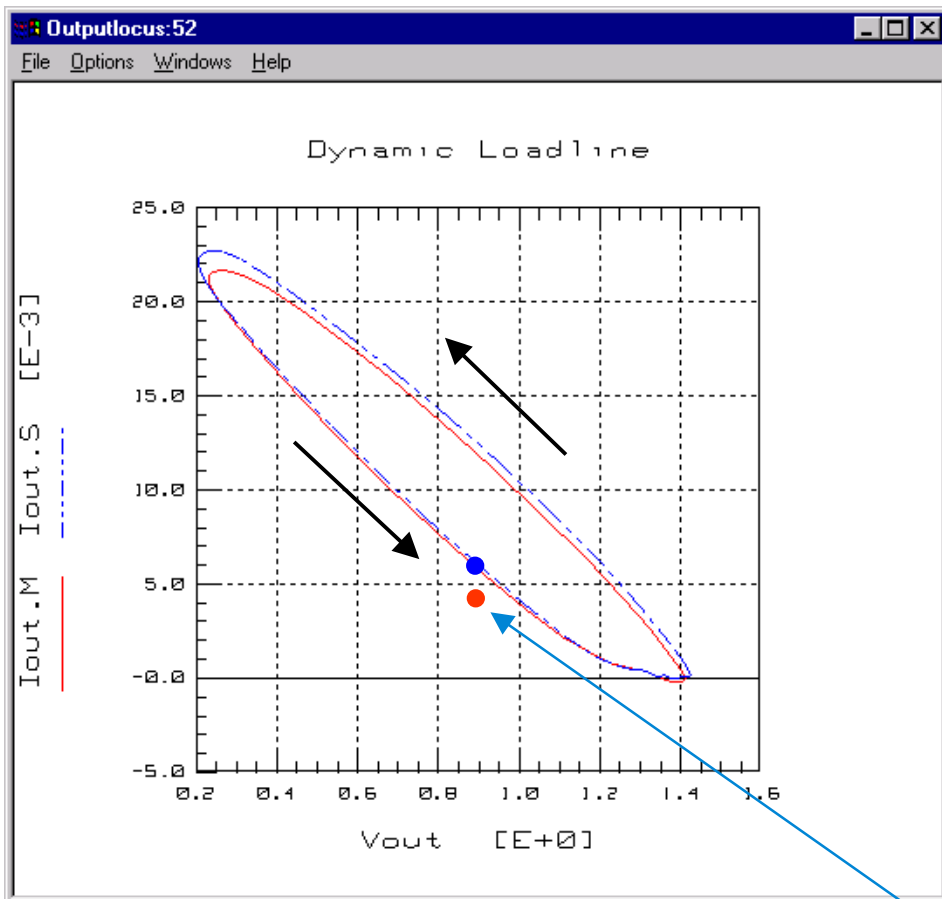
$$V_{gs,dc} = 0.3 \text{ V}$$



Dynamic loadline & transfer characteristic

$$V_{ds,dc} = 0.9 \text{ V}$$

$$V_{gs,dc} = 0.9 \text{ V}$$

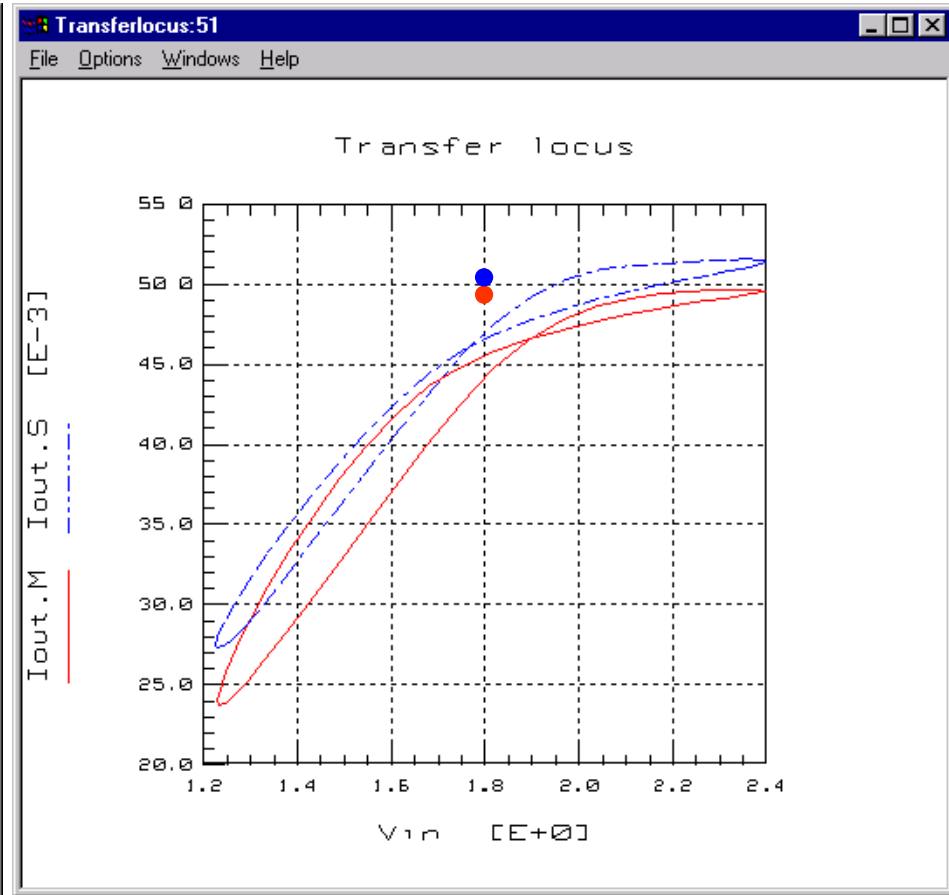
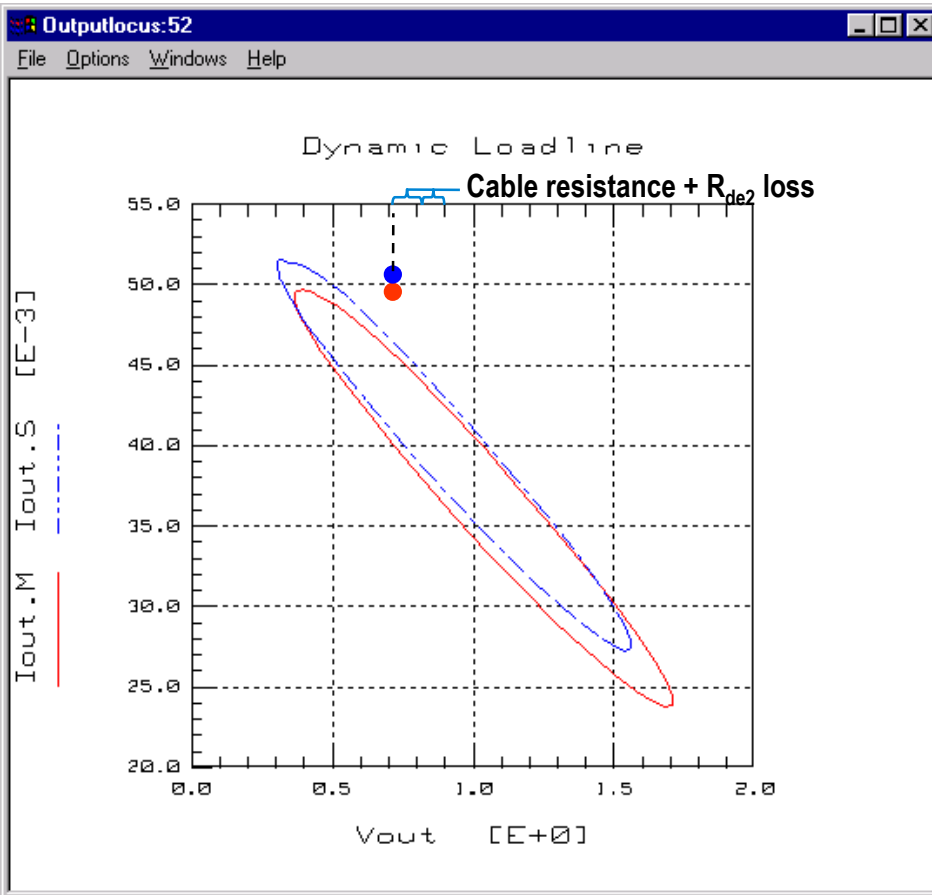


DC operating point if RF
not present \Rightarrow self-biasing

Dynamic loadline & transfer characteristic

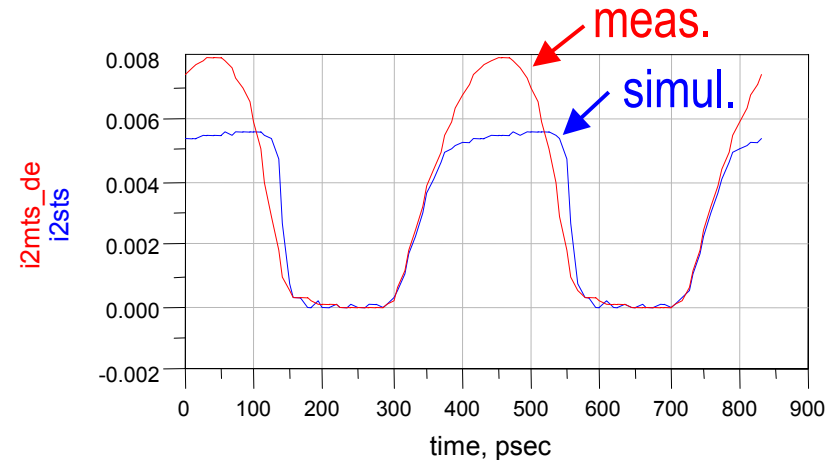
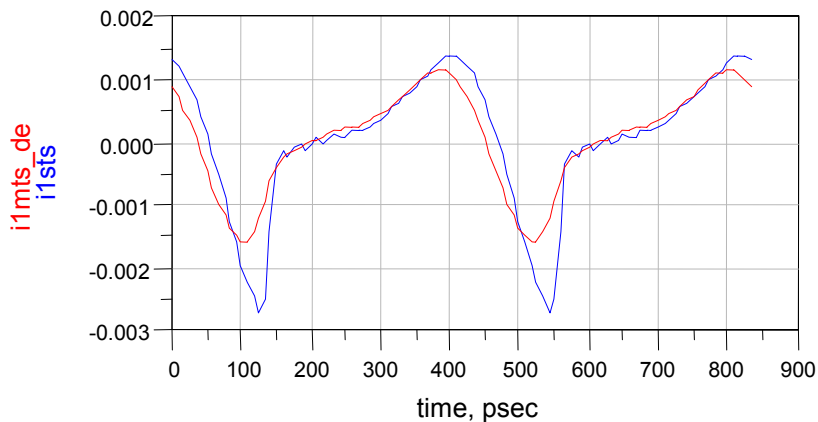
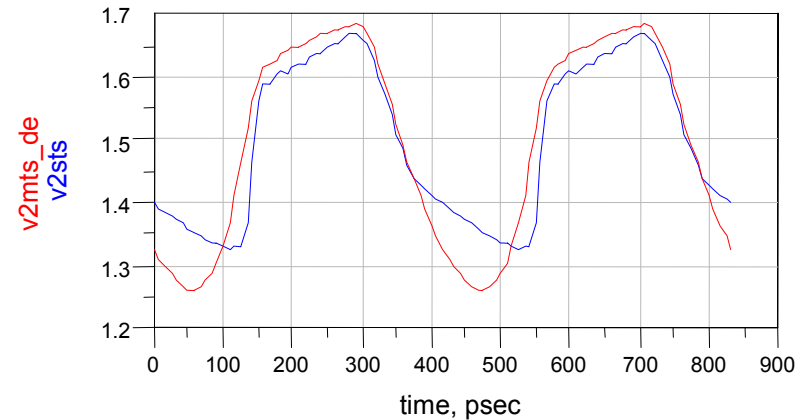
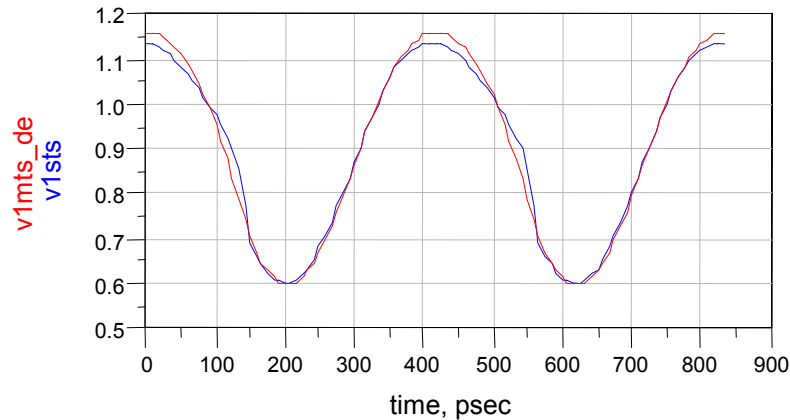
$$V_{ds,dc} = 0.9 \text{ V}$$

$$V_{gs,dc} = 1.8 \text{ V}$$



Intermezzo (1/2): extrapolation example SiGe HBT

Model parameters extracted using DC measurements up to 1 V



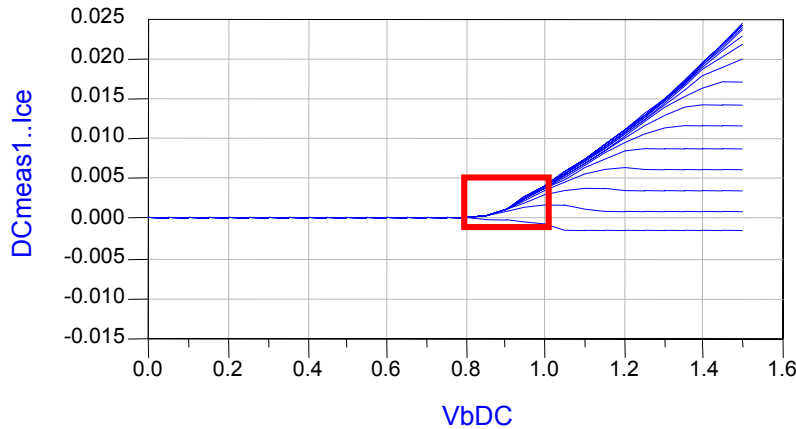
SiGe HBT

$V_{be} = 0.9$ V; $V_{ce} = 1.5$ V; $P_{in} = -6$ dBm; $f_0 = 2.4$ GHz

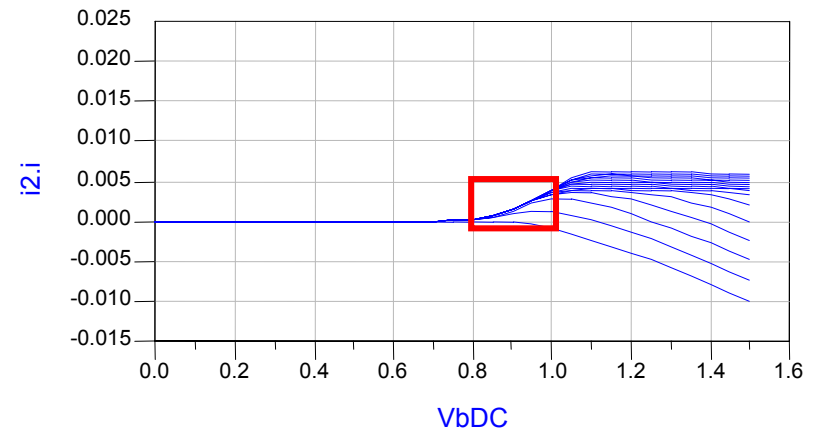
Intermezzo (2/2): extrapolation example SiGe HBT

Measured and simulated DC characteristics

SiGe HBT - DC characteristics



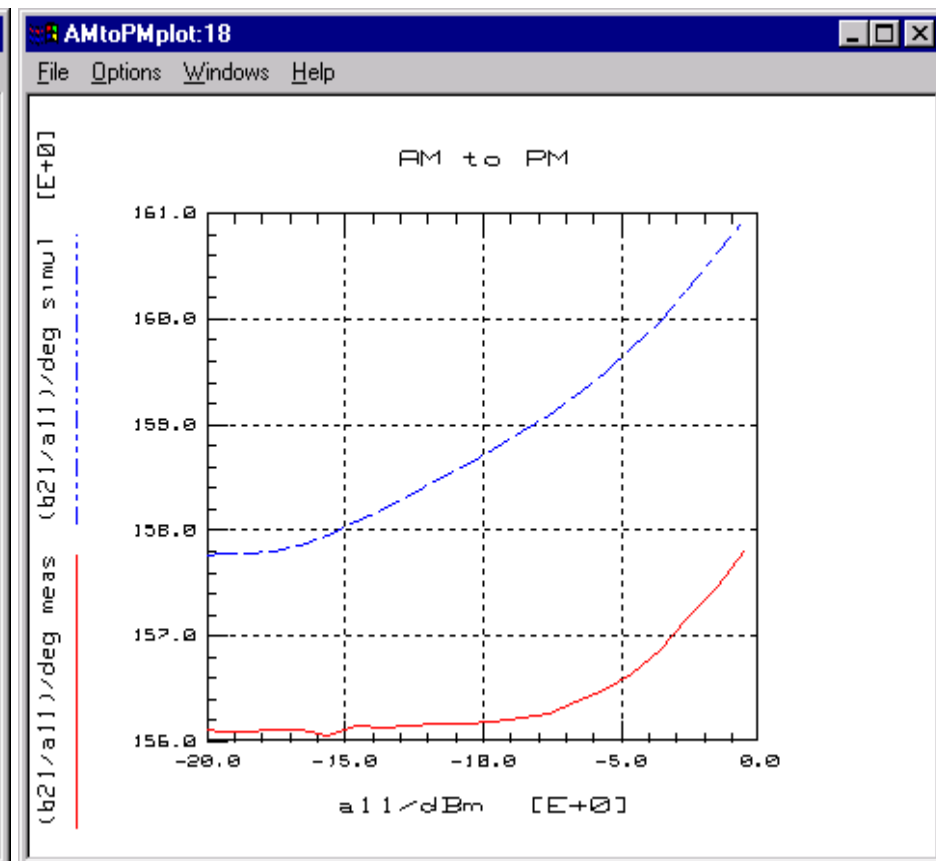
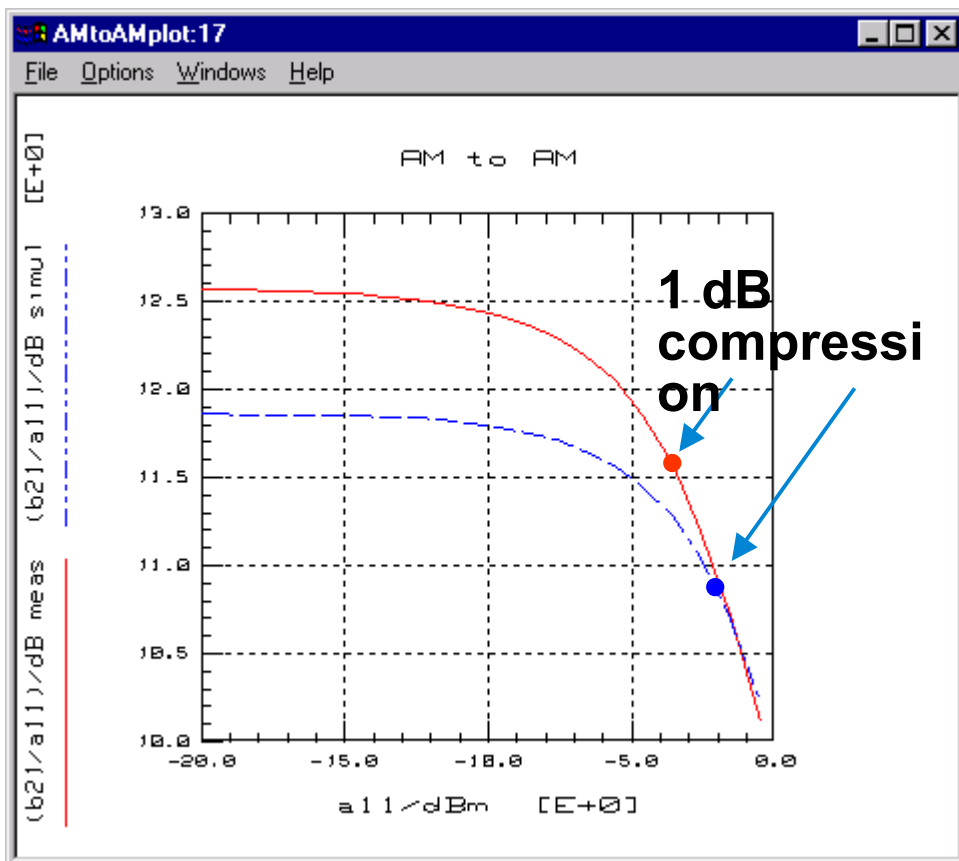
Measurement



Simulation

Alcatel Microelectronics and the Alcatel SEL
Stuttgart Research Center teams are acknowledged
for providing these data.

AM to AM (gain) and AM to PM versus input power



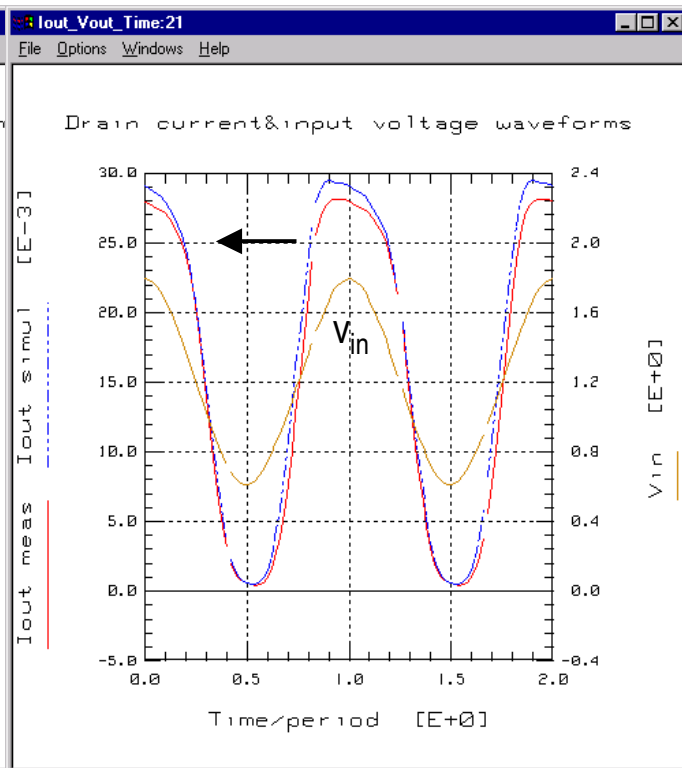
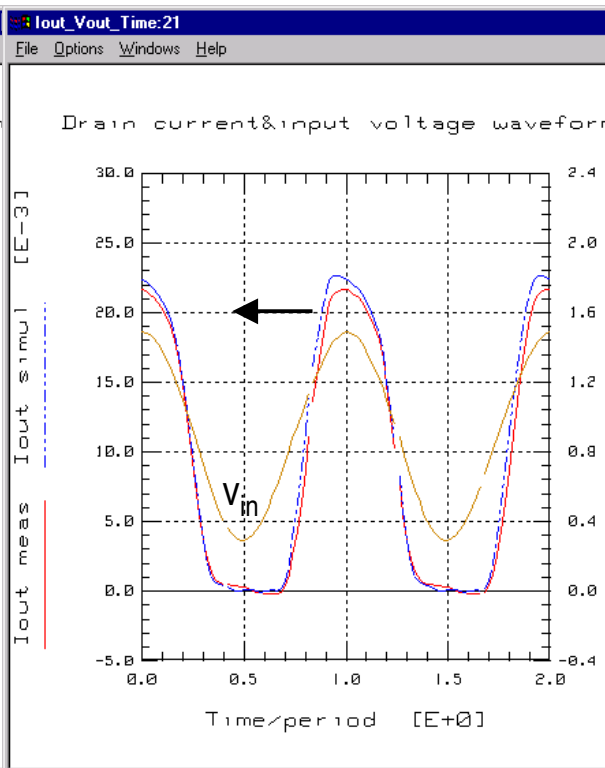
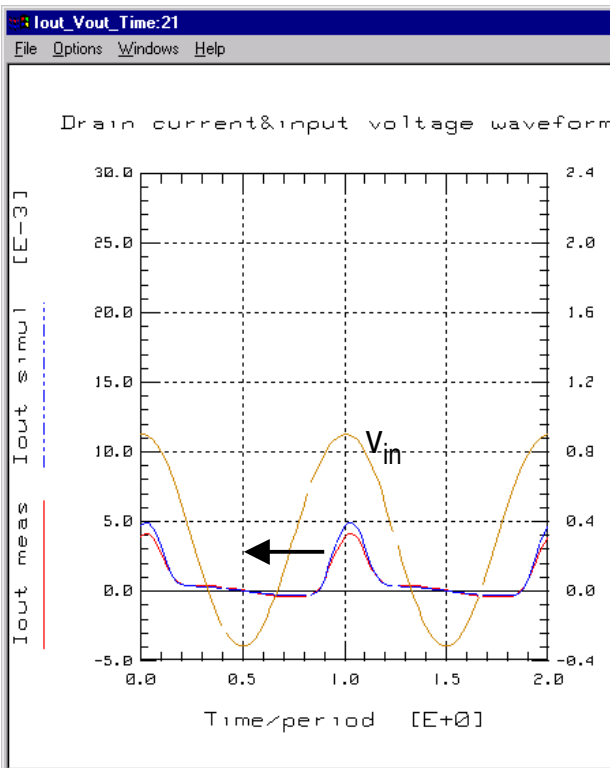
$$V_{ds,dc} = V_{gs,dc} = 1.2 \text{ V}$$

Drain current & gate voltage time domain waveforms

“Class C”

Class AB

Class A



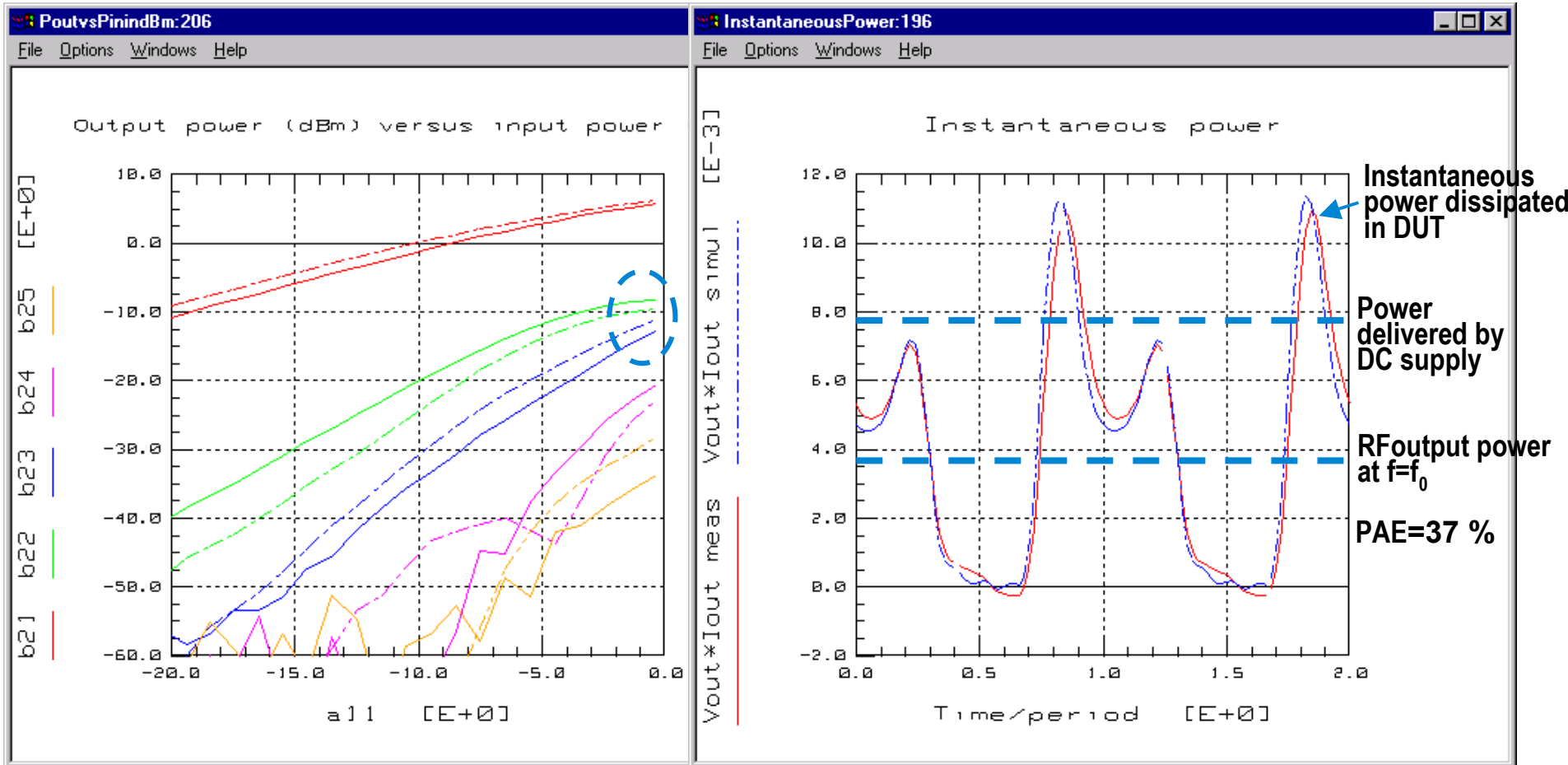
$$V_{gs,dc} = 0.3 \text{ V}$$

$$V_{gs,dc} = 0.9 \text{ V}$$

$$V_{gs,dc} = 1.2 \text{ V}$$

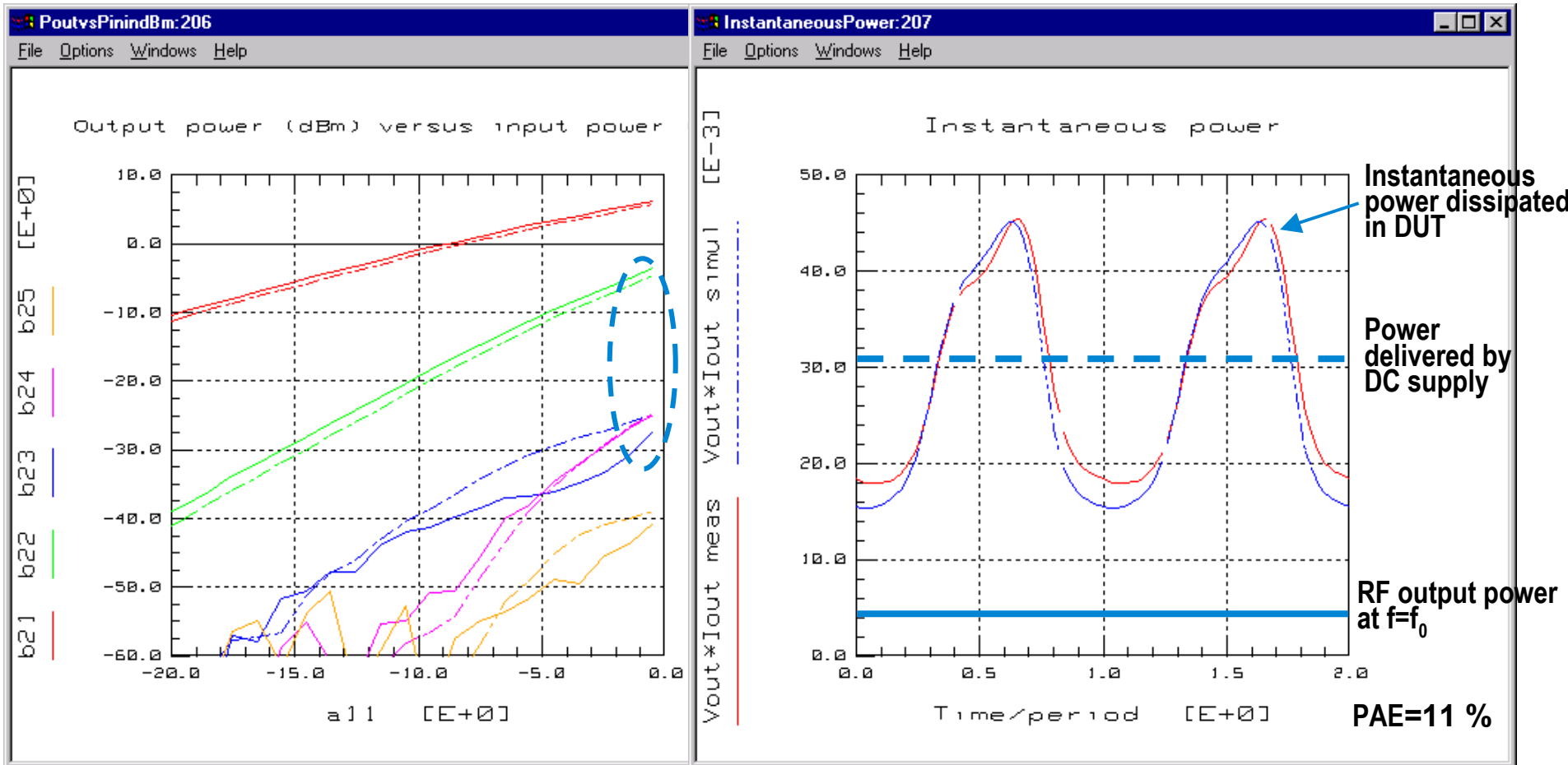
$$V_{ds,dc} = 0.9 \text{ V}$$

Effect of operating regime on dissipated power in the DUT, load, and DC power supply — class AB



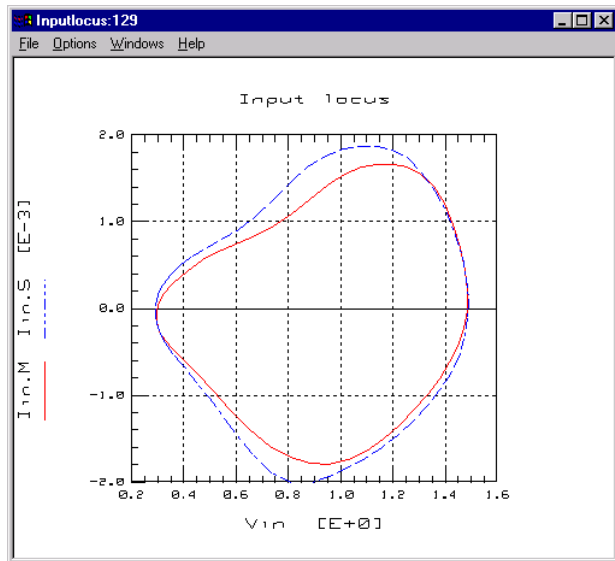
$V_{ds,dc} = 0.9 \text{ V}, V_{gs,dc} = 0.9 \text{ V}$

Effect of operating regime on dissipated power in the DUT, load, and DC power supply — “class A”

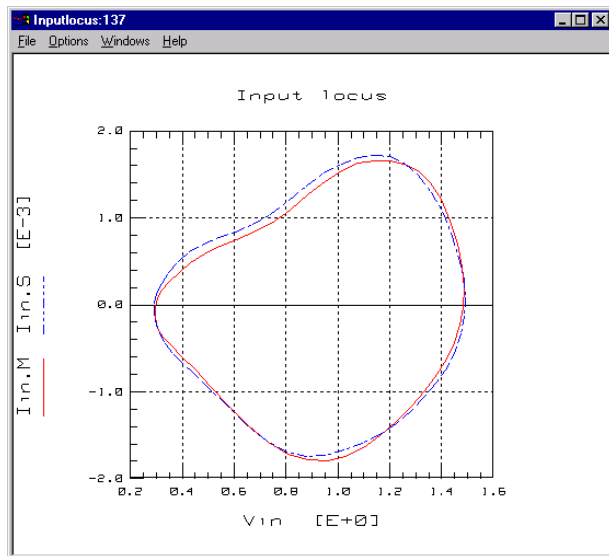
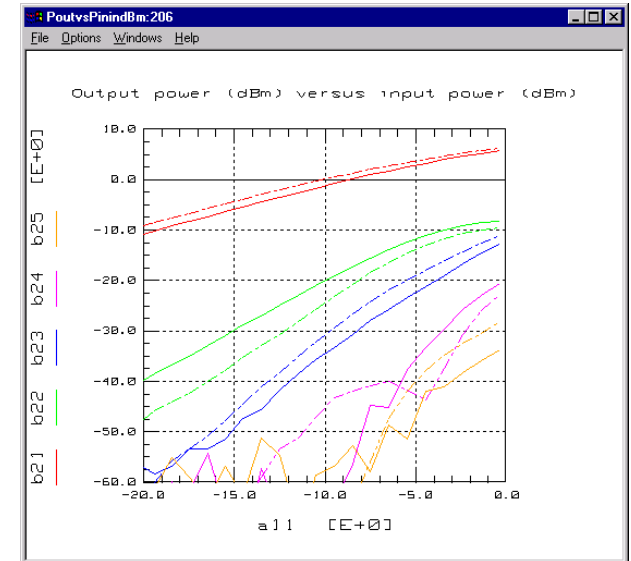


$V_{ds,dc} = 0.9 \text{ V}, V_{gs,dc} = 1.8 \text{ V}$

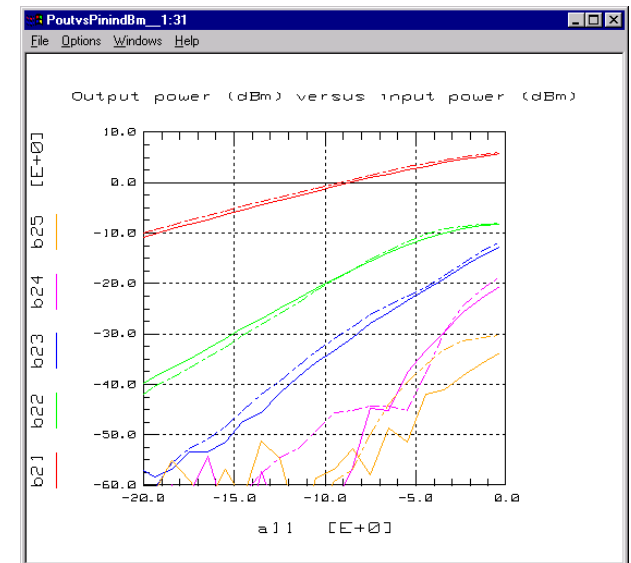
Tuning of model parameters to LSNA measurements



before



after



LSNA measurements in device modelling

Conclusions:

- Unique tool for **complete** large-signal model accuracy assessment under **realistic** RF or microwave signals
 - information on amplitude and phase
- Reduce number of design cycles and reduce manufacturing costs through **better** device models, thus more optimal designs
- **Optimize** model parameters to LSNA measurements
- **Benchmark** various device models, e.g.,
 - BSIM, MM11, EKV, ...
 - Gummel-Poon, VBIC, MEXTRAM, HICUM, ...
- Build **confidence** in your model

Contact

- For info on LSNA technology, visit <http://www.agilent.com/find/lсна>
- Soon, a measurement and consulting service related to Large-Signal Network Analyzer Technology will be available through the 'NMDG' group in Belgium. For info, you need to contact NMDG directly at
email: **Marcus_Vandenbossche@agilent.com**, or
tel.: **+32 - 3 - 890 46 16**