Multi-Level Modeling of Deep-Submicron MOSFETs and ULSI Circuits

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Presentation Outline

Overview	***Challenges in multi-level modeling***: from process through device/circuit to systems
Xsim Compact Model	***A technology-based compact model***: General features, data requirement, parameter extraction, 0.18-μm technology prediction, process correlation
XSIM Mixed-Mode Simulator	***An implicit mixed-signal simulator***: Subcircuit expansion approach, Dynamic circuit partitioning and mode switching, Dynamic-delay model
DOUST Parameter Extraction	***Xsim–DOUST–XSIM modeling environment***: Design and Optimization of Ultra-Small Transistors Multi-level modeling with dual-representation
Conclusion	Summary of our approach to multi-level modeling

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Challenges in Compact Modeling and Circuit Simulation

- **ITRS (2001): one of the difficult challenges beyond 2007 (< 65 nm) in modeling — *Software Module Integration***
  - "Seamless integration of simulation modules with focus on interplay and interfacing of the modules in order to enhance design effectiveness"
  - *Example*: "A complete simulation chain linking process modeling, device modeling, compact model extraction, and library generation"
- **Real challenges in deep-submicron (DSM) modeling and simulation**
  - ***Experimental challenge***
    - Not in making one "short-channel" DSM transistor
    - But in making millions of the same transistor across different dies/wafers/lots
  - ***Modeling challenge***
    - Not in accurate modeling of one transistor (perfect match to measurement)
    - But in predictive modeling for a given technology and its process fluctuations
  - ***Multi-level circuit simulation challenge***
    - Not in simulating different types of electronic circuits (transistor/gate/block levels)
    - But in combining distinctively different algorithms in one unified simulator and applying to the same circuit described at different levels of abstraction

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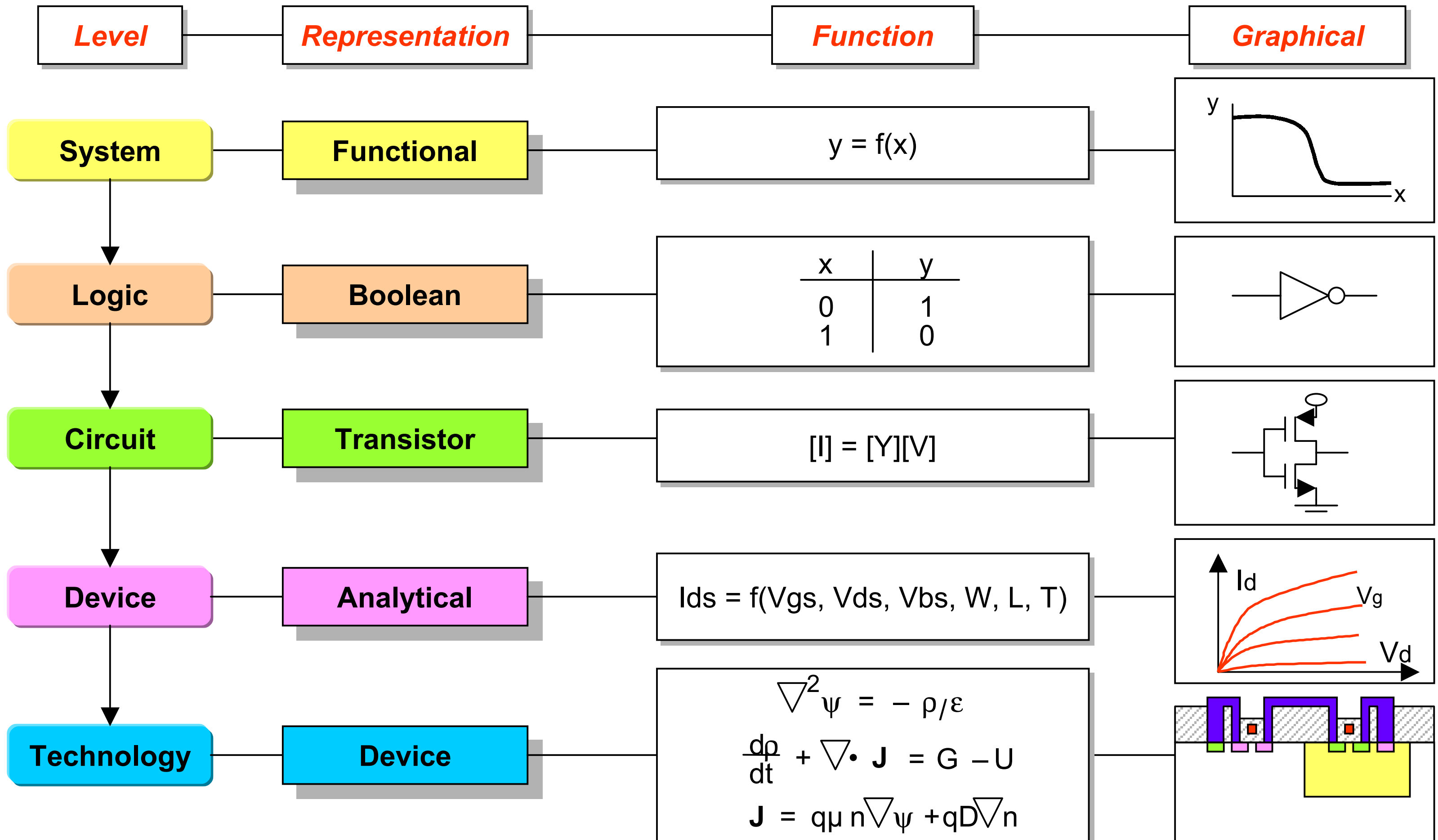
Multi-Level Representation



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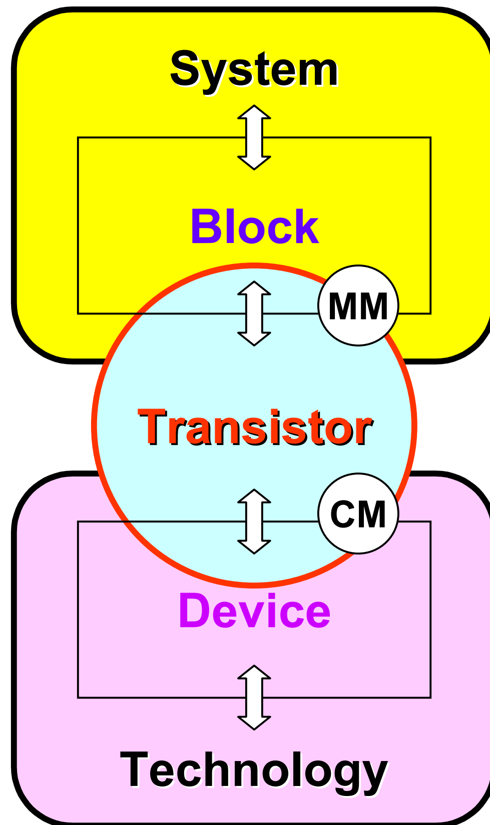
Multi-Level Modeling:
from Technology through Device to System



- How to "propagate" the detailed physics captured at low level to higher-level abstraction?
- Two keys to the solution:
  - ***Consistent dual-representation at each level of abstraction***
    - Higher-level model extracted from its lower-level equivalent
    - Compact-model (**CM**) & mixed-mode (**MM**) at device/transistor/circuit level
  - ***Unified single-engine simulator environment***
    - Separate (commercial) simulators are good for their respective areas
    - But lose information when combined

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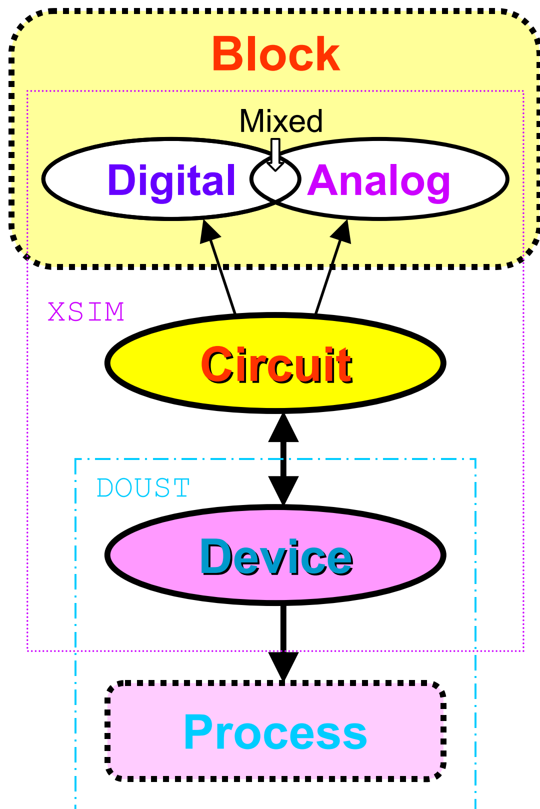
Xsim–DOUST–XSIM:
Compact Model — Extraction — Circuit Simulator



- **Xsim** — ***technology-based compact model***
  - Single-piece, regional, source-referenced, V_t-based compact model
  - Separate technology (V_t–L) / transistor (I–V) modeling and characterization
- **DOUST** — ***parameter-extraction program***
  - Separate process-dependent *fitting* parameters and process-variable *physical* parameters
  - Automated *one-/two-iteration* parameter extraction
- **XSIM** — ***implicit mixed-signal simulator***
  - *Subcircuit-expansion* approach
  - *Automatic* digital/analog circuit partitioning
  - *Dynamic* mode switching with *dynamic delay*

➢ ***Goal*** — *a single-engine, multi-level simulator with true process-variable input for technology development and circuit design / system performance optimization*

Website: `http://www.ntu.edu.sg/home/exzhou/Research/DOUST/`

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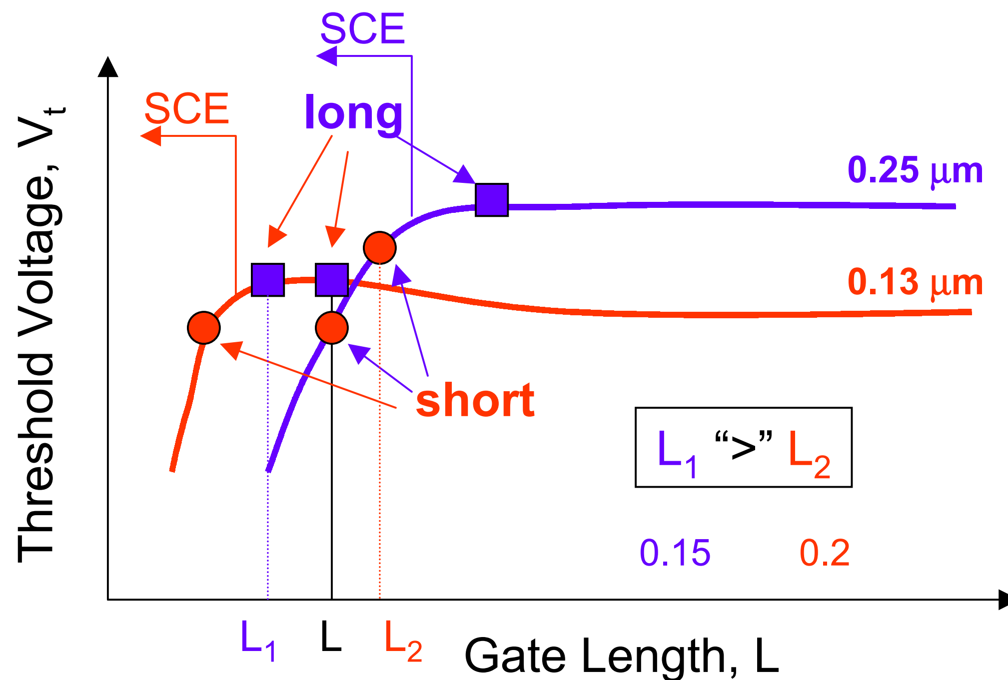
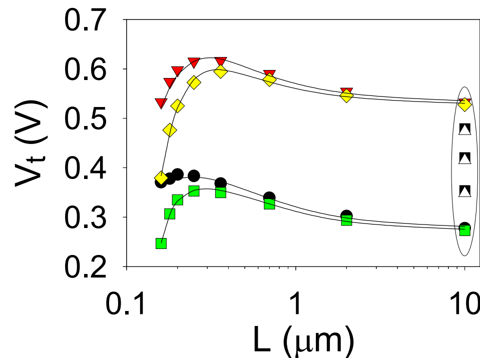
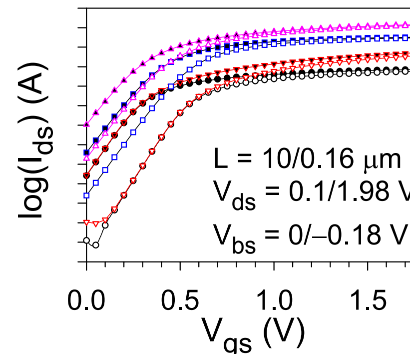
Long-Channel or Short-Channel?

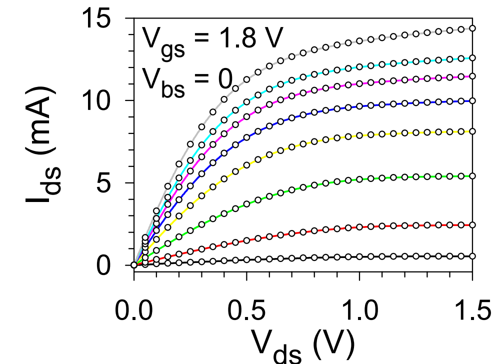
- **Short-channel effect (SCE)** — technology dependent (depends on where the device "sits" on the V_t – L curve, not the actual dimension)
- **Challenge in modeling** — geometry dependence in the SCE regime



Separate Technology (V_t–L) and Transistor (I–V) Modeling & Characterization







- **Technology characterization** — *technology-based model*
  - Model parameters are extracted from the technology data of varying geometry at corner bias.
  - V_t formulation does not require knowledge of μ_{eff} and R_{sd}; effects are contained in the V_t–L data.
  - *Bias coefficients* are used to empirically model the bias-dependent model parameters.

- **Transistor characterization** — *single-transistor-based model*
  - Model parameters are extracted from the electrical data of varying bias at corner geometry.
  - μ_{eff}, R_{sd}, and A_b are physically modeled and extracted at the conditions they are defined.
  - *Geometry coefficients* are used to empirically model the length-dependent model parameters.

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Xsim: Physical Modeling of Linear/Saturation & Drift/Diffusion Currents

$$I_{dsat0} = v_{sat} W C_{ox} \left(V_{gs} - V_t - A_b V_{dsat} \right)$$

$$L_{eff} = L - \Delta_{CD} - 2\sigma x_j$$

$$V_{ds} \rightarrow V_{deff}$$

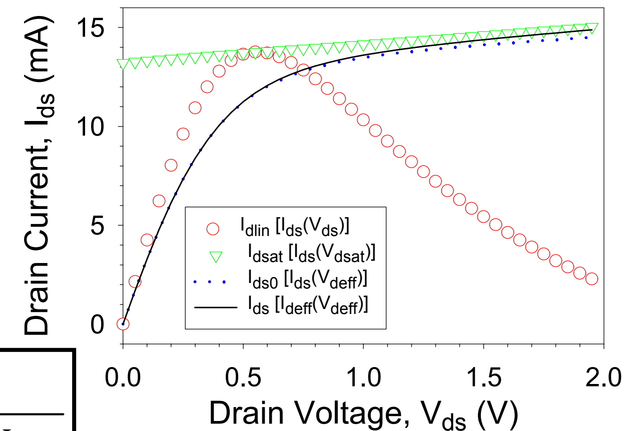
$$I_{ds0} = \mu_{eff} C_{ox} \frac{W}{L_{eff}} \left[\left(V_{gs} - V_t \right) V_{deff} - \frac{A_b}{2} V_{deff}^2 \right]$$

$$V_t = V_{FB} + \phi_s + \gamma_{eff} \sqrt{\phi_{s0} - V_{bs}}$$

$$I_{deff} = \left[1 + \left(V_{ds} - V_{deff} \right) / V_{Aeff} \right] I_{ds0}$$

$$I_{ds0} = \mu_0 C_{ox} \frac{W}{L} \left[\left(V_{gs} - V_t \right) V_{ds} - \frac{A_b}{2} V_{ds}^2 \right]$$

$$I_{ds} = \frac{I_{deff}}{1 + \left(R_{sd} I_{deff} \right) / V_{deff}}$$



$$I_{ds0} = \mu_{eff} C_{ox} \left(W / L_{eff} \right) V_{ge}$$

$$V_{gs} - V_t \rightarrow V_{geff}$$

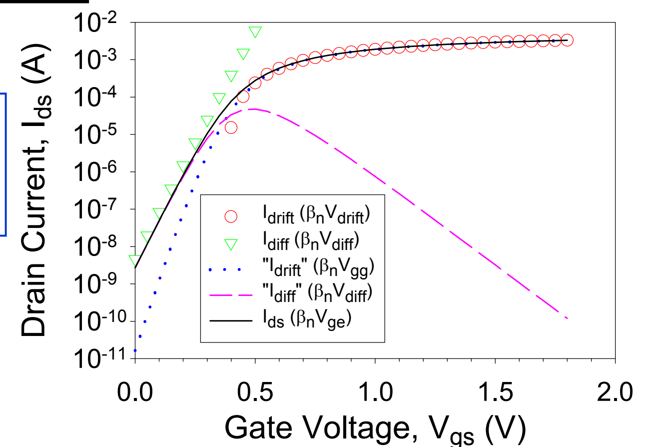
$$V_{geff} V_{de} \rightarrow V_{gg}$$

$$V_{gd} + V_{gg} \rightarrow V_{ge}$$

$$I_{ds0} = \mu_{eff} C_{ox} \frac{W}{L_{eff}} V_{geff} V_{deff} \left(1 - \frac{A_b}{2} \frac{V_{deff}}{V_{geff}} \right)$$

$$I_{ds0} = \mu_{eff} C_{ox} \left(W / L_{eff} \right) V_{gd}$$

$$I_{diff} = \mu_0 C_{ox} \frac{W}{L} v_{th}^2 \left(C_d / C_{ox} \right) e^{\left(V_{gs} - V_t - V_{off} \right) / \left(n v_{th} \right)} \left(1 - e^{-V_{ds}/v_{th}} \right)$$



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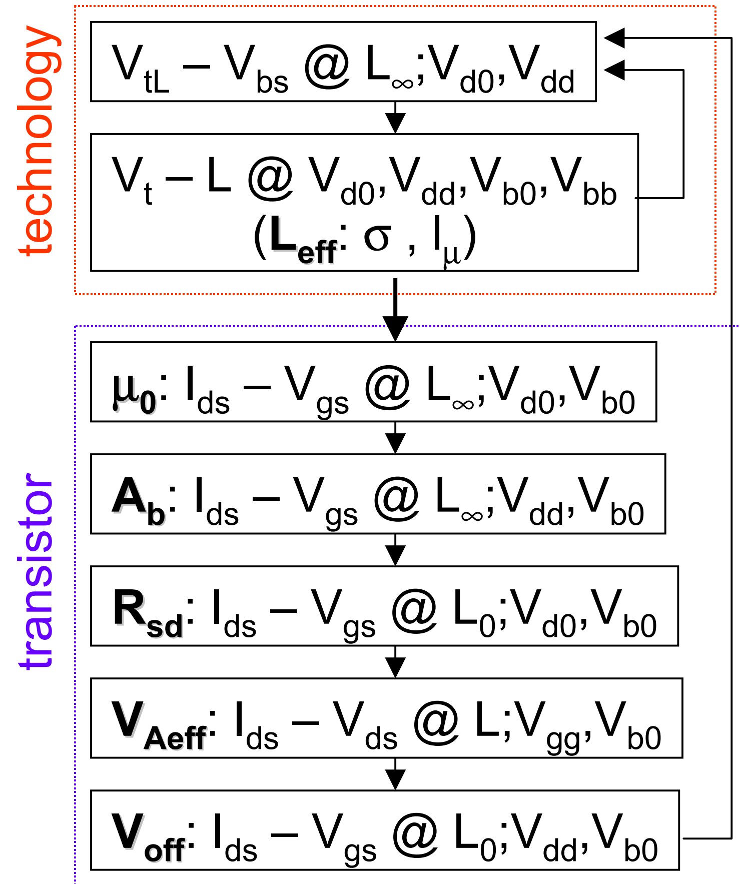
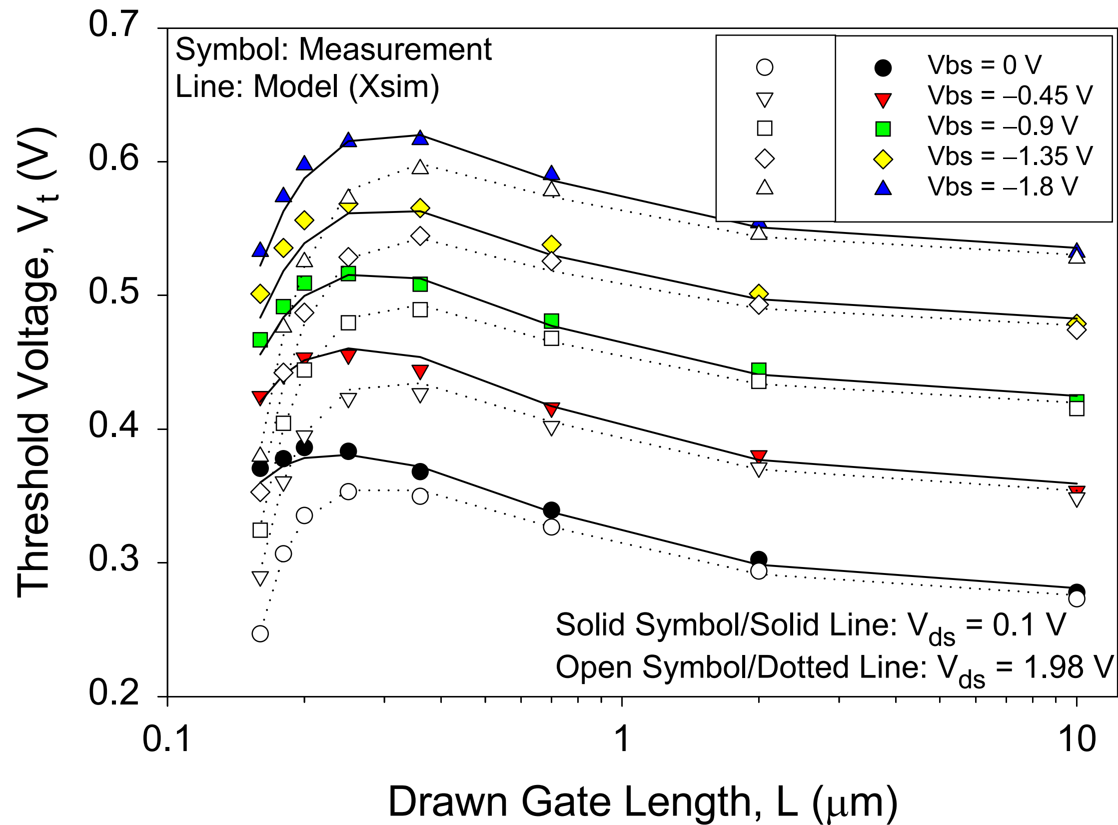
DOUST: Prioritized One-/Two-Iteration Model Parameter Extraction

- **Principle assumptions**
  - Short-channel equations approach long-channel ones
  - Un-extracted parameters should have little effect in the current step of extraction
  - Once extracted, their values should be fixed; subsequent extraction should not affect what have been calibrated
- **Errors involved**
  - Corner conditions not being "wide" enough
  - Switching from simple to full equations
  - ➢ Second iteration using full equations and first-iteration values as initial guess



Technology Prediction on the 0.18-μm Technology

Threshold Voltage Prediction



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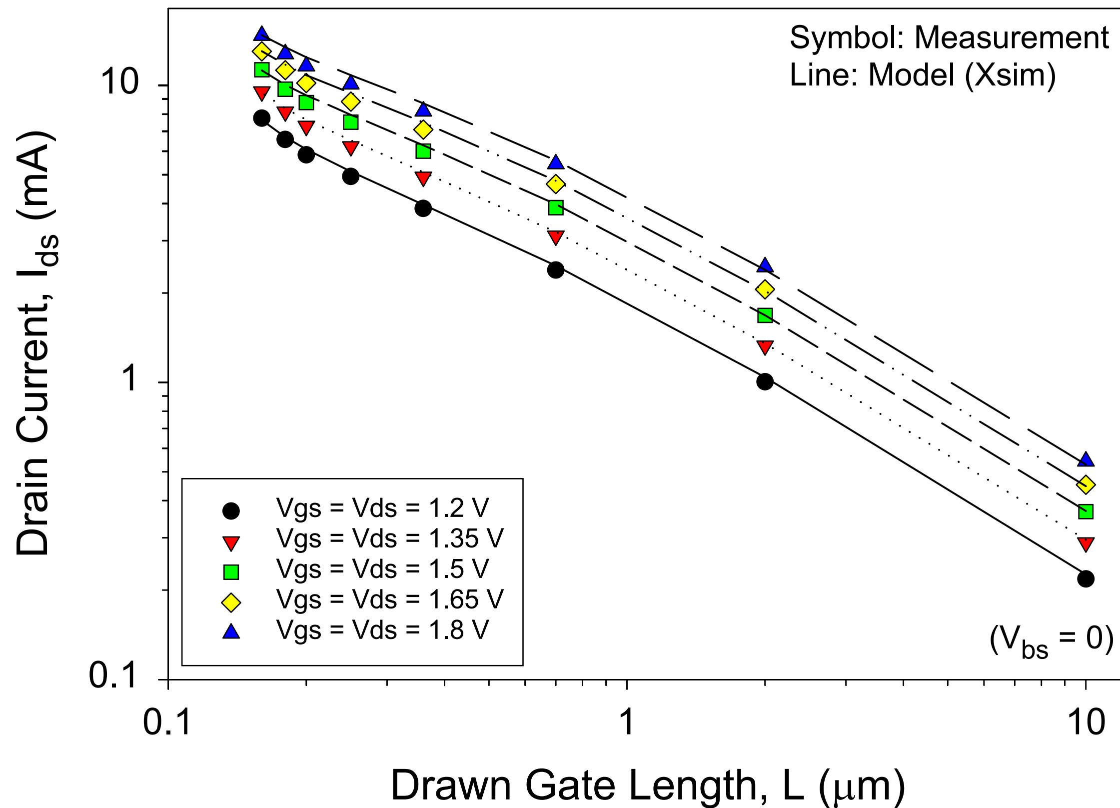
Technology Prediction on the 0.18-μm Technology
Saturation Current Prediction



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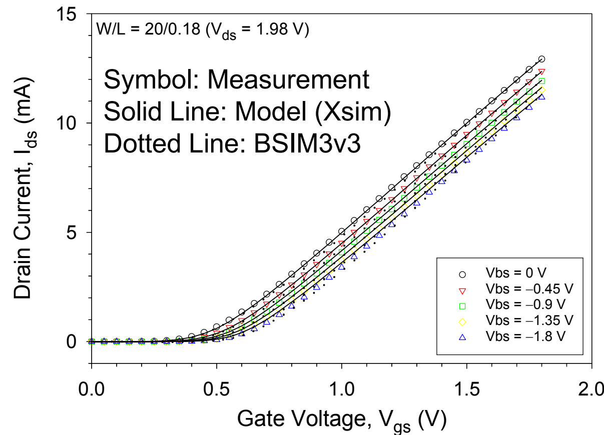
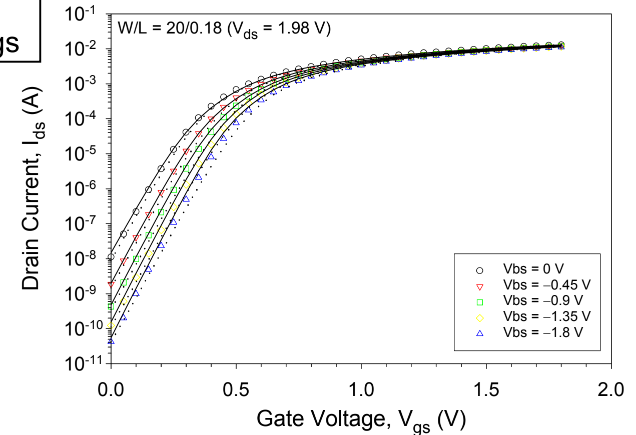
Technology Prediction on the 0.18-μm Technology
Transfer (Gate) Characteristics

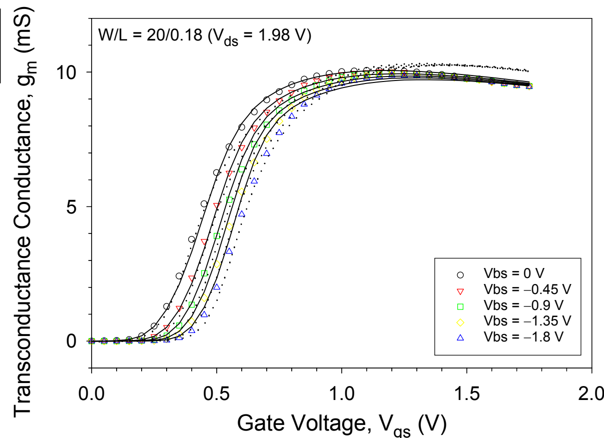
I_{ds}–V_{gs}



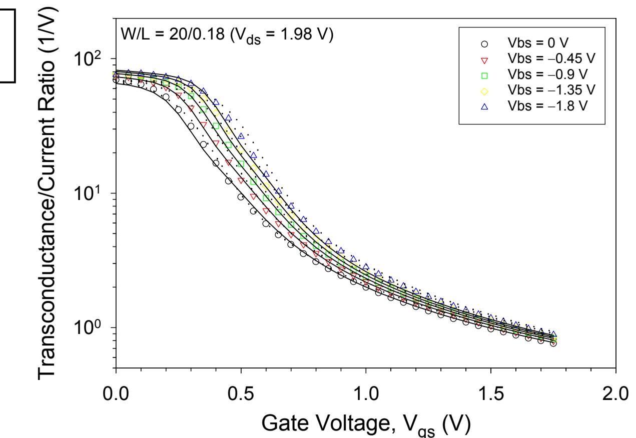
log(I_{ds})–V_{gs}



g_m–V_{gs}



g_m/I_{ds}–V_{gs}



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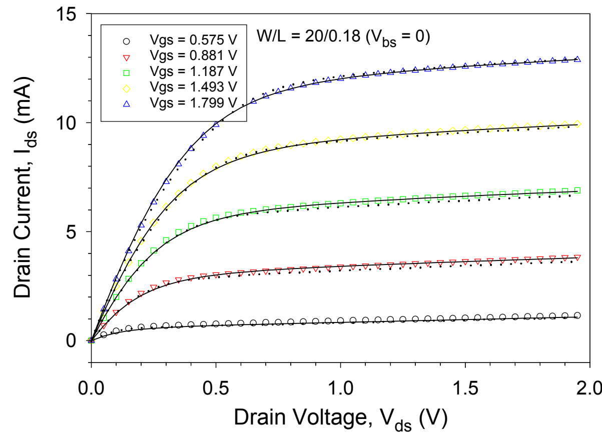
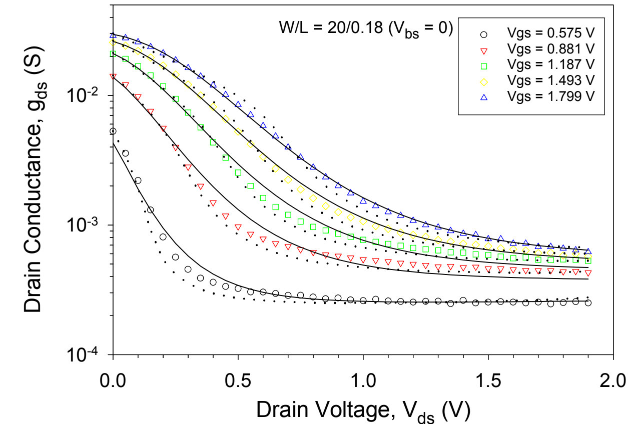
Technology Prediction on the 0.18-μm Technology

Output (Drain) Characteristics

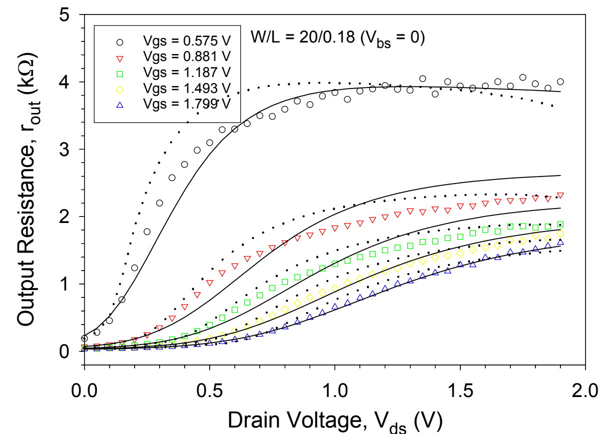
I_{ds}–V_{ds}



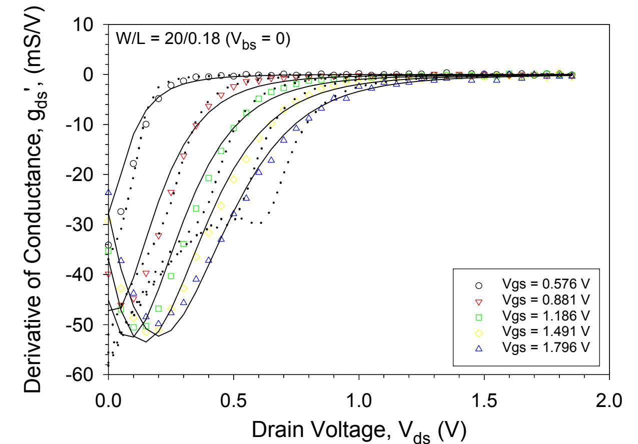
g_{ds}–V_{ds}



r_{out}–V_{ds}



g_{ds}'–V_{ds}



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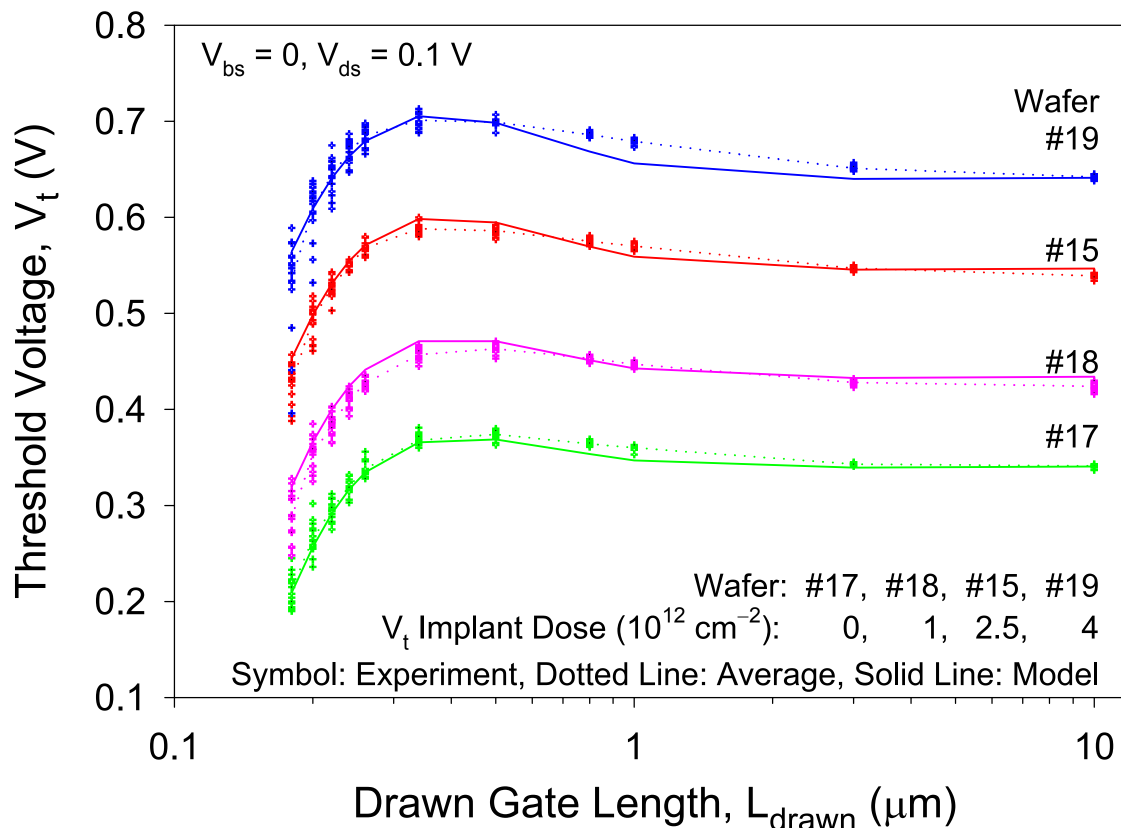
Threshold Voltage Prediction

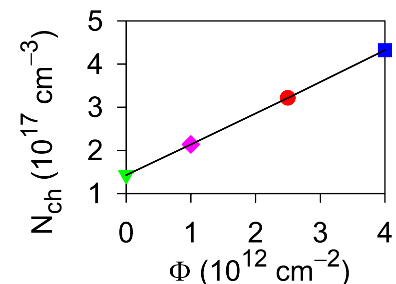
Experimental data measured from 17 sites of split-lot wafers



Process correlation

- Using wafer #15 to calibrate V_t model
- Using long-channel V_t–V_{bs} from wafers #15/17/19 to extract N_{ch} for each wafer
- Correlating N_{ch} to V_t-implant dose Φ with linear approximation
- Predicting V_t–L_{drawn} (especially #18) with Φ as input

$N_{ch} = 1.426 \times 10^{17} + 7.231 \times 10^{4} \Phi$



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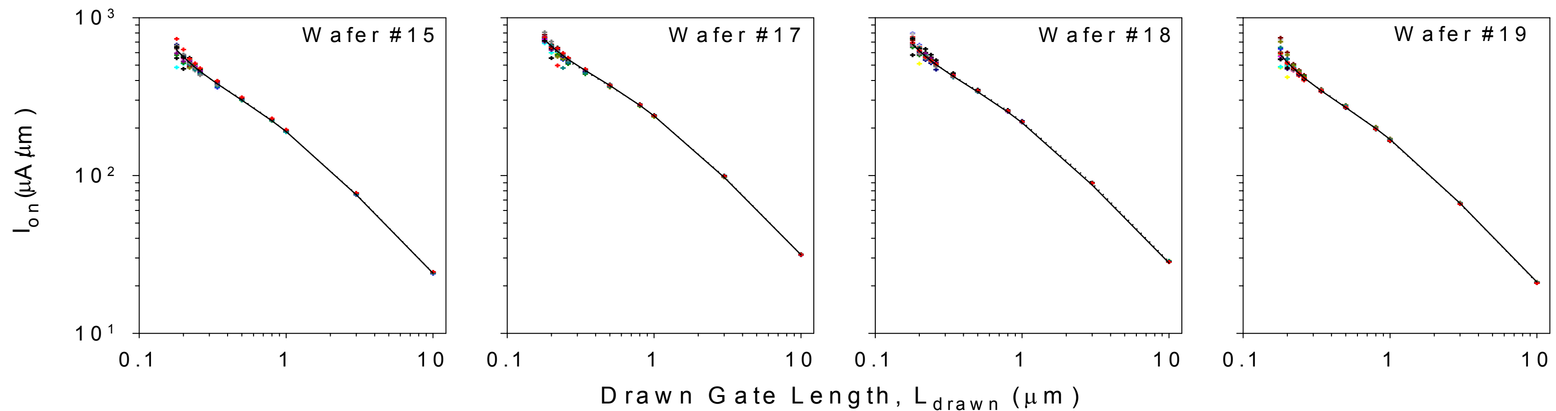
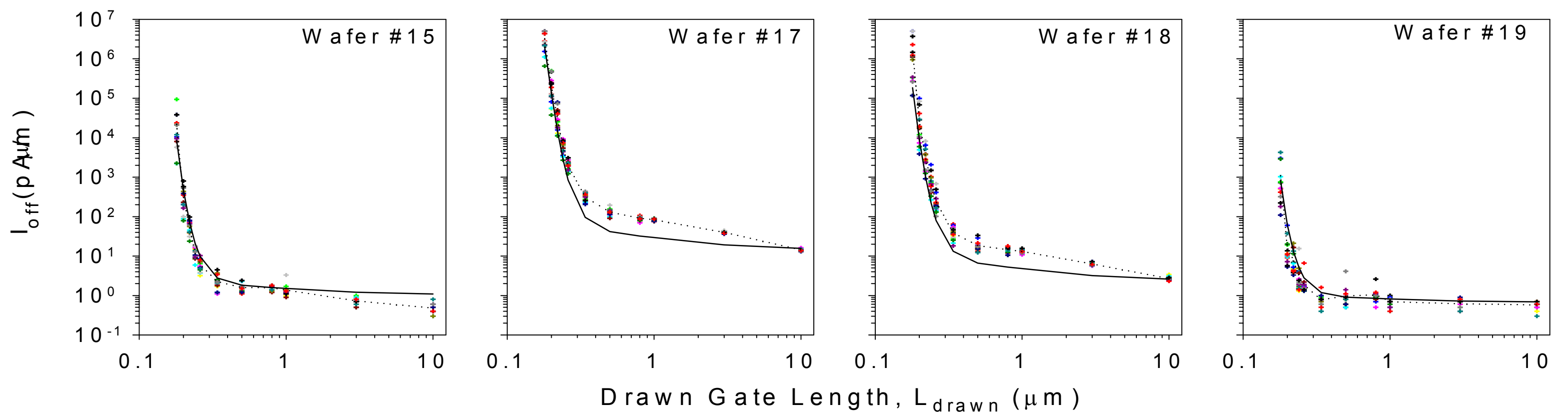
Process Correlation on the 0.25-μm Technology

Saturation/leakage Current Prediction





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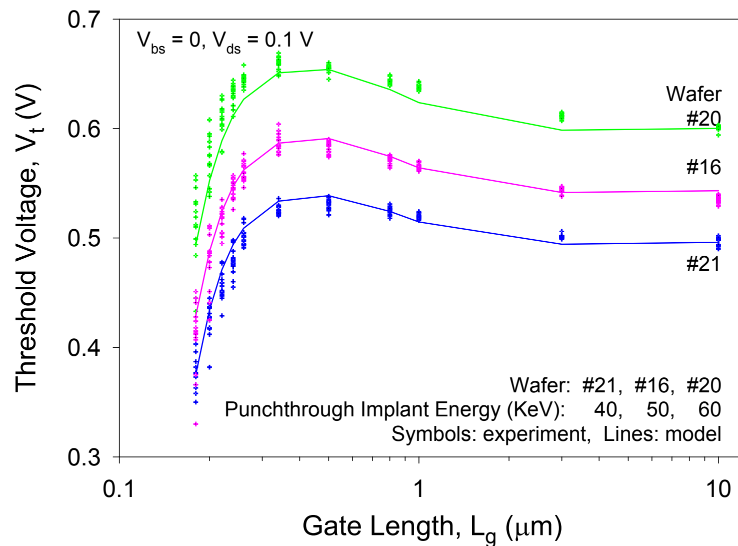
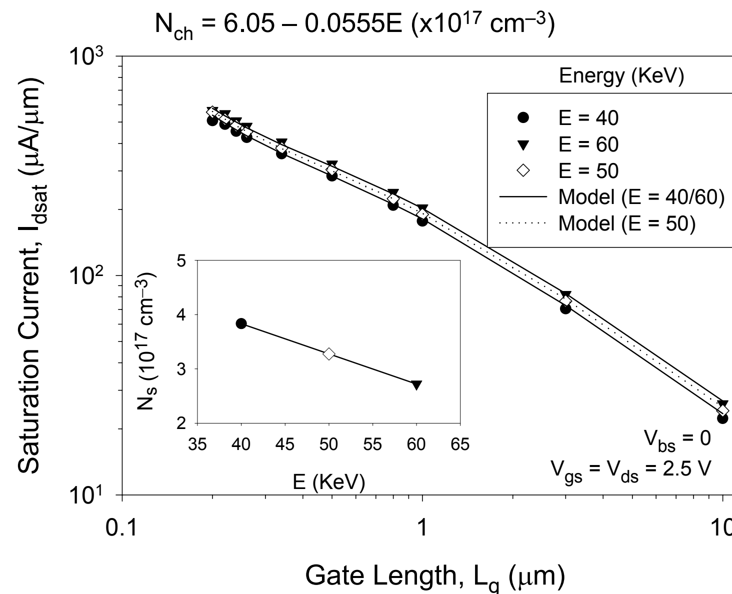
Punchthrough Implant Energy Correlation

$V_t - L_g$ Prediction



$I_{dsat} - L_g$ Prediction



Xsim prediction (wafer #16) with PT-implant energy as input parameter

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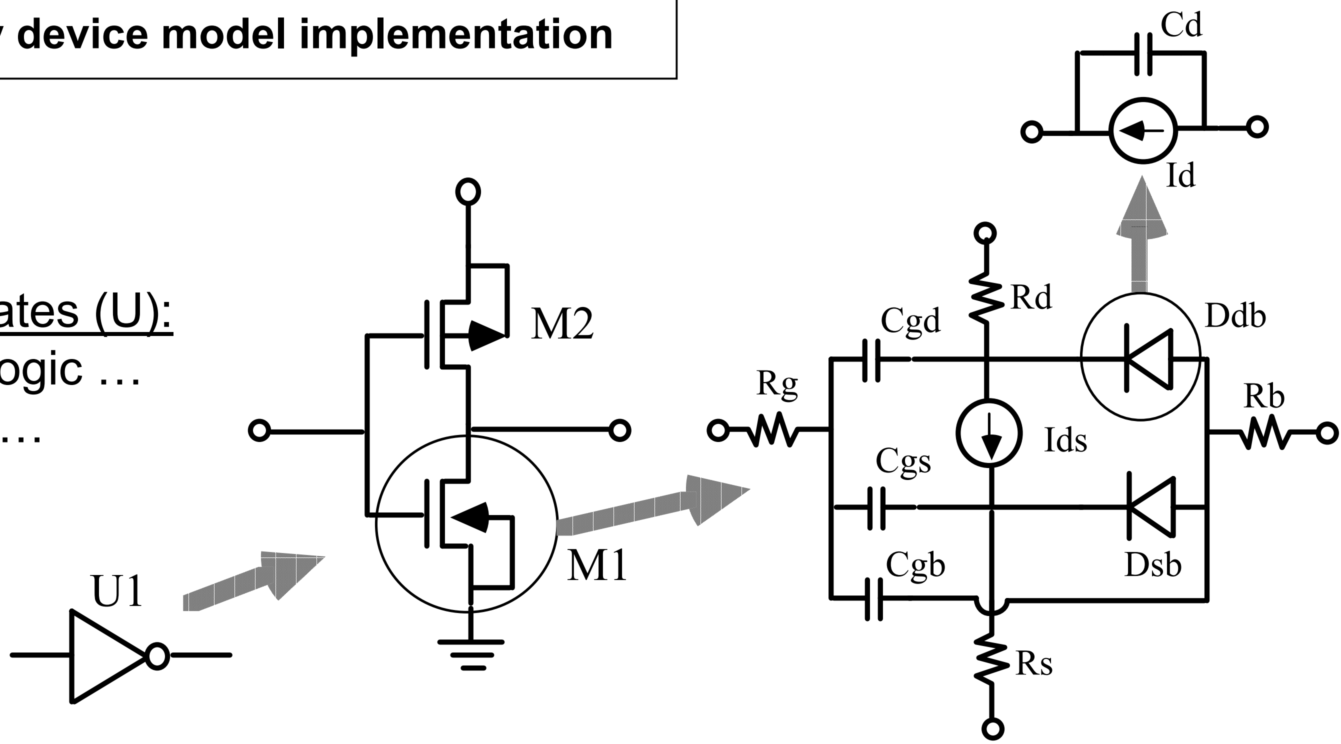
XSIM: Subcircuit Expansion Approach

- **Natural circuit partition (BBD matrix)**
- **Consistent dual representation**
- **Easy device model implementation**

Digital gates (U):
.model logic …
.subckt …



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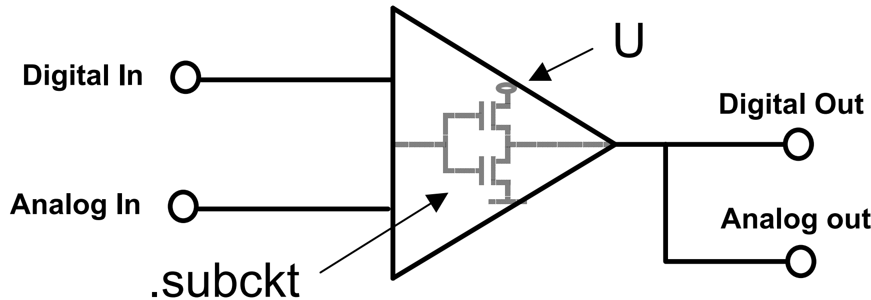
Dynamic Partitioning and Mode Switching



Three modes:	As if:
.set mode=**ana**log	**X**
.set mode=**dig**ital	**U**
.set mode=**mix**ed	**X↔U**

- **Dual representation**
  - Each digital gate (**U**) has two representations: ***logic*** and ***subckt***
  - Higher-level (*logic*) model parameters are extracted from lower-level (*subckt*) equivalent, thus, a consistent dual-representation
- **Accuracy–speed tradeoff**
  - In ***analog*** mode: **U** elements are simulated with "analog accuracy" (as if **X**)
  - In ***digital*** mode: **U** elements are accelerated with "digital speed"
  - In ***mixed*** mode: **U** elements are switching between *analog* and *digital*, at run time, depending on the "quality" of the input signal

➢ ***An "implict"/automatic/dynamic mixed-signal simulator***

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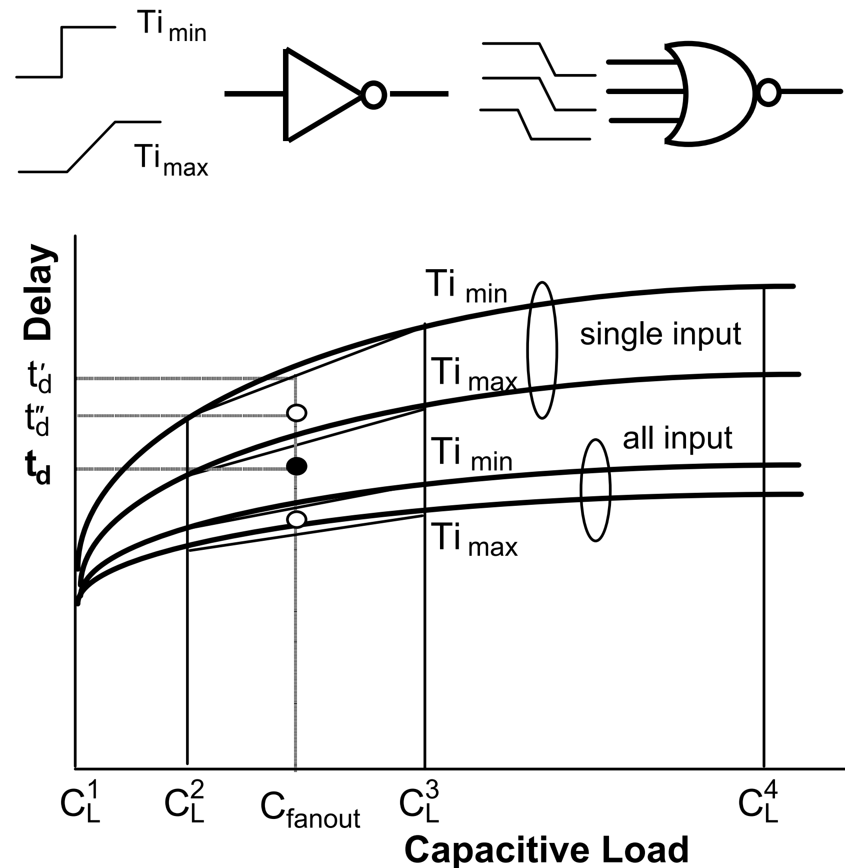
Dynamic-Delay Model

- **Delay depends on:**
  - Load capacitance (user-netlist)
  - Input transition time (run-time)
  - Input triggering (run-time)
- **Logic parameters**
  - Input/output capacitances
  - Intrinsic delays, rise/fall times
- **Dynamic-delay model**
  - ***Nonlinear load dependence***: *N*-breakpoint algorithm
  - ***Input-slope dependence***: Linear interpolation/extrapolation
  - ***Multiple-input triggering***: Single-/all-input triggering

➢ *Pre-calculated by simulating the full-subcircuit & stored in* ***.model***



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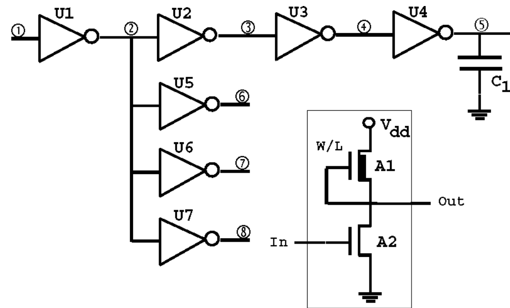
Comparison of Different Delay Models

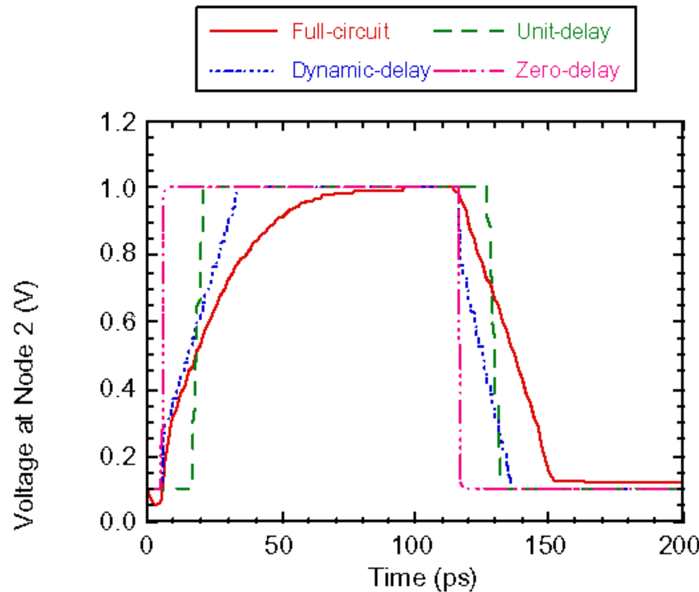


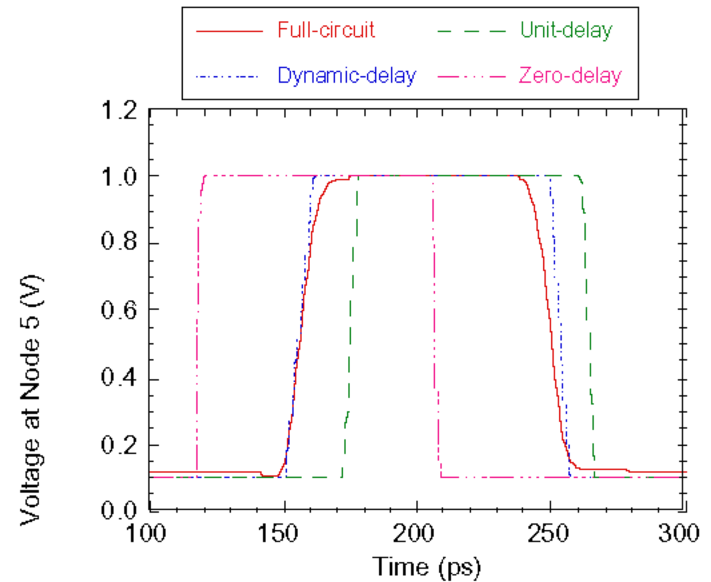
Fanin capacitance:

Cin1–4 = 4.48 fF
Cin5 = 4.64 fF
Cin6 = 4.33 fF
Cin7 = 4.20 fF

CPU time (s):

Full-circuit = 21.86
Dynamic-delay = 3.89
unit-delay = 3.61
zero-delay = 3.54





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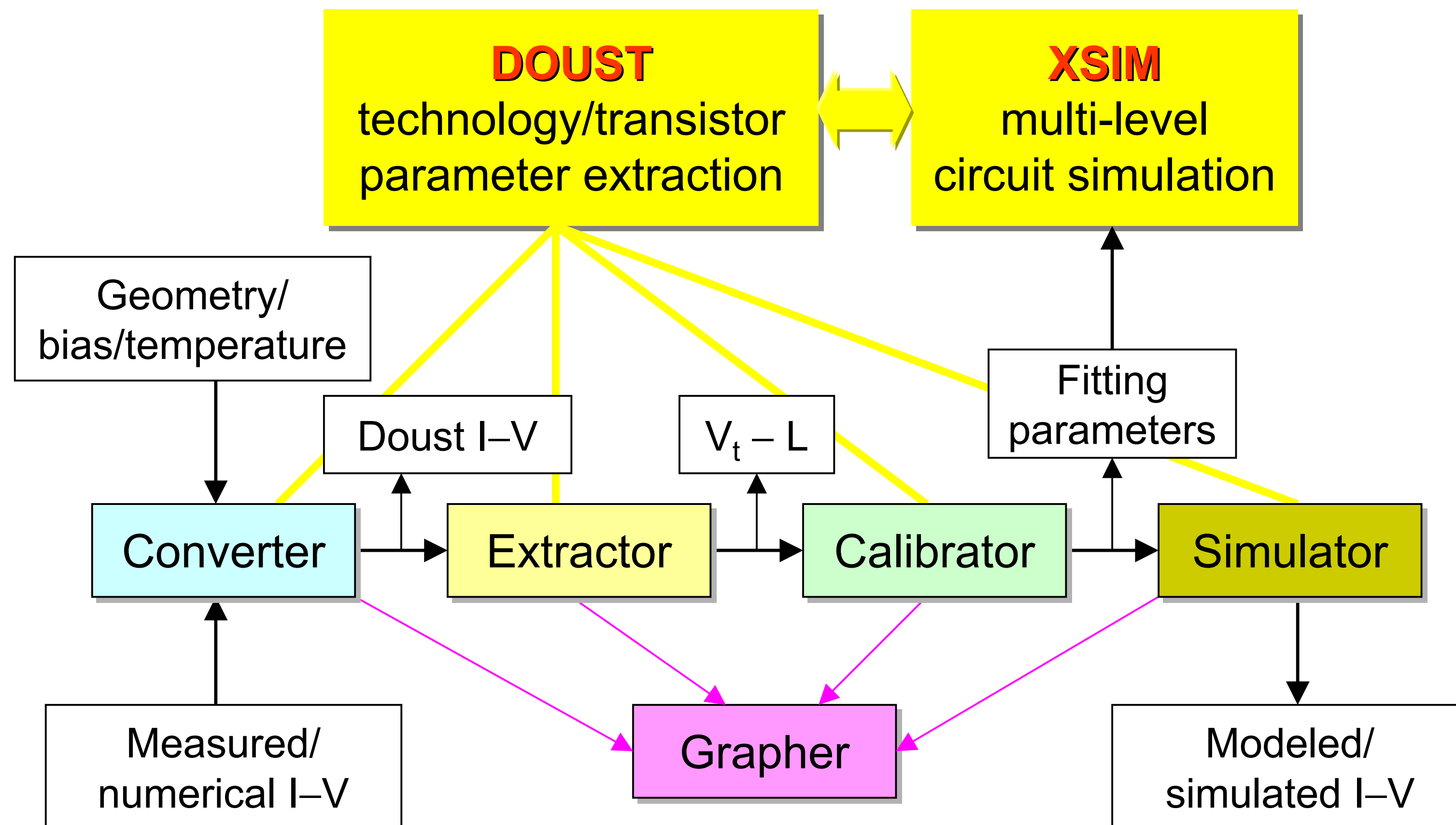
DOUST:
*D*esign and *O*ptimization of *U*ltra-*S*mall *T*ransistors



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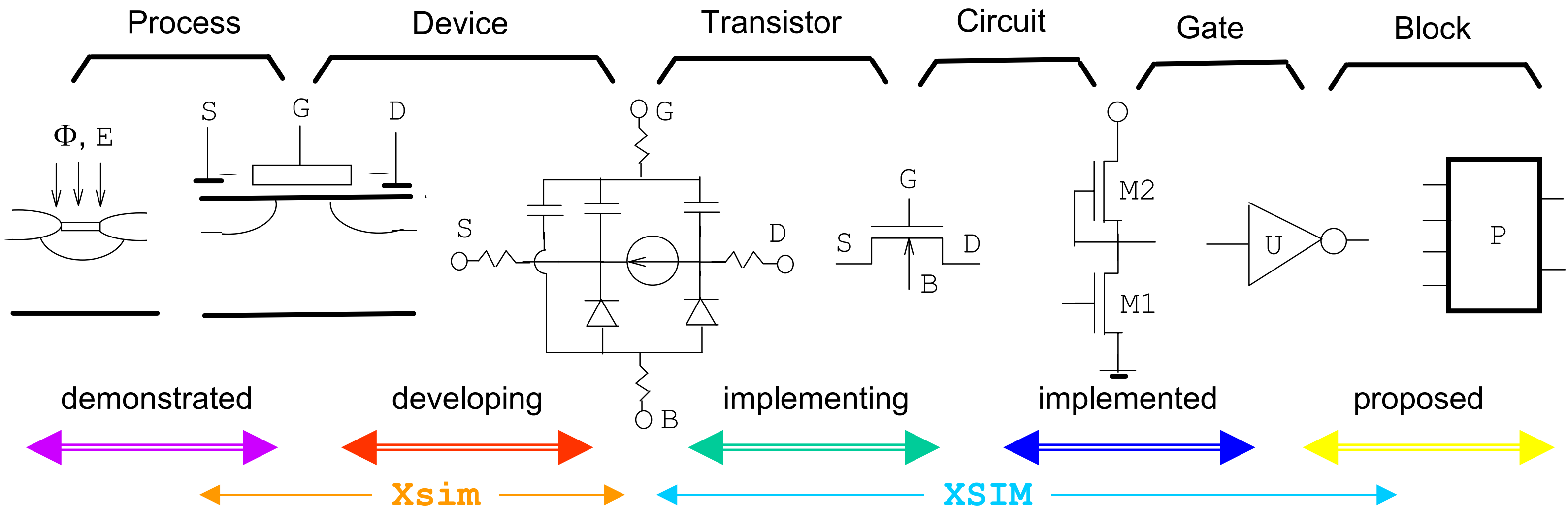
Multi-Level Modeling with Dual Representation: From Process Through Device/Circuit to System



Device Level	Transistor Level	Gate Level	Block Level
.model	**Mxx** <Nd> <Ng> <Ns>	**Uxx** <Nref> <Nout> <Nin1>	**Pxx** <Nref> <Nout1>
+ *<Mname>*	+ *<Mname>* <L> <W>	+ [<Nin2> …] *<Family>*	+ [<Nout2> …] <Nin1>
+ **nmos**	**.subckt** *<Cktname>*	+ *<Type><n>* *<Cktname>*	+ [<Nin2> …] *<Blk_name>*
+ [*param-list*]	+ <N1> [<N2> …]	**.model** *<Family><Type><n>*	+ *<Blk_type>* *<Ckt_name>*
:	+ [*param-list*]	+ <N1> [<N2> …] **logic**	**.model** *<Blk_name>* **block**
+ [*process-vars*]	**.ends**	+ cap1 drms dfxa … [*param-list*]	+ [*param-list*]

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Conclusions

- **Multi-level modeling environment**
  - ***Compact Model*** (CM) is at the core of the modeling hierarchy, as it bridges between a given technology and circuit design and determines the accuracy/speed tradeoff.
  - Centered at the ***transistor*** level, "push down" to ***technology*** level for process correlation, and "push up" to ***block*** level for system performance optimization.
- **Dual representation in single engine**
  - The key to having a consistent multi-level solution is to have a ***dual-representation*** at each level.
  - The key to establishing the link between the technology developers and circuit designers lies in the development of a ***single-engine*** tool.
- **Vision**
  - A compact model for technology developers
  - A circuit simulator with process-variable input

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