Integrated Circuits design using open-source EDA tools and open-source PDK’s

Krzysztof Herman

MOS-AK, LatAm 2025

Projects: BMFTR -> FMD-QNC (16ME0831)

IHP in a nutshell

- IHP is the European research and innovation centre for silicon-based systems, ultrahigh-frequency circuits and technologies,
- Unique selling point of a 200mm pilot line for state-of-the-art BiCMOS technologies, operated under industry-like conditions, 24/7, for the provision of prototypes and low-volume production runs.
- Qualified technological platform with direct access for science and industry
- Vertical structure from material research to system architecture
- 350+ employees, 40+ nationalities

Vision

"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalized and networked world as well as for the sustainable preservation of our natural living conditions."

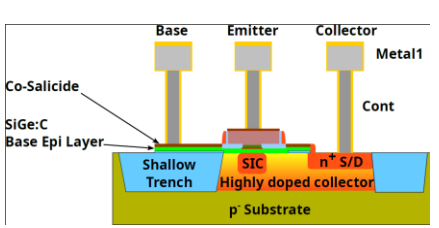
130nm SiGe BiCMOS Technologies for RF Applications

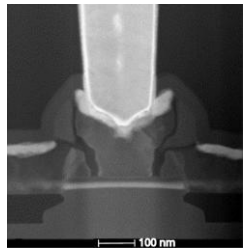
	SG13S	SG13G2	SG13G3Cu
HBT f_t / f_{max}	250 / 340 GHz	350 / 450 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CE0}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
TWIN-RELECTors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	2.1 fF / µm²
Metallization	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm)	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm	*Cu: 4 + 2 (3µm) Al: 2 (3µm

*Cu BEOL from X FAB

- Target are high-end technology developments, low volume market introduction, technology transfer for potential mass production in commercial fabs
- SG13S & SG13G2 are qualified and ready for Low Volume of high end products
- SG13G3Cu is early access - qualification scheduled 2025

- SG13G2 technology was selected for the development of an open source PDK





What is open-source ?

*Open source is software whose source code is publicly available under a license that lets anyone **use, study, modify, and share** it.*

Two big license families:

- **Permissive** (MIT, BSD, Apache-2.0): few restrictions; OK for closed-source forks.
- **Copyleft** (GPL, AGPL, LGPL): derivatives must remain open under similar terms
- **Dual license** – is a freqent option

Well known and used open-source projects:

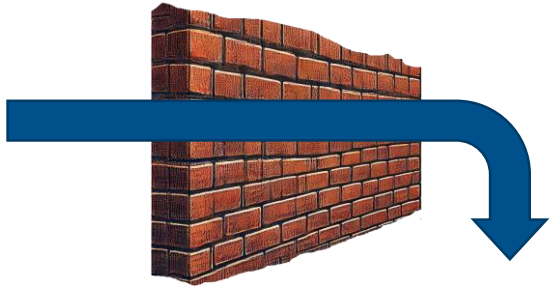
- Linux kernel
- Android OS
- RISC-V ISA

Red Hat (RHEL) — subscriptions, support & services around open-source Linux (acquired by IBM for ~$34B).

Inside the app: PowerPoint → **File → Account → About PowerPoint** → look for **Third-Party Notices/Additional Credits**. Microsoft includes a “Third-Party Software Notices and Information” page with the open-source licenses used in that build

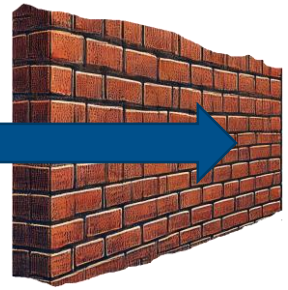
Traditional ASIC development (academic perspective)

EDA provider

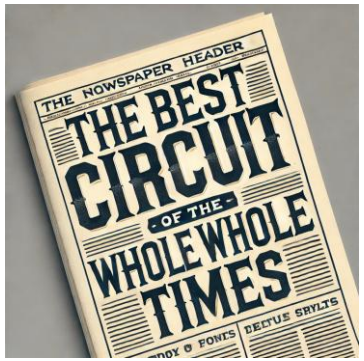


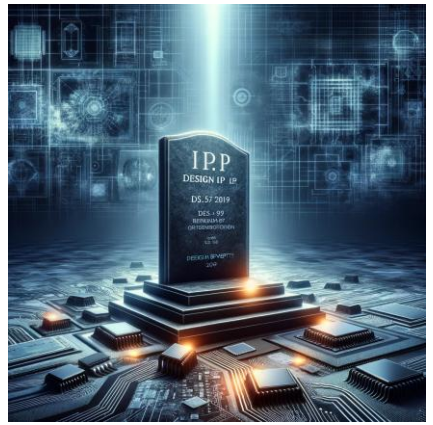
NDA walls

Existig IP blocks

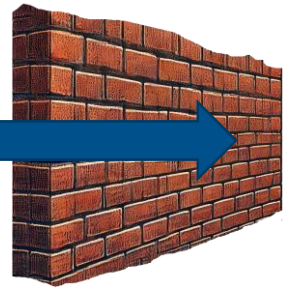


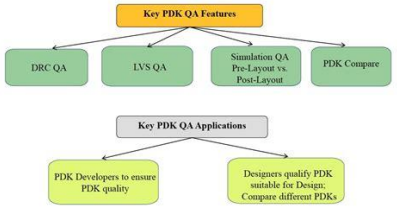
Designer





Foundry

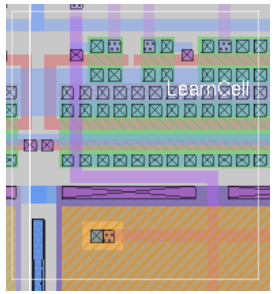




PDK

Flexibility is wanted

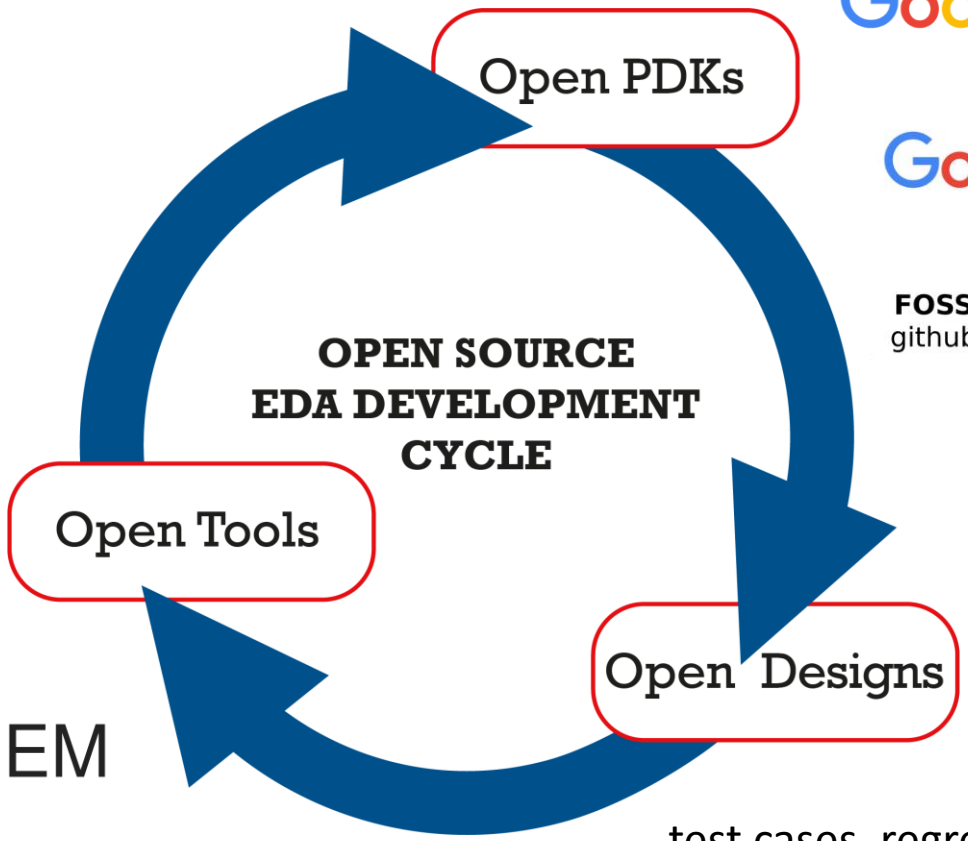
Open source silicon development cycle



Qucs

NGSPICE

XSCHEM



Google + skywater TECHNOLOGY

Google + GLOBAL FOUNDRIES

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

IHP-Open-PDK

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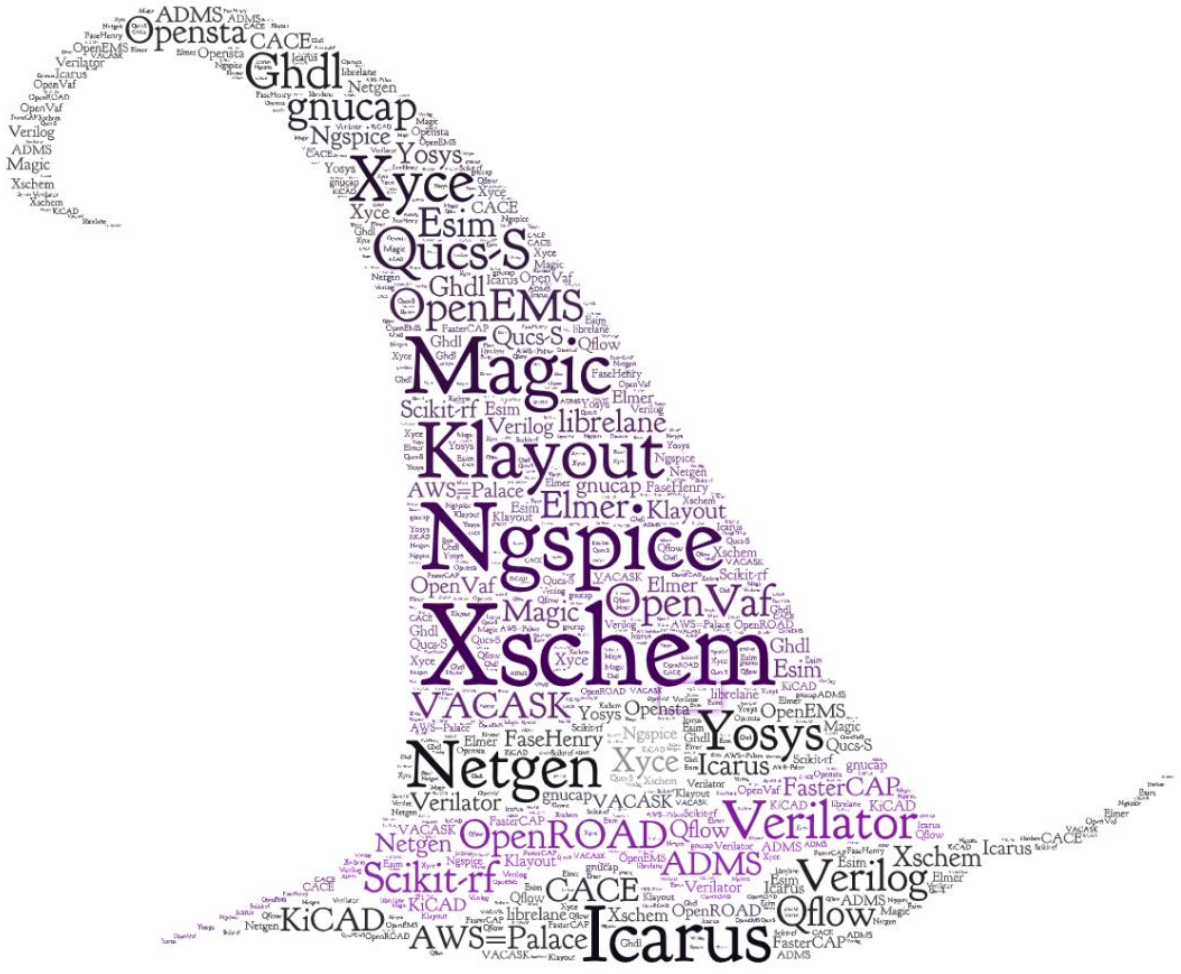
RISC-V®

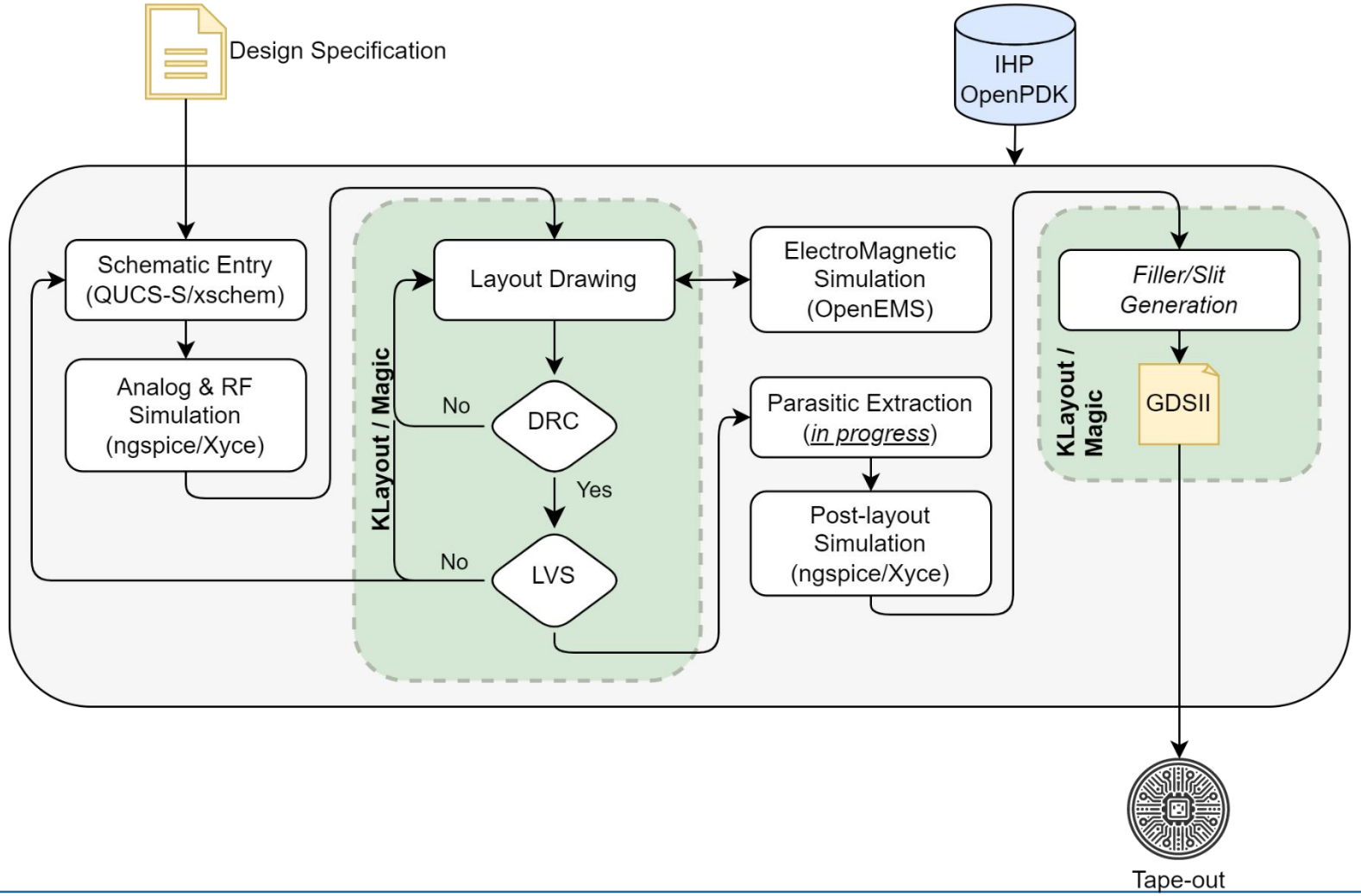
test cases, regression tests, benchmarks, use cases,
user stories, feedback, error reports, feature requests

Open-source EDA Tools



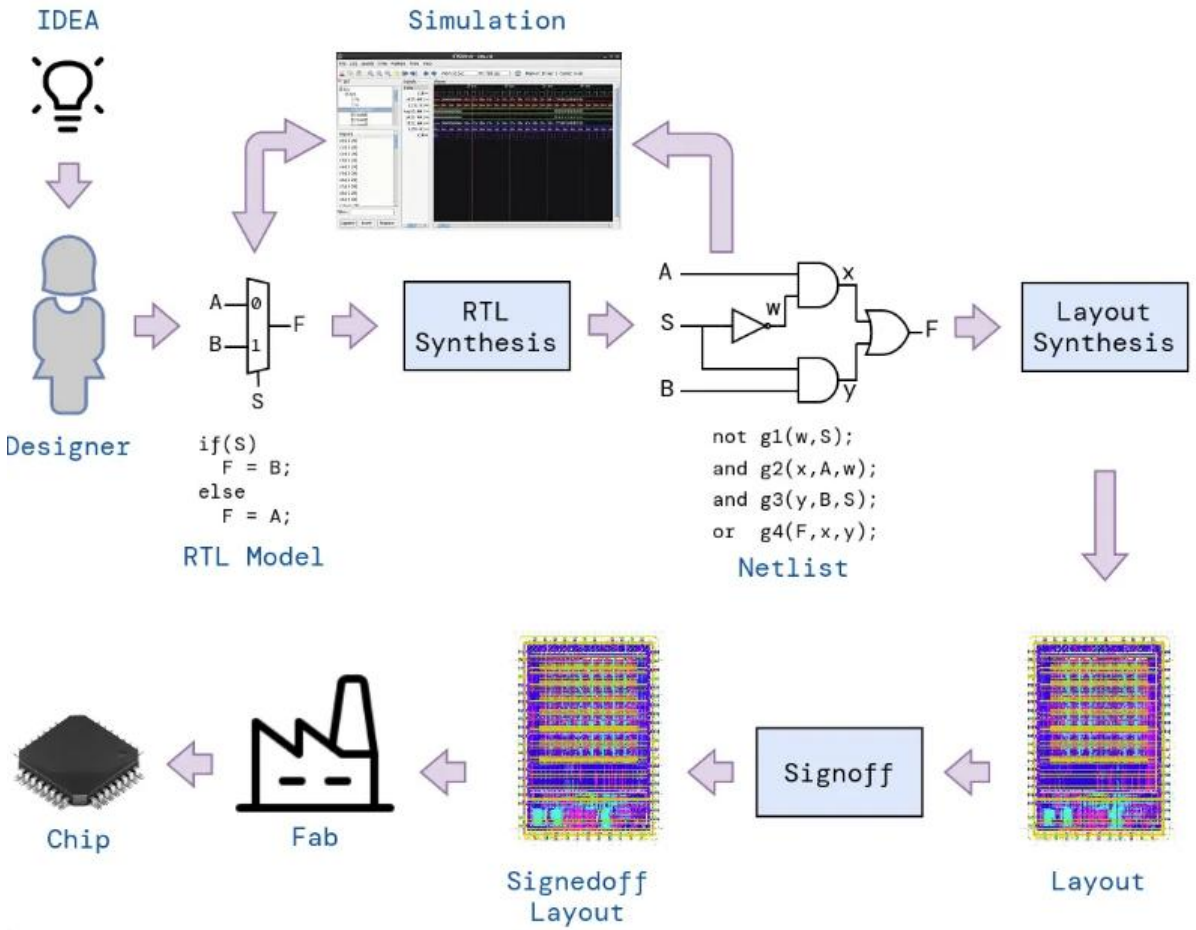
- Tools are usually task specific: simulation, layout editing, schematic capture, design checks etc.
- Flow is a set of tools to execute tasks in a specified order
- Flows are specific: analog, digital, mixed signal, RF, low power, verification etc…
- Flow can be parametrized
- Flow can be automated (TCL, Python)

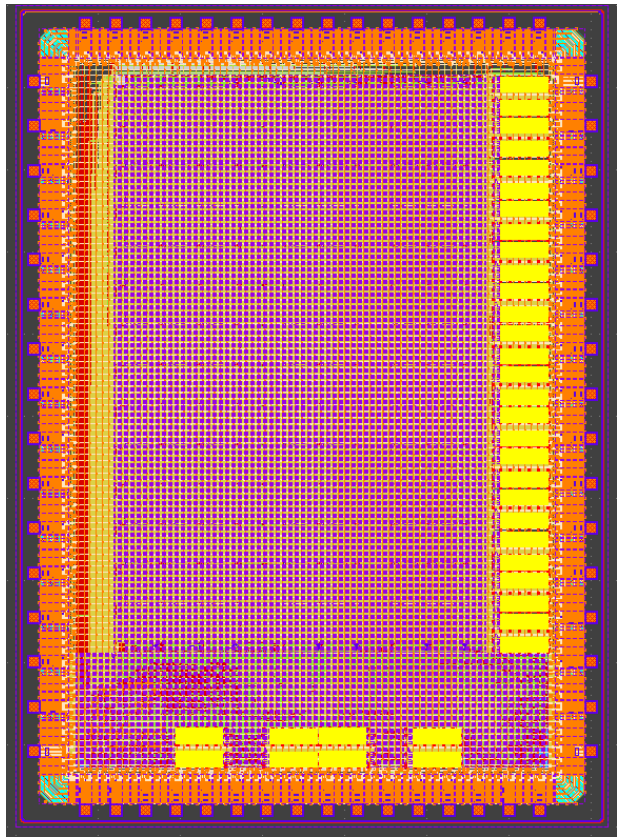
Analog/RF Open Source Design Flow: status at a glance

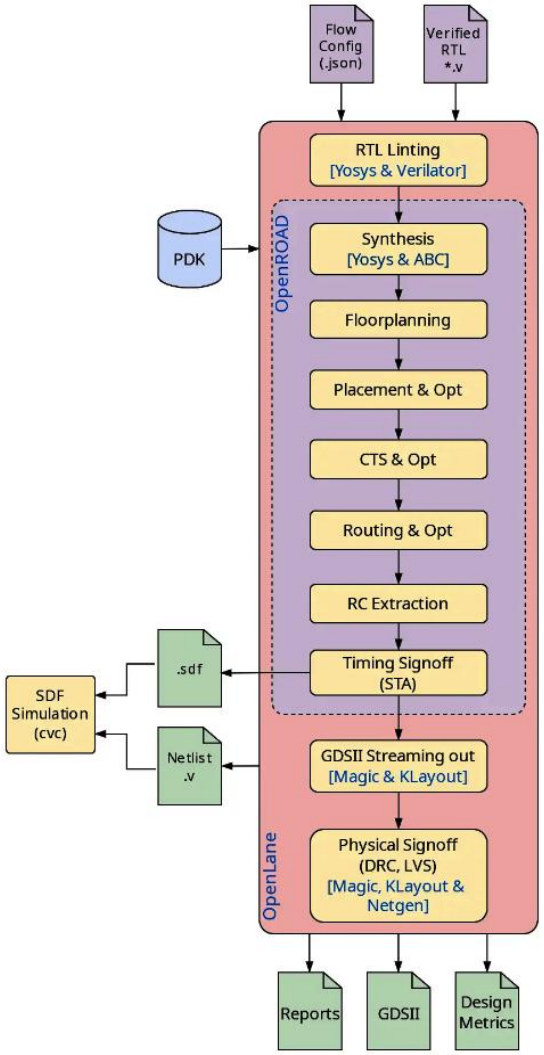


- KLayout-oriented flow
  - Layout design
  - Parameterizable cells
  - Physical Verification
- QUCS-S, xschem
- ngspice, Xyce, gnucap, VACASK
- Openvaf, ADMS
- OpenEMS, ElmerFEM, AWS Palace

Digital LibreLane based flow







https://github.com/librelane/librelane

Process Design Kit – what is that ?

Process Design Kit aka. PDK is a set of information called libraries to make the designer's life easier. Additionally a PDK:

- is process specific: SG13G2, SKY130A, GF180mcuC,
- the information should be compatible with the standards/tools,
- contains building blocks: standard cells, IO cells, macros, primitive devices,
- delivers symbols for schematics and Pcells for layout
- provides models for simulators,
- includes rules for checking DRC and LVS aka. "decks",
- comes with process specifications and layout rule manual,
- showcases examples of use of the technology

EDA tools + PDK =
Design Environment

Open source PDK's comparison

Google + skywater

- 150 nm triple pwell process
- 1.8 V core CMOS3.3 V and 5 V / 10.5 V / 11 V / 16 V high-voltage MOS options
- Multiple threshold flavors (LVT, RVT, HVT)
- Native NMOS and isolated devices
- Parasitic lateral PNP and vertical NPN transistors
- Schottky and ESD diodes (standard, HV, antenna, photo)
- Poly-silicon resistors (low-R, high-R)Diffusion and well resistors (N+, P+, P-well)
- MiM and MOS capacitors (multiple density options
- Inductor structures supported (via top metals)5
- metal BEOL stack

Google + GLOBAL FOUNDRIES

- 180 nm CMOS mixed-signal / MCU technology
- 1.8 V / 3.3 V / 5 V / 6 V MOS devicesLVT / RVT / HVT MOSFET options (low, regular, high Vt)Native NMOS (low-Vt) devices
- Isolated N-well / P-well devices
- Diodes: signal, ESD, and high-voltage junction types
- Optional parasitic vertical NPN / lateral PNP devices
- Poly-silicon resistors (high R and low R variants)
- Diffusion and well resistors (N+ / P+ / P-well)
- MiM capacitor (metal–insulator–metal)MOS capacitor (gate oxide)Up to 6-metal BEOL (5 thin + 1 thick)
- Inductor-capable top metals for RF

IHP-Open-PDK

- 130 nm triple pwell BiCMOS:C process
- Ultra fast HBT's
- 1.2/3.3 CMOS
- Schottky, antenna diodes
- Svaricap
- ESD devices
- PNP lateral device
- isolation box
- 3 poly res
- MiM capacitor
- 7 metal BEOL (5 thin, 2 thick),
- Inductor capable
- RF analog + mixed signal

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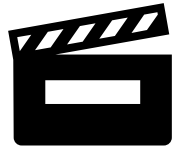
- 55 nm CMOSprocess
- Digital design oriented
- Abstracted views
- 745 std cells!
- 7 metal BEOL
- WiP
- iEDA + iPD down to 28 nm

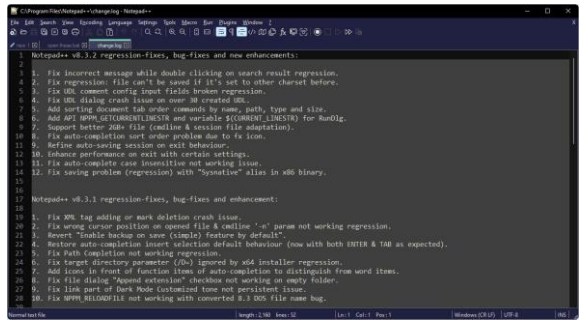
Open source PDK’s comparison – digital primitives

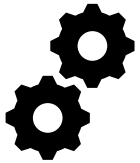
PDK	Standard Cells	I/O Cell Library	SRAM / Memory Macros	Notes
SkyWater SKY130	Yes — multiple libraries (HD, HS, MS, LS, LP, HVL)	Yes — sky130_fd_io covers full pad set	Partial — OpenRAM and 3rd-party SRAM macros available	Strong ecosystem, proven in open-source tape-outs; SRAM user-integrated
IHP SG13G2 (130 nm BiCMOS)	Yes — base standard cell set provided	Yes — full IO cellset (CDL, GDS, LEF, Liberty, Verilog)	Yes — 6 SRAM variants (64×64 → 2048×64) included	Excellent primitive coverage; still “preview” maturity
GF180MCU (180 nm)	Yes — 7-track and 9-track libraries	Yes — gf180mcu_fd_io I/O ring library	Yes — SRAM macros provided	Complete primitive set; older technology; experimental open PDK

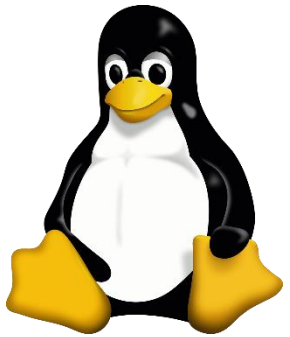
How to start ?

- Education
  - Books: L. Baker, W. Sansen
  - Youtube (fossi fundation)
  - Courses
  - Matrix Fossi channel
- Practice
  - Reverse engineering
  - Design experience
  - Setup the tools on linux
- Participation
  - Contribution to the OSS ecosystem









Courses on github

- Boris Murmann -> ECE628
- Harald Pretl
- Carsten Wulff
- Zero to Asic
- IHP GPT ;)

Education

From 2021 I've been teaching courses at NTNU.

Advanced Integrated Circuits

- aic2025 - PDF epub
- aic2024 - PDF epub
- aic2023 - PDF epub
- aic2022

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1_Lectures
2_Assignments
3_Tools
4_Technology
5_Design
6_Test
7_References

Analog Circuit Design

AUTHORS
Harald Pretl
Michael Koefinger
Simon Dorrer

AFFILIATION
Johannes Kepler University

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1 Introduction

This is the material for an intermedia
number 336.009 ("KV Analoge Schalt

The course makes heavy use of circu
The 130nm CMOS technology **SG13C**

Radio-Frequency Integrated Circuits

AUTHOR
Harald Pretl

AFFILIATION
Johannes Kepler University

PUBLISHED
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1 Introduction

This is the material for an introductory radio-frequency integrated circuits course. The contents are largely based on (Razavi 2011) and (Darabi 2020); these two books are an excellent introduction into this topic and are highly recommended! For a general introduction into RF and microwave (Pozar 2011) is a great read!

It is assumed that readers are familiar with the contents of this Analog Circuit Design course.

Design examples and courses of IHP

IHP-GmbH / IHP-AnalogAcademy

Code | Issues 32 | Pull requests | Actions | Projects

IHP-AnalogAcademy Private

main | 2 Branches | 0 Tags

Table of contents

OS-EDA / Course

Code | Issues 3 | Pull requests | Projects | Wiki | Security | Insights

Course Public

main | 1 Branch | 10 Tags | Go to file

Course instance: 1 Week, hands on

Mon	Tue	Wed	Thu	Fri
L1: Introduction T1: Training	Q1, Q2: Recap **Feedback** L3: Verilog T3: Training	Q3, Q4: Recap **Feedback** L5: PDK T5: Training	Q5, Q6: Recap **Feedback** L7: OpenROAD Flow scripts T7: Training	Q7: Recap L8: Tapeout **Feedback**
L2: OpenROAD tools T2: Training	L4: OpenROAD first run T4: Training	L6: OpenROAD GUI T6: Training	L7: OpenROAD Flow scripts 2 T7: Training	Spare time and Wrap-Up

L : Lectures

T : Training and Hands-On

Q : Questions

Tools

- Docker images- JKU, IEEE UNICAS
- Setup own machine at the university
- Build your own capacities to setup and maintain the tools
- Experiment with coding agents to contribute

IEEE UNICAS and SSCS activities

IEEE SSCS TC-OSE "Code-a-Chip" Travel Grant Awards at ISSCC'26

The IEEE SSCS Code-a-Chip Travel Grant Award was created to:

Low cost access to the silicon using open-source PDKs

Google + skywater TECHNOLOGY

- ChipFoundry.io
- 996 USD/ sq. mm
- Padframe + SOC+ Board
- 100 x QFN
- RTL to GDS open source flow
- 4 months turn around time
- Not disclosed designs

Google + GLOBAL FOUNDRIES

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

- Wafer.space
- 350 USD/sq. mm
- Min area 20 sq. mm.
- 1000 bare dies
- 4 months turn around time
- Not disclosed designs

IHP-Open-PDK

- IHP
- SG13CMOS5L
- 1500 EUR/sq. mm
- 20 bare dies
- 4 months turn around time
- Wafer sharing in EU
- Min area 1 sq. mm.
- Open source – yes
- Not disclosed – yes (higher price)

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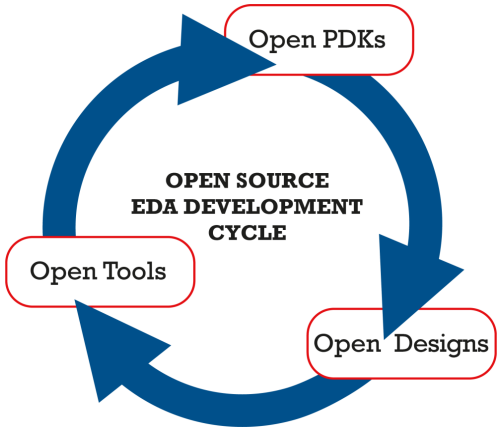
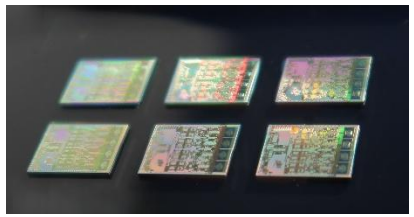
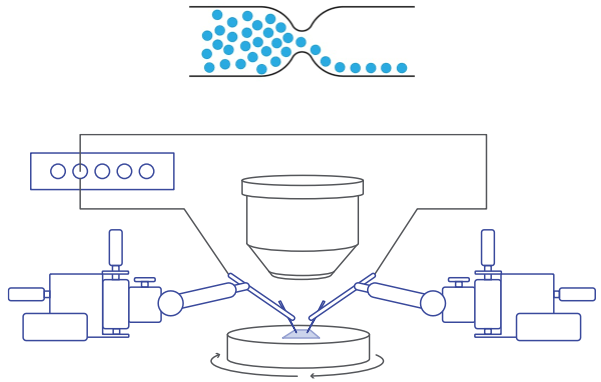
- TBD
- 5576 USD/sq. mm

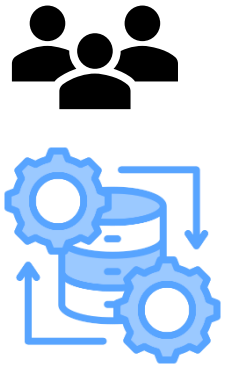
The future – Joint Evaluation – get involved!

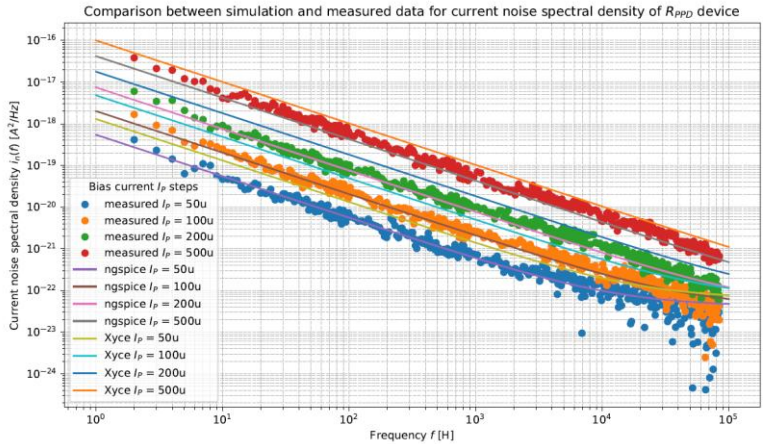
- Receiving your own silicon is just one milestone—it doesn't mean the development cycle is complete.
- The samples/wafers from free OpenMPW will be stored at IHP
- Anybody can rent chips for mesurments
- Silicon cross validation as research good practices
- Verified IP can become part of an open-source design library
- **How to organize the measurement to balance the load of the measurements lab ?**
- **How to organize the data processing ?**





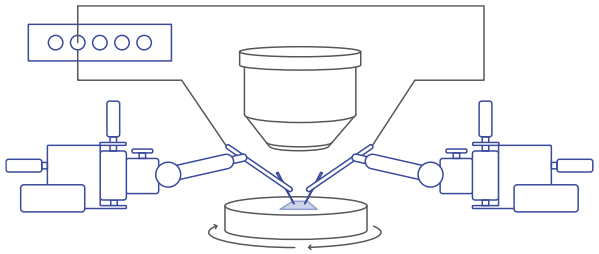


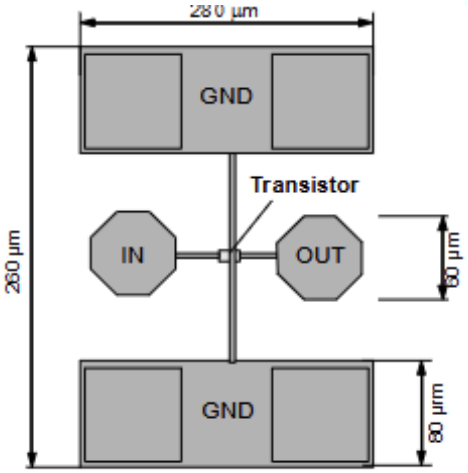


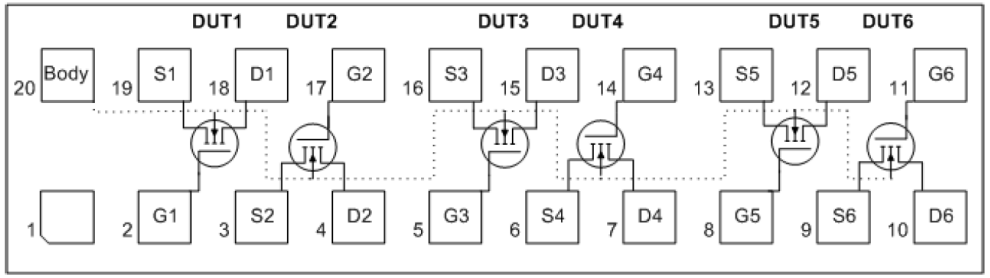


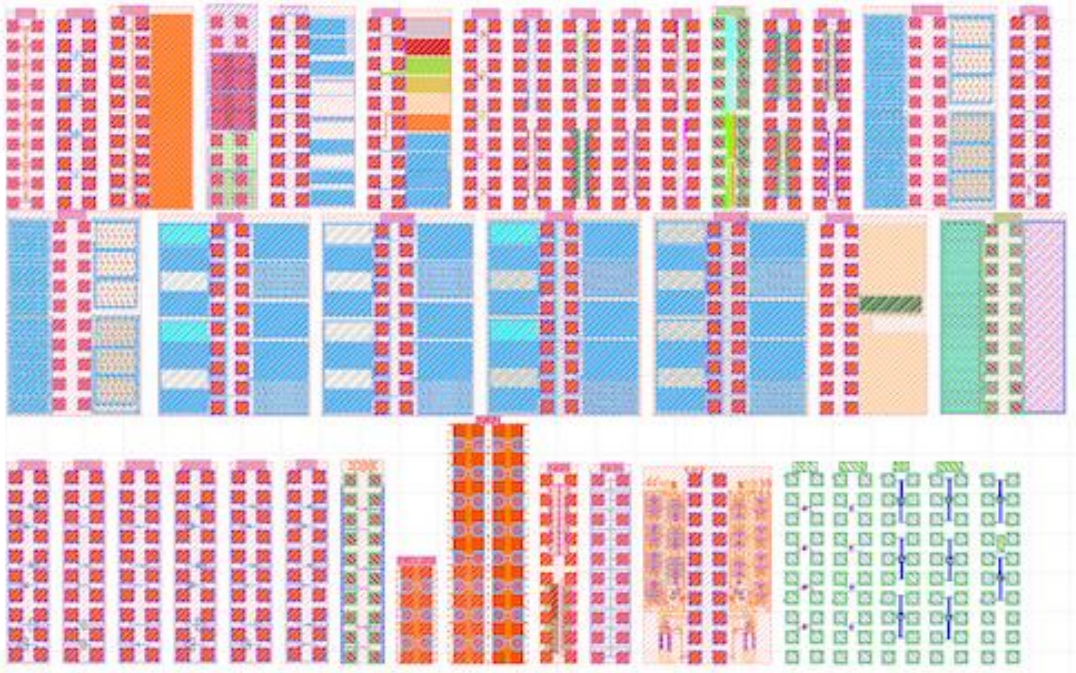
IHP – Open Test Structures

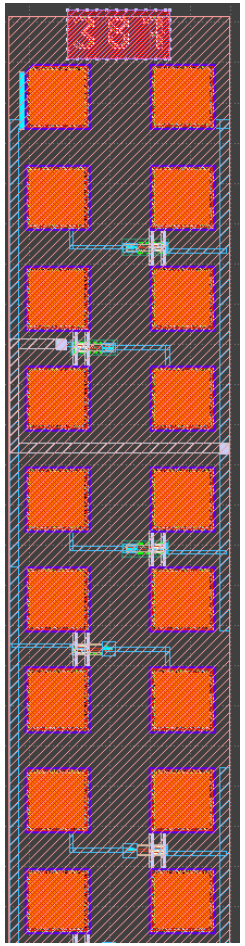
- Test structures to characterize the process
- Fully open source
- Ducumented testfields – layout + DUT parameters
- Diced chips can be shared anywhere
- Wafer sharing in EU is an option











The future – European Chip Design Platform with open-source

- Chips JU initiative for SME's (training, acceleration)
- Cloud based design environment with EDA tools, flows and IP's
- Open source is part of the platform: Analog, RF, AMS, Digital and Photonics related tools, flows
- Open-source design library: open source IP's

DCT

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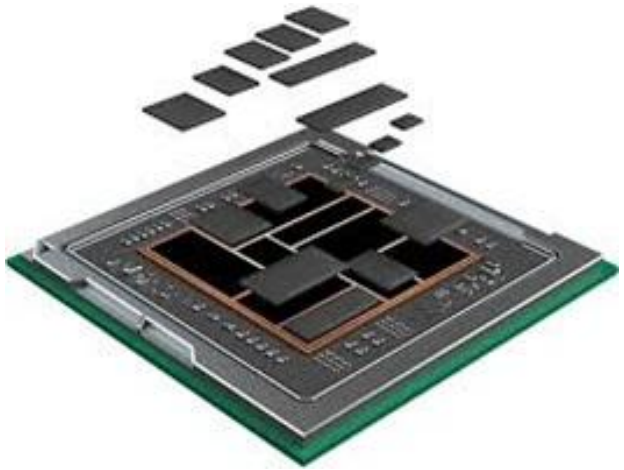
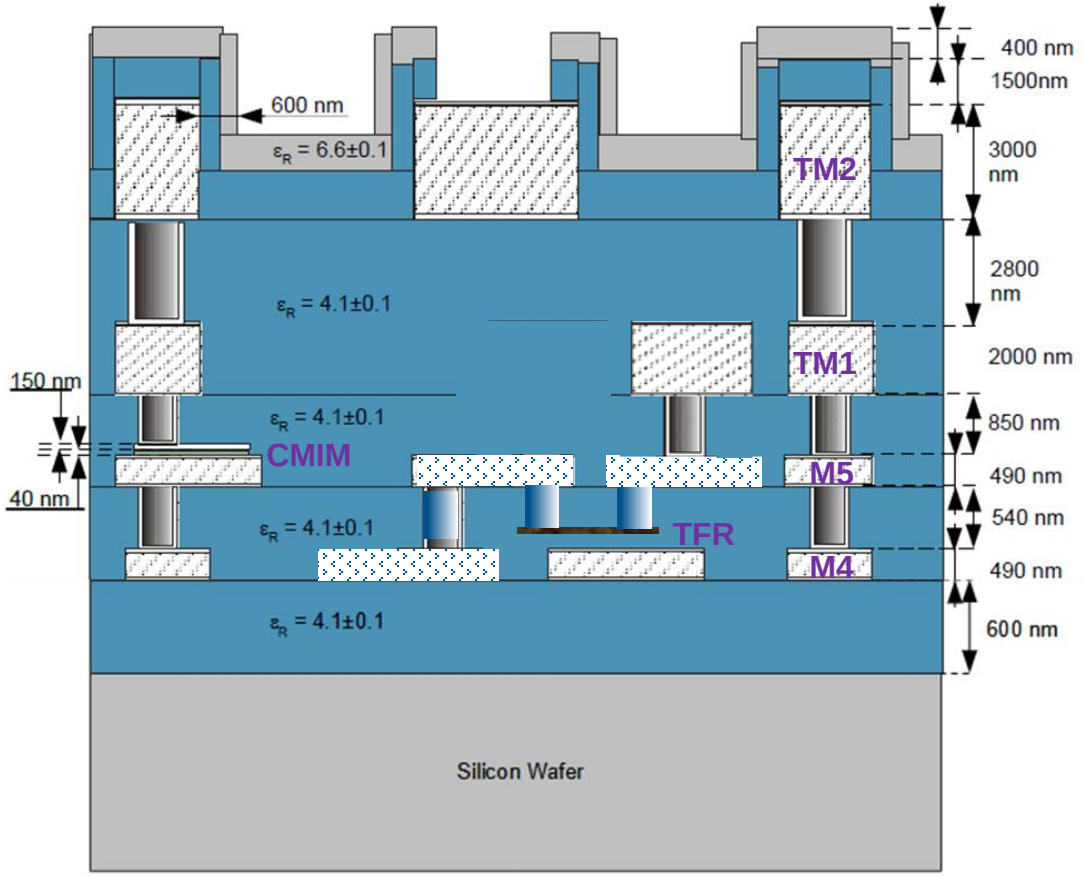
EuroCDP

IHP Open-source ADK Development

- IHP Silicon Interposer Technology
  - 130 nm Back-end of line (BEOL)
  - High-resistive silicon wafer
  - 4 Aluminum Metallization (3/2/0.49/0.49 µm)
  - MIM Capacitor (TM1-M5, 1.5 fF/µm²)
  - TFR Resistor (TiN - TFR, M5-M4, 25 Ω/□)

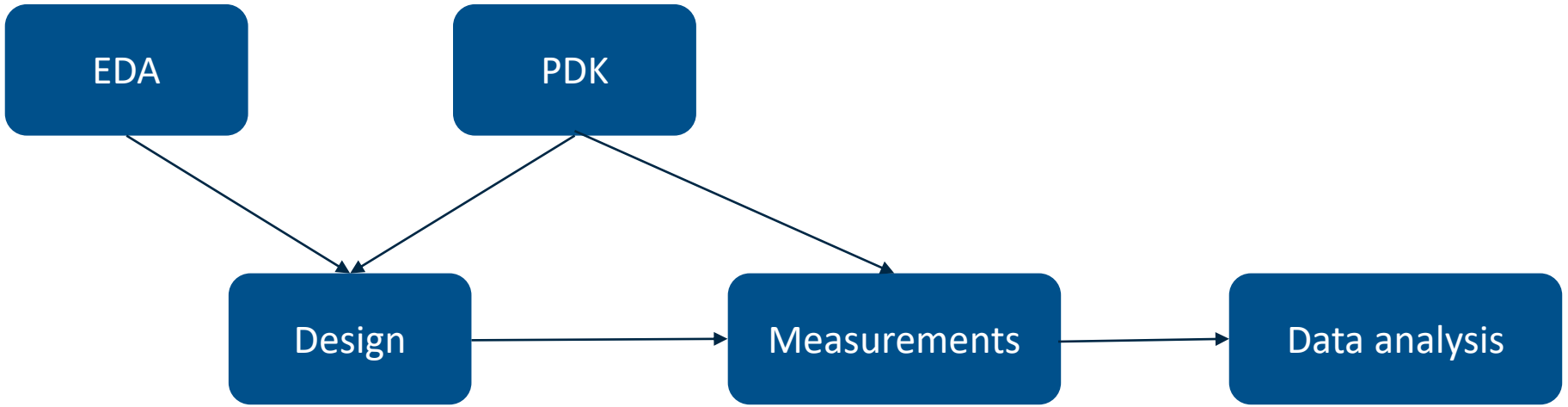
Heterogenous integration

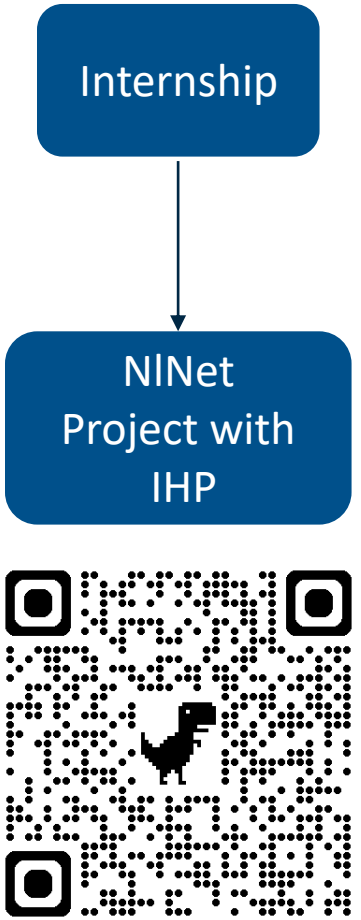




IHP internship opportunities

- 3 months paid internship (we do not cover the travel expanses),
- work visa,
- preferably early master, late undergrads students,
- dedicated task development (ie. RF components modeling and simulation using XSPICE and EM simulator)





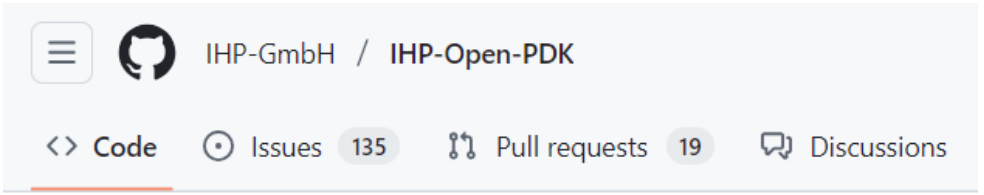
How to reach us

Email

- openpdk@ihp-microelectronics.com

GitHub

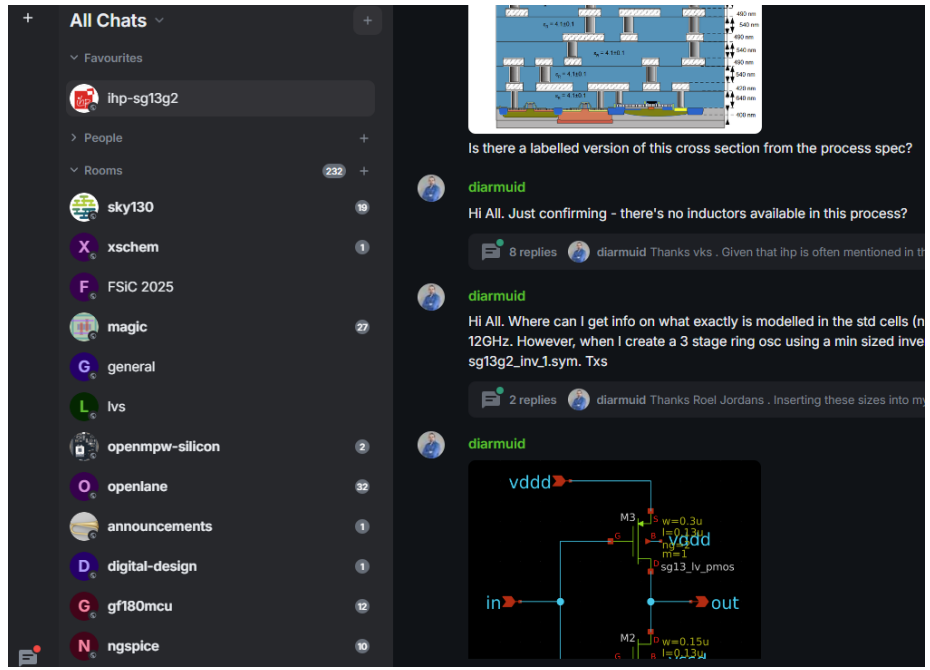
- issues – for reporting issues, questions
- discussions – for requesting features



Open Source Fossi-Chat.org channel:

`#ihp-sg13g2`

- general discussions
- announcements



Acknowledgements

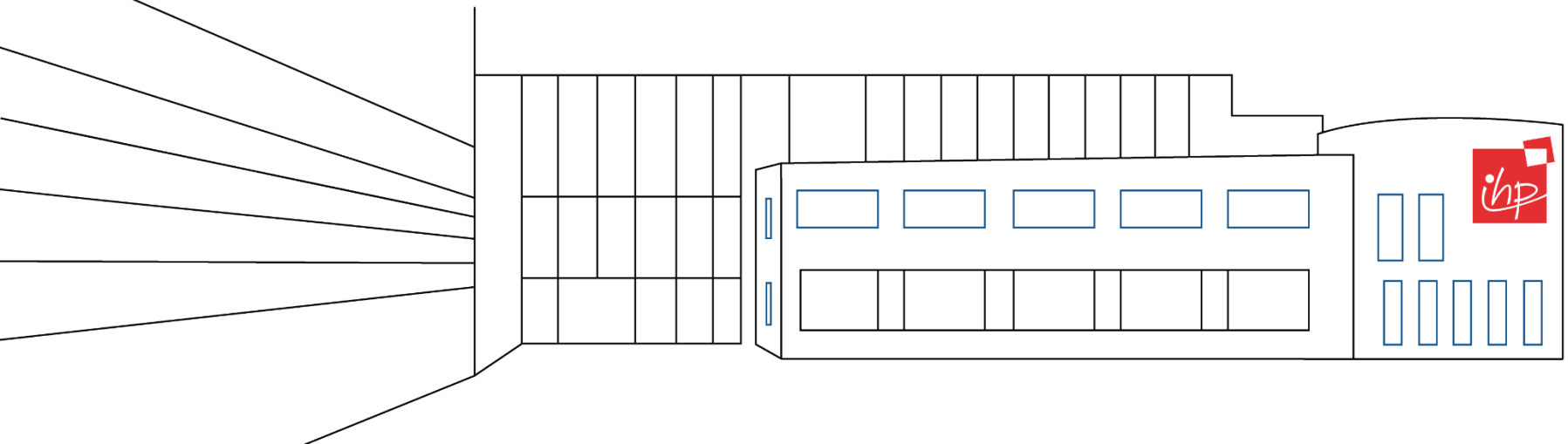
To BMFTR -> FMD-QNC (16ME0831) https://www.elektronikforschung.de/projekte/fmd-qnc

To our team at IHP

To all members of the open-source community who have supported and contributed our initiatives

Thank you for your attention!

IHP GmbH – Innovations for High Performance Microelectronics
Im Technologiepark 25
15236 Frankfurt (Oder)
Tel.: +49 (0) 335 5625 380
E-Mail: herman@ihp-microelectronics.com



Leibniz Association