

Center for Research and Advanced Studies (CINVESTAV)

Av. del Bosque 1145, El Bajío, 45017 Zapopan, Jal. Méx.

## Design and Integration of Multiple Open-Source Analog Circuits Fabricated in SKY130 Technology within Siliccluster v2.

**Presented by:**

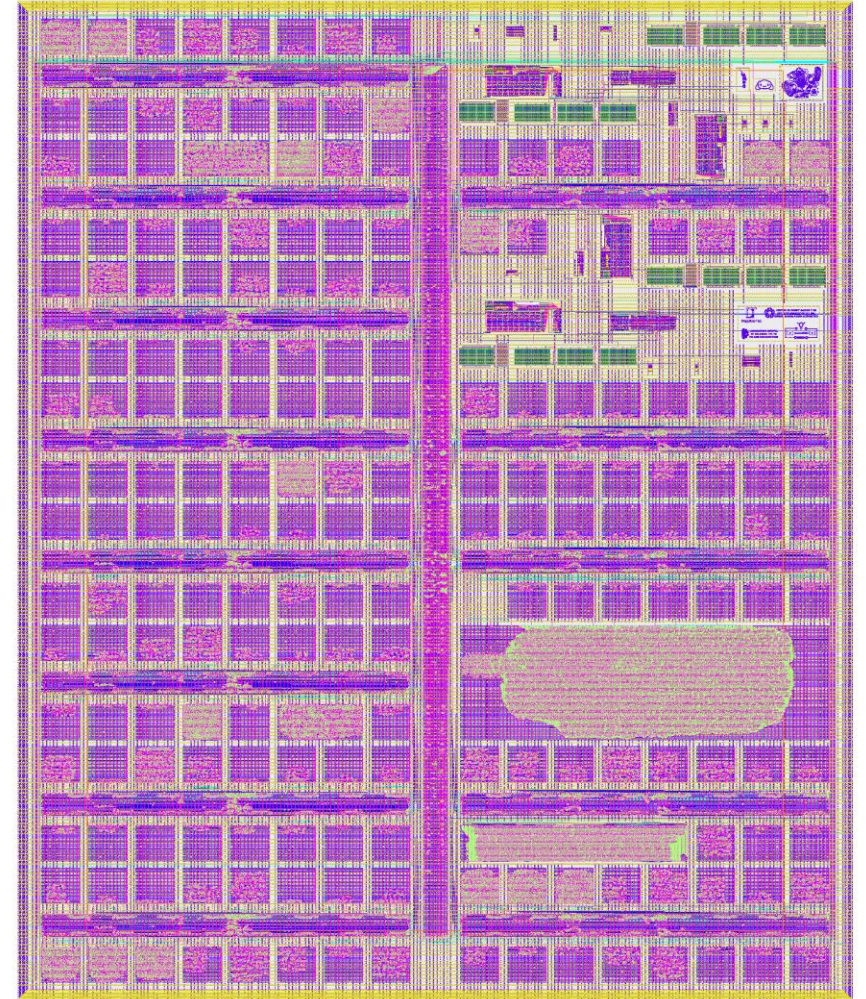
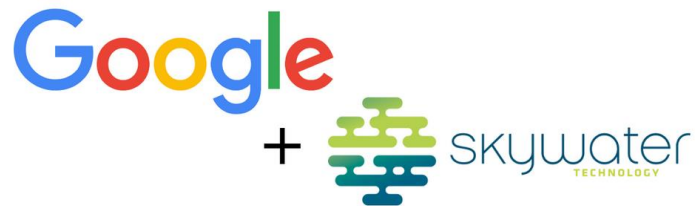
Uriel Jaramillo-Toral, Héctor Emmanuel Muñoz Zapata, Emilio Issac Baungarten,  
Susana Ortega-Cisneros

# Introduction

- This work integrates several compact analog modules inside the Siliclusterv2 chip, using a completely open-source design flow in SKY130 technology.
- It includes filters, oscillators, a buffer, an inverter, and an operational amplifier, as well as mixed-signal blocks for their characterization.
- It demonstrates that it is possible to design and fabricate multiple analog modules on a single chip using only open-source tools, meeting physical-design rules and achieving consistent results.

# What is Silicluste r?

- Silicluste r is a circuit-integration platform that allows grouping dozens of independent modules into a single chip.
- It uses an internal multiplexing architecture that selects any module and connects it to common input/output pins, avoiding the need to fabricate a separate chip for each design.
- It was created to enable testing, characterization, and rapid prototyping using open-source tools and PDKs.



**Silicluste r V2**

# Silicuster Versions

### SILICLUSTER v2

DIGITAL: DIGITAL MUX DEMUX (16 IN TO 16-18 OUT AND 10-16 IN TO 18 OUT), INDEPENDENT DIGITAL BLOCKS

ANALOG & MIXED SIGNAL: ANALOG MIXED-SIGNAL PROJECTS AREA, ANALOG 18-CHANNEL MUX DEMUX (32 REPRESENTATION IN BLOCKS), ANALOG 18-CHANNEL MUX DEMUX (32 REPRESENTATION IN BLOCKS), DAC/CLK 8 BITS (VISUALIZATION IN BLOCKS)

### SILICLUSTER MINIMAL FAB VERSION

ANALOG 18-CHANNEL MUX-DEMUX (VISUALIZATION IN KLAYOUT)

DIGITAL MUX-DEMUX: 4 IN TO 4-18 OUT AND 4-18 IN TO 4 OUT (VISUALIZATION IN KLAYOUT)

### SILICLUSTER v1

Silicuster: Innovation in compact design

Silicuster Plus: More space. More flexibility

Silicuster Pro: Maximum power in your hands

	Silicuster	Silicuster Plus	Silicuster Pro
Blocks	256Block	256Block	256Block
Dimensions	150 x 150 μm	175 x 210 μm (+63% block area)	175 x 210 μm (+63% block area)
Central Multiplexer	4 bits	4 bits	4 bits
Secondary Multiplexers	16 x 4 bits	16 x 4 bits	16 x 4 bits
Inputs/Outputs	10/10 per block	10/10 per block	16/16 per block (+60% inputs/outputs)
Clock	1 per block	1 per block	1 per block
Platform	Caravel	Openframe	Openframe
Chip Size	2920 x 3520 μm (+40% total area)	3170 x 4770 μm (+40% total area)	3170 x 4770 μm (+40% total area)
Total Area	10 mm <sup>2</sup>	15 mm <sup>2</sup> (+50% total area)	15 mm <sup>2</sup> (+50% total area)

### SILICLUSTER BETA

- GPIO
- 6 BITS MUX
- 64 BLOCKS
- RISC-V AREA

•Silicuster has gone through four versions. The Beta version integrated 64 digital modules, while version 1 increased the capacity to 256.

•Later, a test version was developed using Minimal Fab technology.

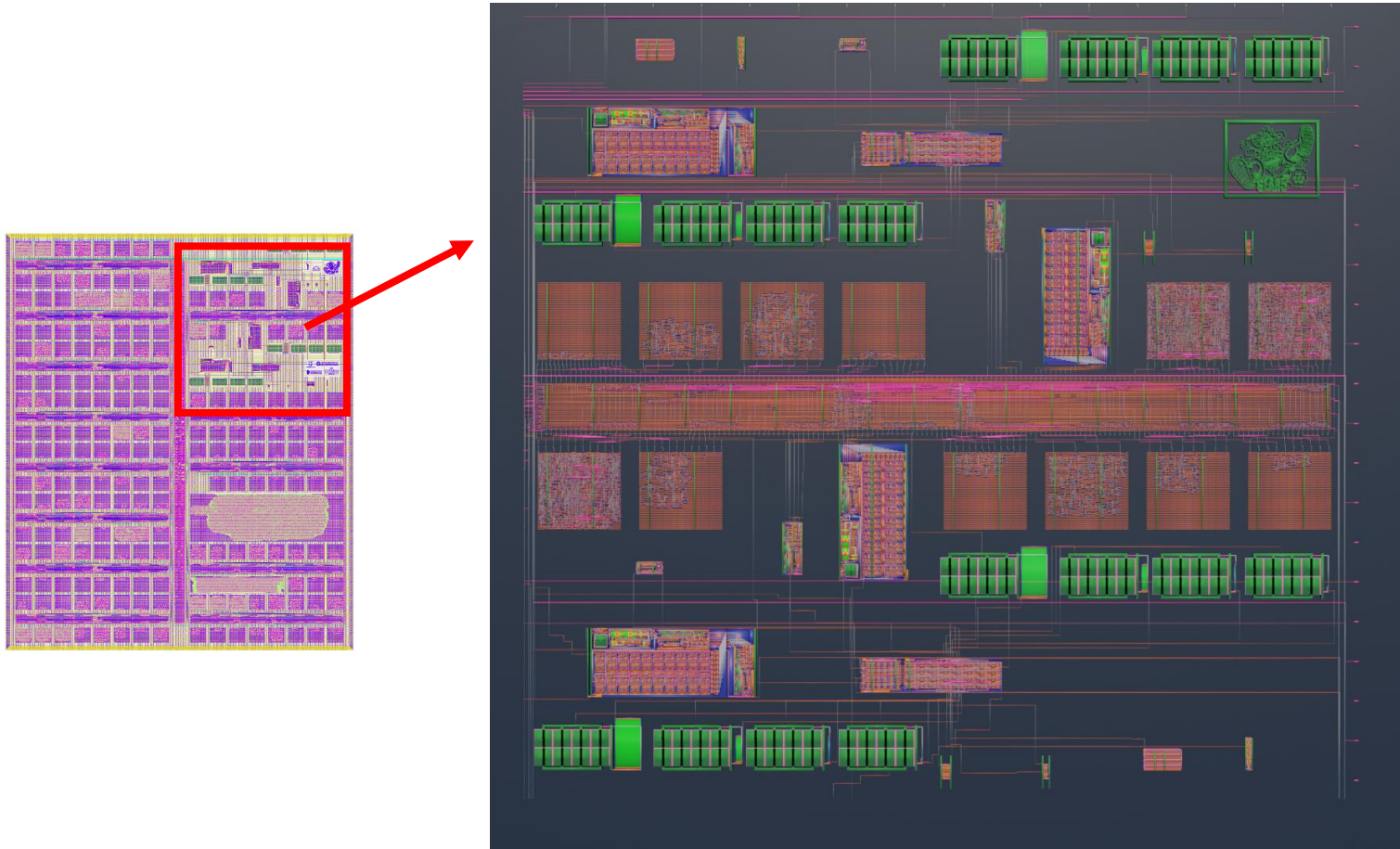
•Finally, version 2 kept the 256 modules but added the capability to include up to **48 analog or mixed-signal blocks**, enabling more complete characterization.

# International Recognition of Silicluster

Silicluster has gained international visibility with three IEEE 2025 conference publications: **APCCAS in South Korea, VLSI-SoC in Chile, and LAEDC in Mexico**, establishing it as a notable platform for integrated-circuit design



# Analog Circuits Designed for Siliclusterv2

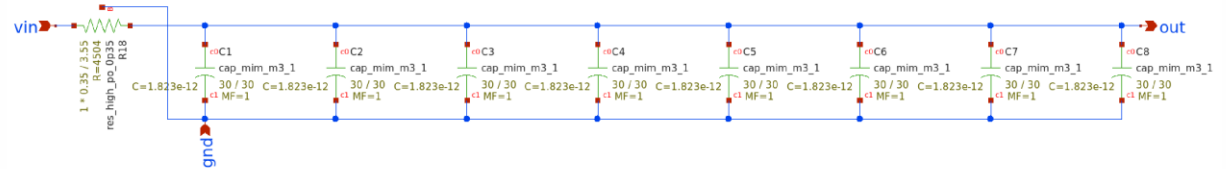


- Low-pass filters
- Ring oscillators
- Buffer
- Inverter
- Operational amplifier
- Analog demultiplexer

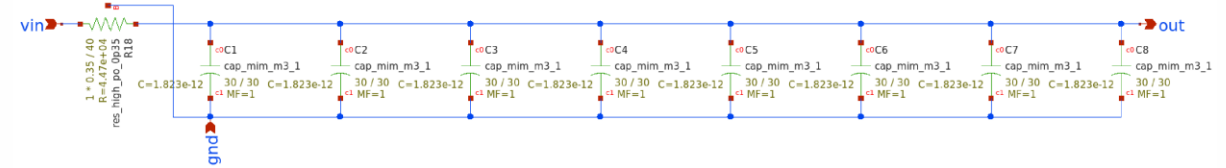
# RC Low-Pass Filters

- The four low-pass filters were implemented using eight parallel capacitors while maintaining the same total capacitance.
- Different cutoff frequencies were obtained by modifying only the resistance, achieving  $-3$  dB points from a few kHz up to several MHz.
- Simulations confirmed the expected behavior, and the layout showed a compact integration compatible with SKY130.

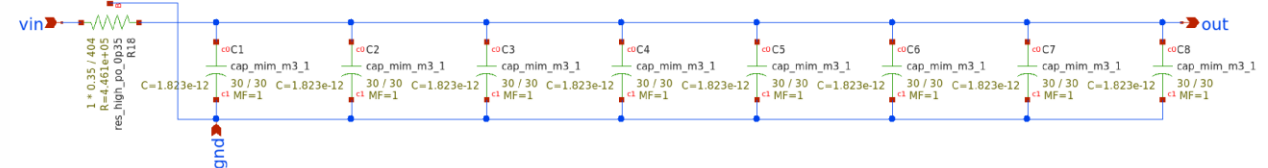
Frecuencia de corte 2.43 Mhz



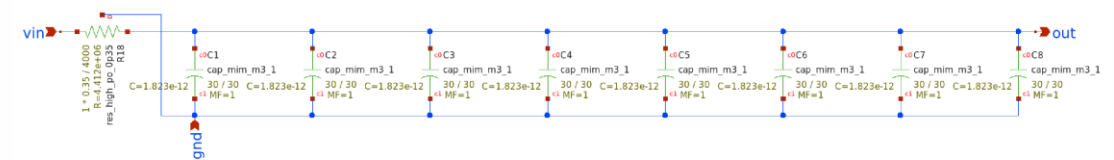
Frecuencia de corte 243 khz



Frecuencia de corte 24.3 khz

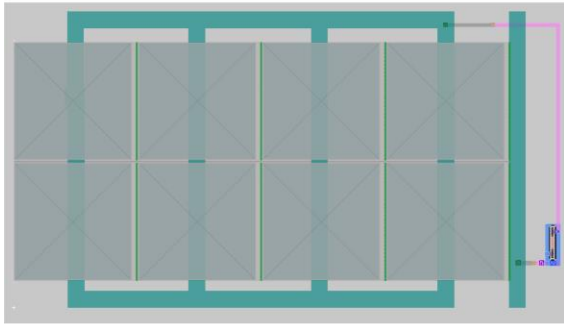


Frecuencia de corte 2.43 khz

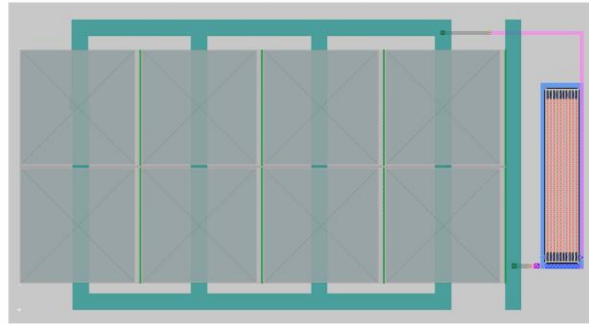


# Low-Pass Filters

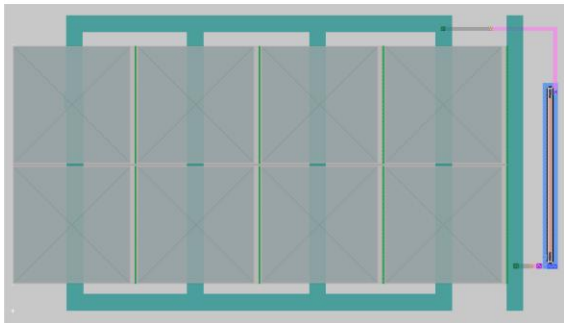
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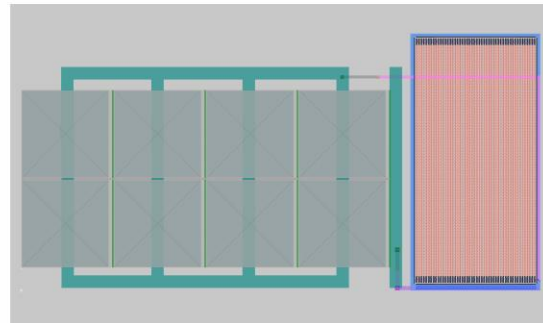
Frecuencia de corte 24.3 khz



Frecuencia de corte 243 khz

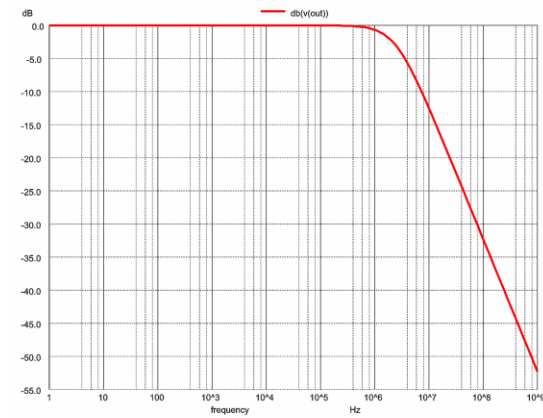


Frecuencia de corte 2.43 khz

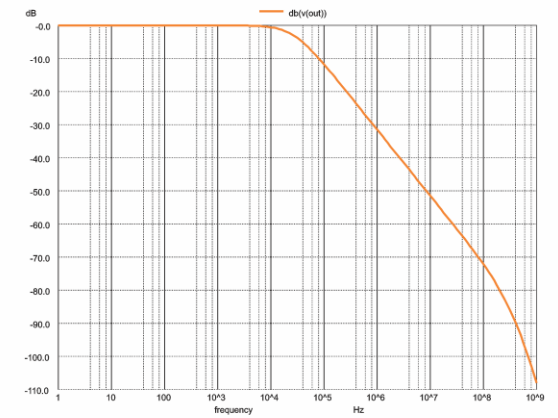


## Layouts

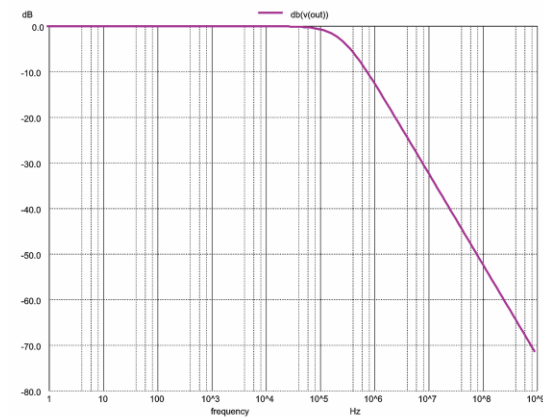
Frecuencia de corte 2.43 Mhz



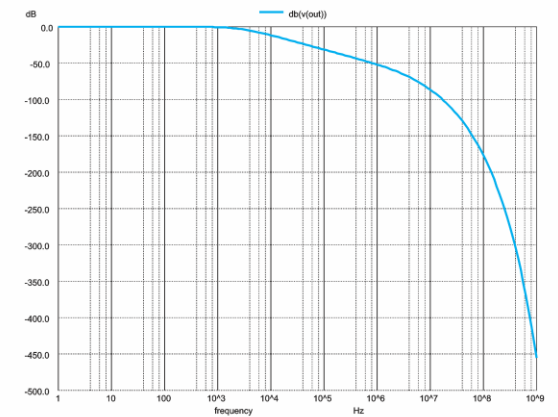
Frecuencia de corte 24.3 khz



Frecuencia de corte 243 Mhz



Frecuencia de corte 2.43 khz

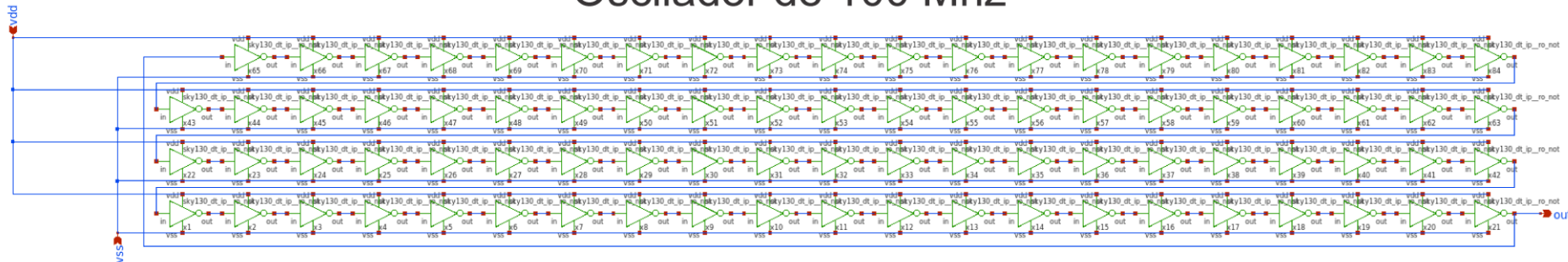


## AC Analysis

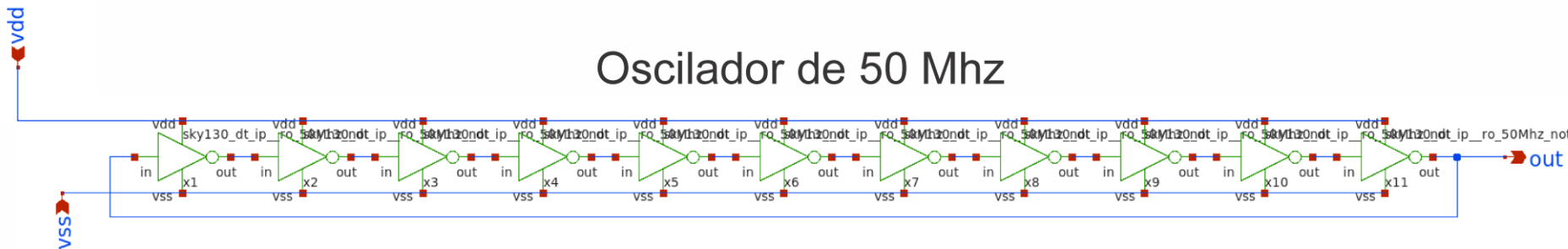
# Ring Oscillators

Two ring oscillators were implemented at 50 MHz and 100 MHz using chains of inverters. Simulations confirmed stable oscillation, and the layout showed a symmetric distribution suitable for SKY130. These blocks enable testing of internal high-frequency signals in an open-source environment.

## Oscilador de 100 Mhz

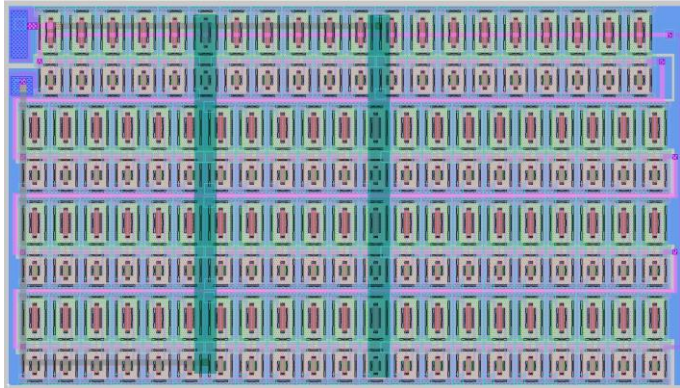


## Oscilador de 50 Mhz

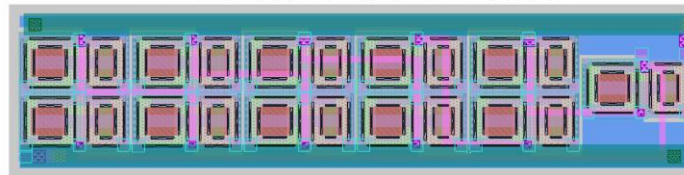


# Ring Oscillators

Oscilador de 100 Mhz



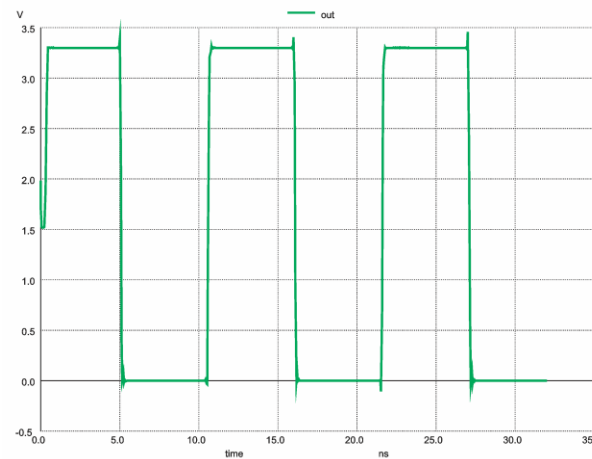
Oscilador de 50 Mhz



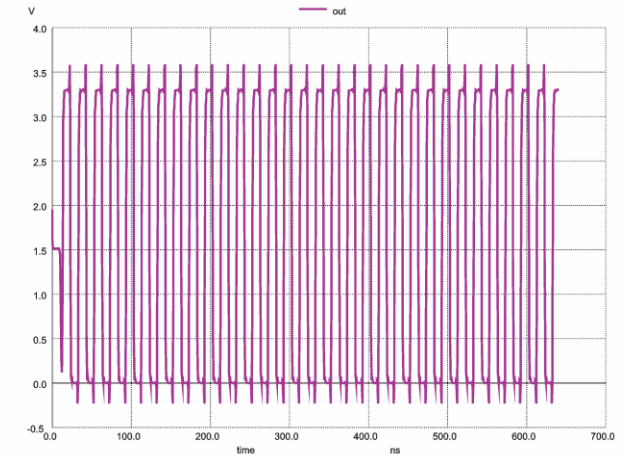
## Layouts

## Transient Analysis

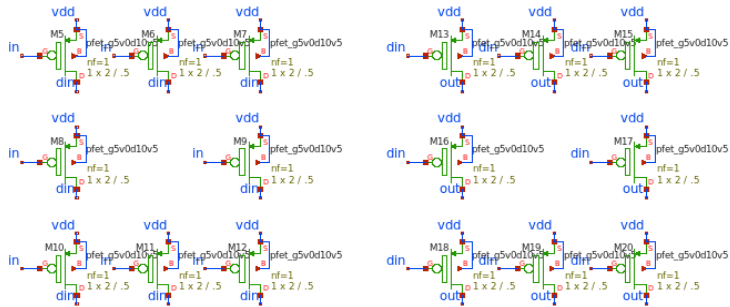
Oscilador de 100 Mhz



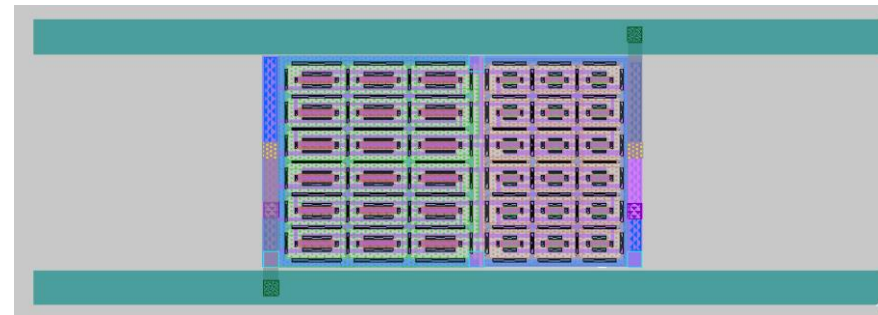
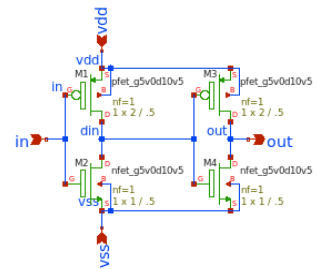
Oscilador de 50 Mhz



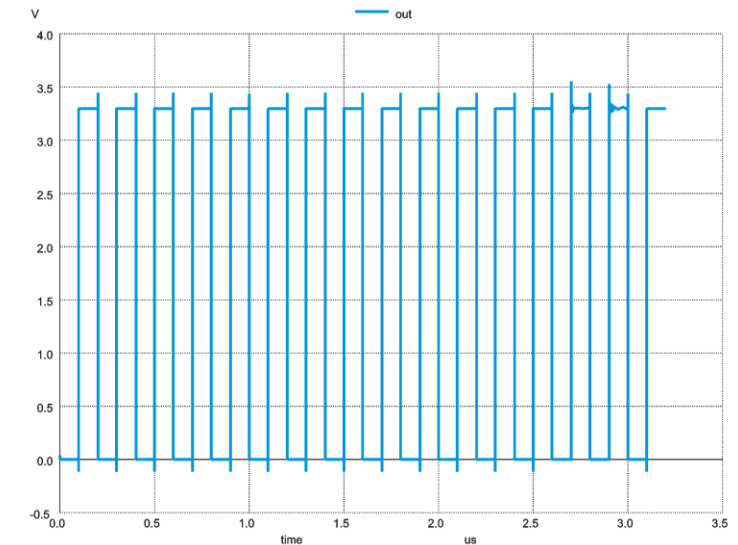
# Buffer



- A buffer was implemented using discrete SKY130 transistors, designed as a simple, compact stage. Transient simulations show stable response to input variations, and the layout meets process-design rules.
- This block serves as a reference for evaluating small conditioning stages inside Siliclusterv2.



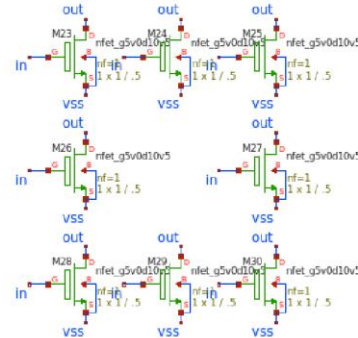
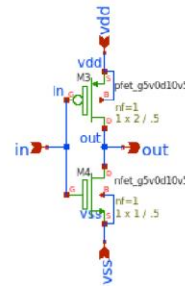
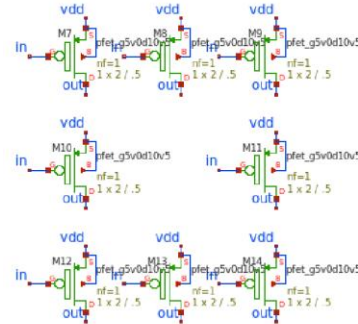
Layout



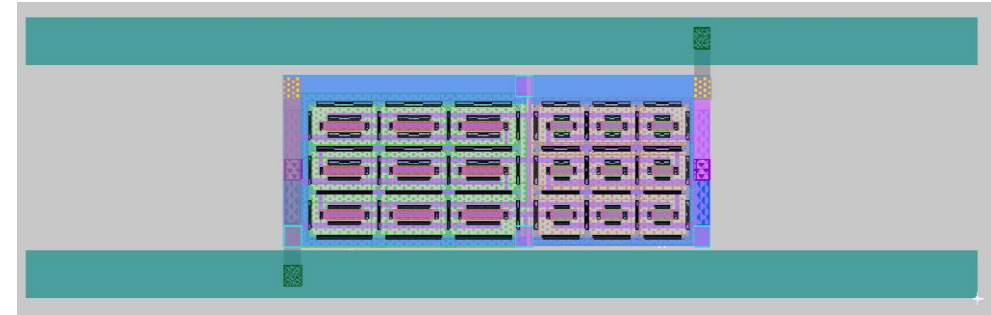
Transient Analysis

# Inverter

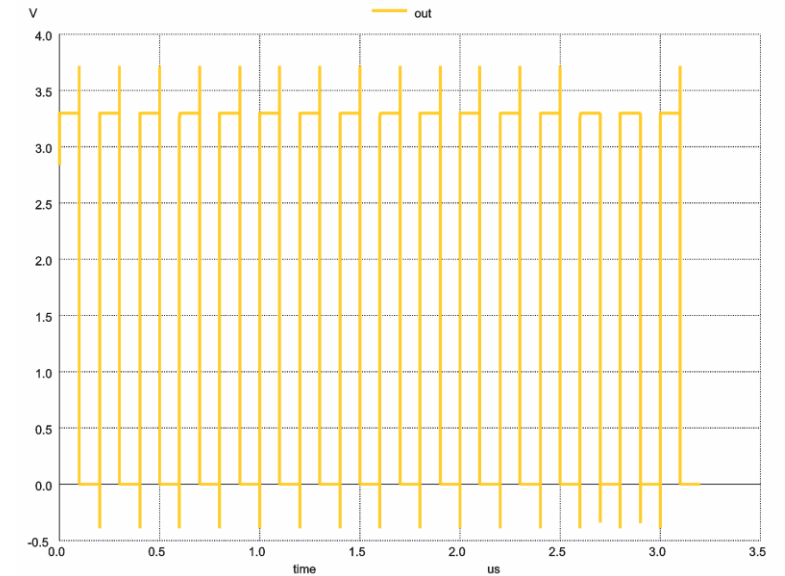
- An inverter was integrated with dummy transistors on the edges to improve matching and reduce edge effects in a compact area.
- Simulations show stable switching, and the layout demonstrates a symmetric arrangement with properly placed dummies.
- This block enables evaluation of how physical design influences switching behavior in SKY130.



Schematics



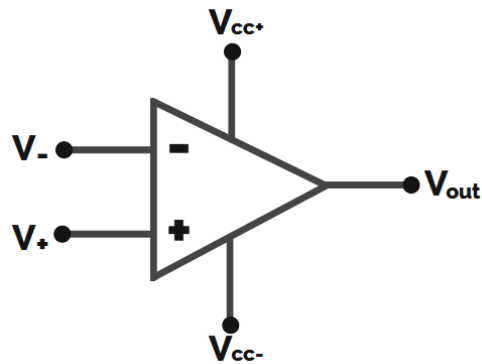
Layout



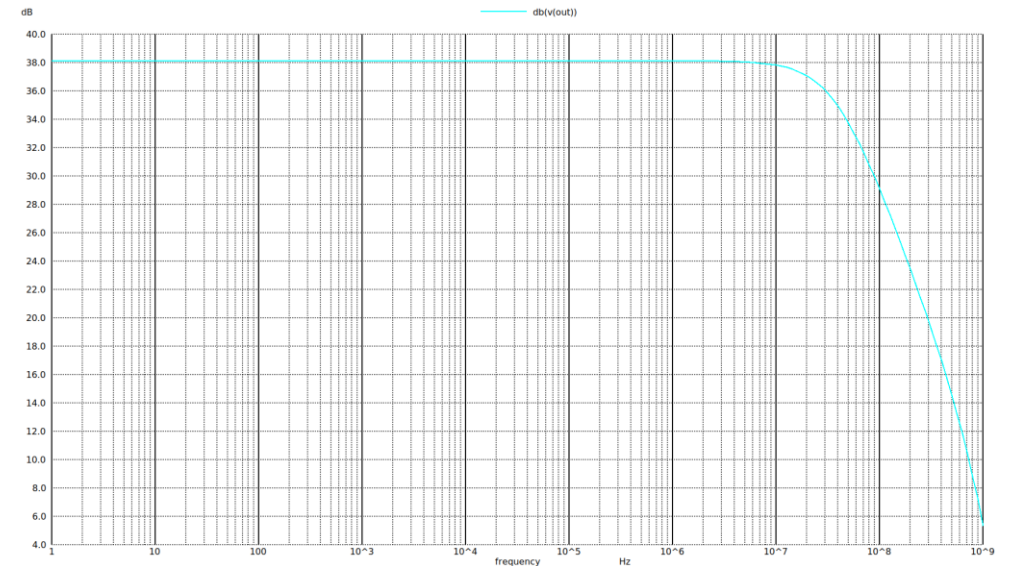
Transient Analysis

# Two-Stage Analog Operational Amplifier

- The open-loop gain of the amplifier was measured at **38 dB**.
- The linear-gain bandwidth extends up to **7 MHz**.
- The cutoff frequency is measured at **400 MHz**.

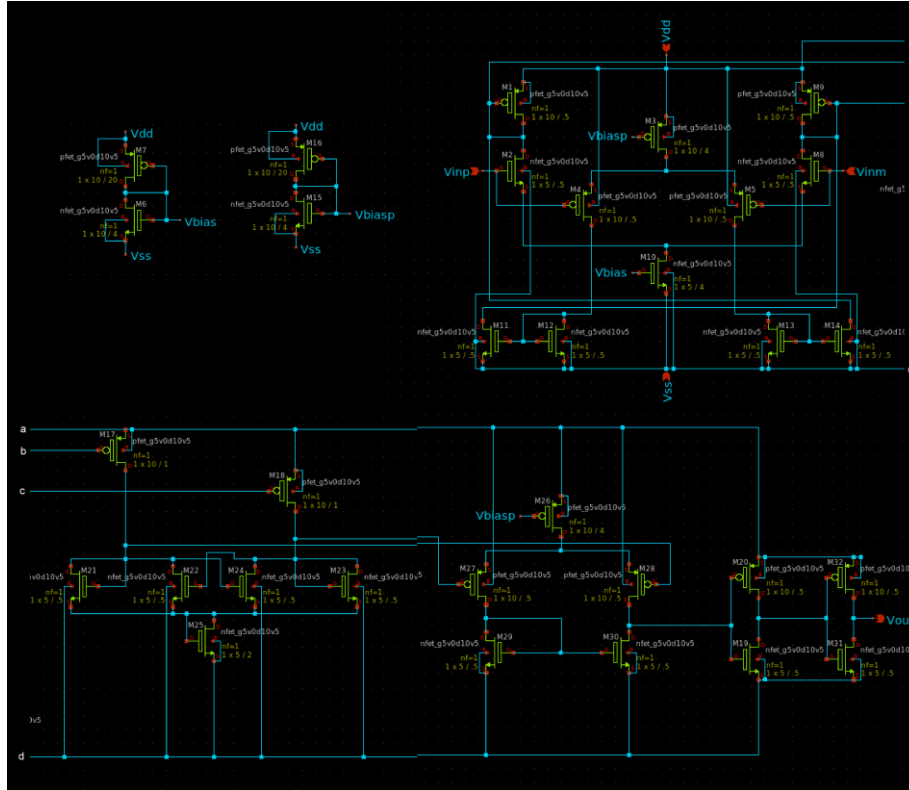


Opamp

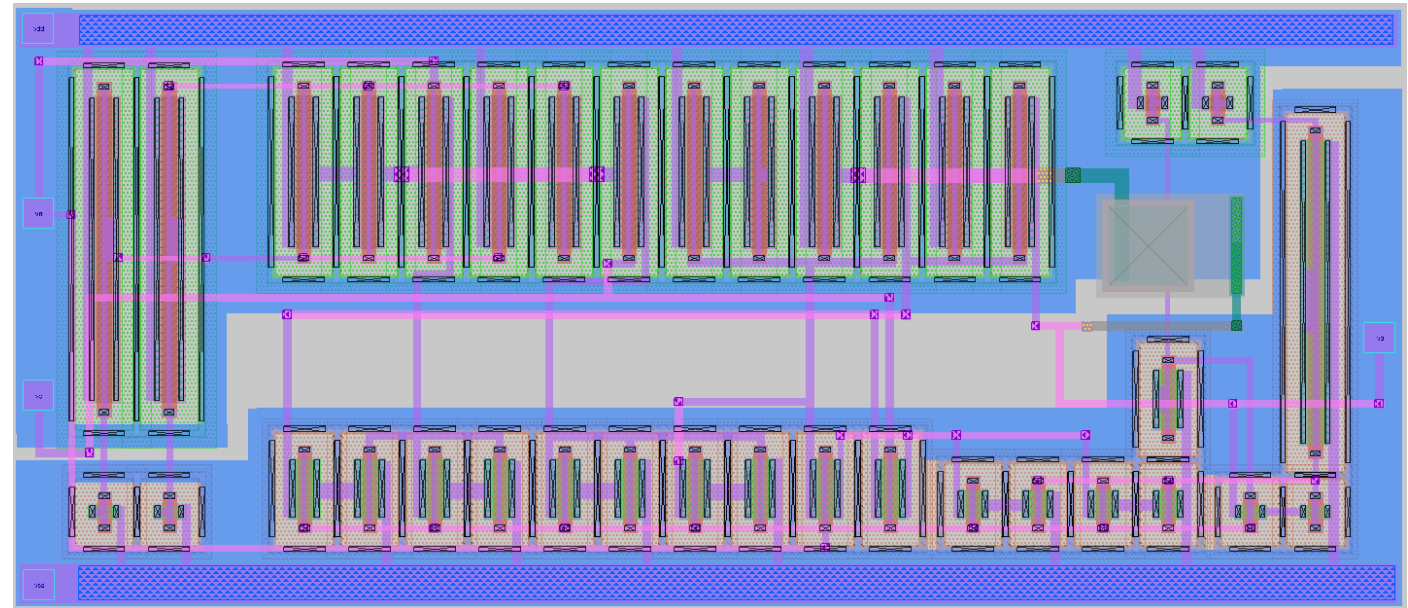


AC Analysis

# Two-Stage Analog Operational Amplifier



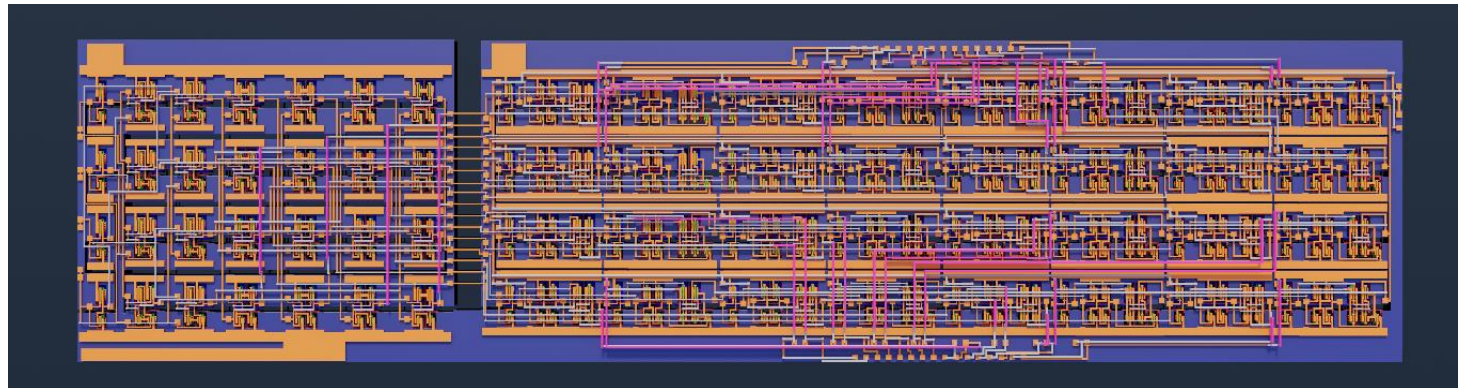
Schematic



Layout

# Analog Multiplexer

- The analog multiplexer connects each analog block to a common input and output line. It operates in the analog domain at **3.3 V**, allowing the selected blocks to directly deliver their signal to the outside without requiring additional interface stages.



Render — Analog Demultiplexer Layout



## SILICLUSTER v2



chipfoundry



Dugalba Tec

Siliclust also includes digital and mixed-signal designs such as:

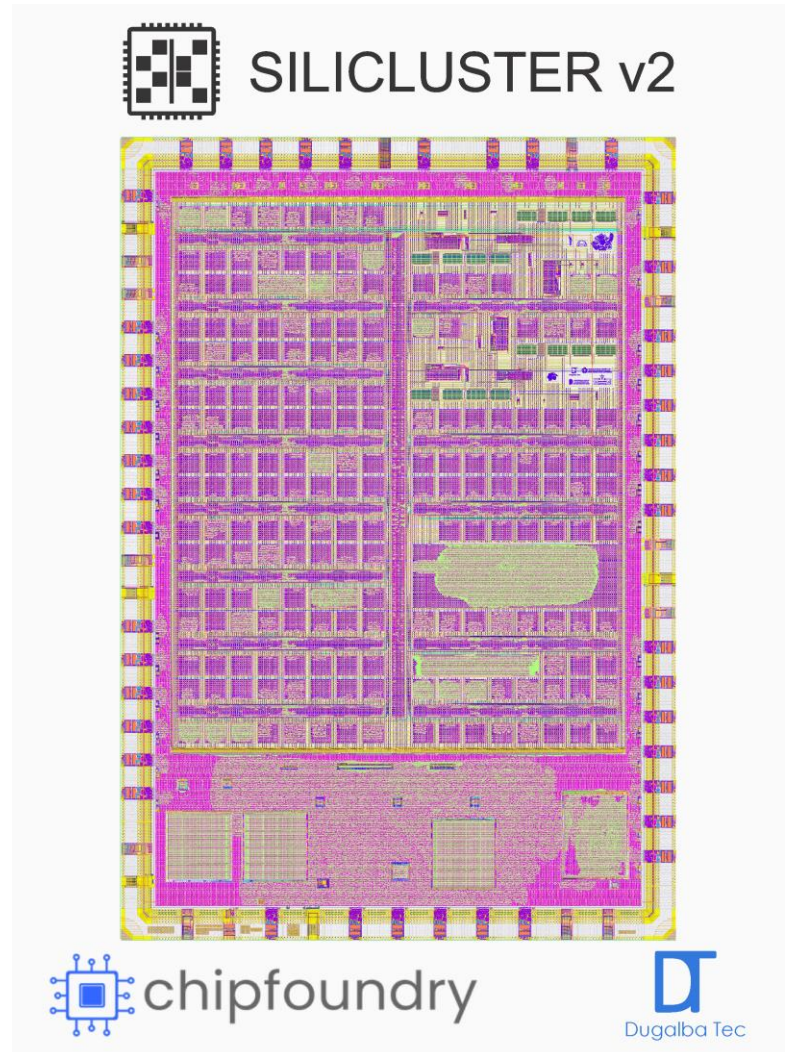
- A 4-bit Flash Analog-to-Digital Converter (ADC) and an 8-bit Successive Approximation Register (SAR) ADC.
- An 8-bit R-2R Digital-to-Analog Converter (DAC).
- 16-bit counters.
- Neural networks.
- State Machines.
- Encryptors, among others.

# Conclusion

- This work demonstrated that it is possible to integrate several compact analog modules into a single chip using only open-source tools and the SKY130 technology.

The filters, oscillators, buffer, inverter, and operational amplifier were implemented and validated through simulation and layout within Siliclusterv2, confirming stability and compliance with physical-design rules.

- These results show the maturity of the open-source ecosystem for analog design and enable the integration of more complex circuits in future versions of the project.



Thank you very much for your attention!  
Any questions?