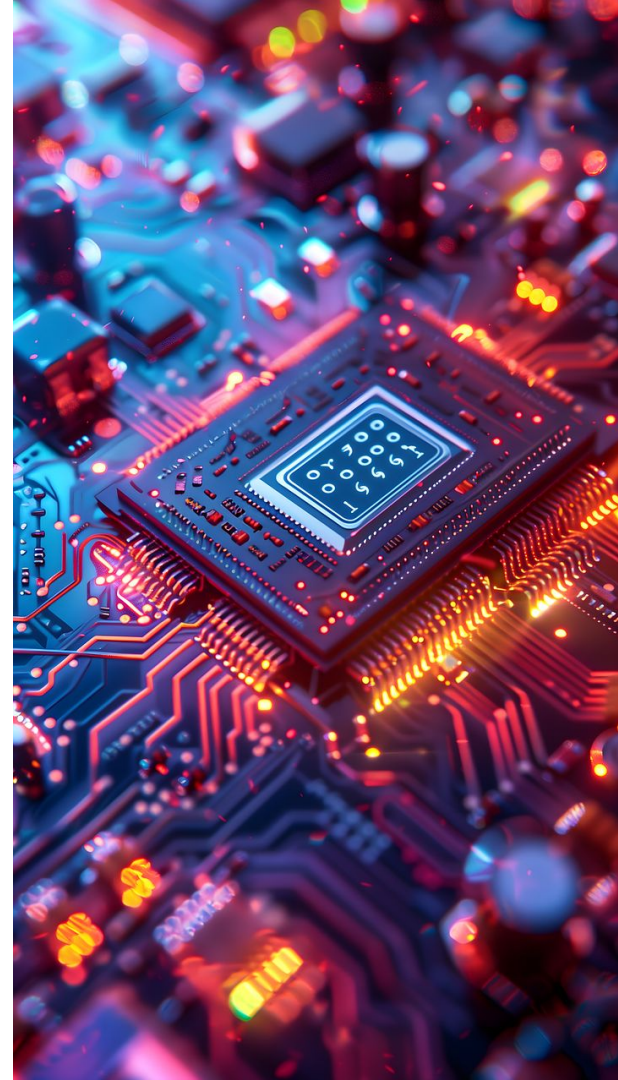


Building an Ecosystem Through IC Education in Colombia: A Model for Emerging Semiconductor Regions

Juan Sebastián Moya Baquero -
SymbioticEDA



About me

- 03/2025: AMS Designer at SymbioticEDA
- 2024: Researcher at MICL - University of Michigan
- 2023: Ph.D.
- 2016: Master in Electrical Engineering - IC Area
- 2011: Electronics and Electrical Engineer



About me

- 2025-2
Professor

Introduction to IC design - Analog Flow (8 weeks) - gf180mcuD
Digital IC design (8 weeks) - ihp 130



- 2023-1:
Professor
IC design - sky130A



- 2017 - 2022:
Professor

Electronics Devices (Semiconductors, PN junction, BJT, AC and DC MOSFET model).

Electronics System Design (Negative feedback, stability, frequency compensation and noise)



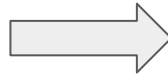
IC design Flow - Proprietary CAD tools

cādence[®]



Tools license → \$10,000 - \$100,000
Virtuoso → \$15,000 per license
In some countries in Latam, no possibility to access directly the tools. Via third party.

SYNOPSYS[®]
Silicon to Software™



Tools license → \$20,000 - \$100,000
Chile (Victor Grimblatt) → Prices are affordable in Latam

SIEMENS **Mentor**[®]
A Siemens Business



Tools license → \$1,000s - \$10,000s

Taken from : https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/training/training-na-catalog-price-list.pdf
<https://c2s2.engineering.cornell.edu/blogposts/SP23/MagicVLSIvsCadenceVirtuoso#:~:text=If%20you%20want%20to%20be,the%20tool%20outside%20of%20industry.>
<https://www.quora.com/How-much-is-a-single-license-of-mentor-graphics-synopsys-or-cadence-electronic-design-automation-software>

IC design Flow - PDK access

MUSE SEMICONDUCTOR

It's not just an MPW.

TSMC MPW FULL BLOCK TAPEOUTS

We support all TSMC technologies. Some of the most popular are below.

	180 MS RF G	180 HV BCD G2	130 MS RF G	65 MS RF GP/LP	40 MS RF G/LP
Price (\$/mm ²)	1,000	1,160	1,800	4,625	7,000
	28 HPC+ RF	22 ULL	16 FFC	12 FFC	7 FF
Price (\$/mm ²)	10,600	10,600	28,000	28,000	87,500



AMF Silicon Photonics General-Purpose Fabrication Process



\$22,000
(per 3 mm x 8 mm design)

AMS 0.35 μ m CMOS Process Technology (Basic)



\$998/mm²
(Minimum charge is for a 10 mm² design)

GlobalFoundries[®] 12 LP



\$37,050/mm²
(Minimum charge is for a 1 mm² design)

\$29,952/mm²
(Minimum charge is for a 9 mm² design)

Note: This price is available only to academic researchers.

Tomado de :

<https://www.musesemi.com/dedicated-mask-tapeouts>

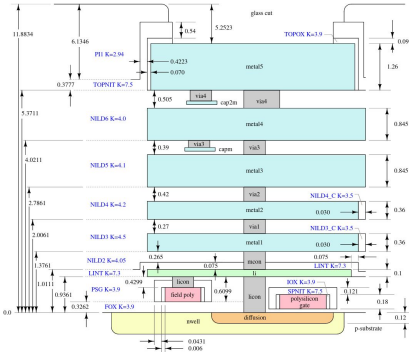
<https://www.cmc.ca/technologies/>

Open Source PDKs

2020



FOSS 130nm Production PDK
github.com/google/skywater-pdk



1.8V/ 5V/ 10V

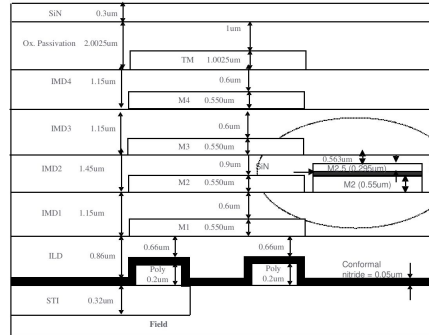
poly, high-res poly,
N-well, P-well

MIM capacitor,
varactors, poly
capacitors.

2022



FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

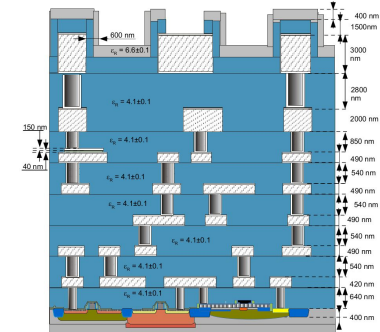


3.3V/ 5V/ 6V

P+Poly, N+Poly
and HRES
resistors

MIM caps

2023

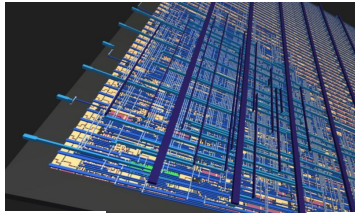


SiGe BiCMOS

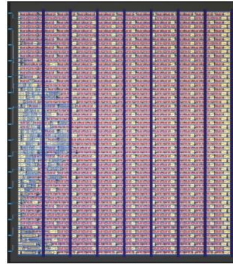
1.2V digital /
3.3 thick oxide

Polysilicon
resistors / MIM
caps

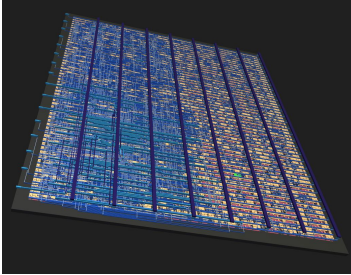
Tiny Tapeout 3 (2023)



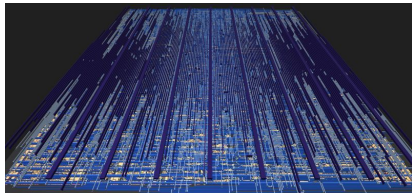
Pseudo Random
Number Generator



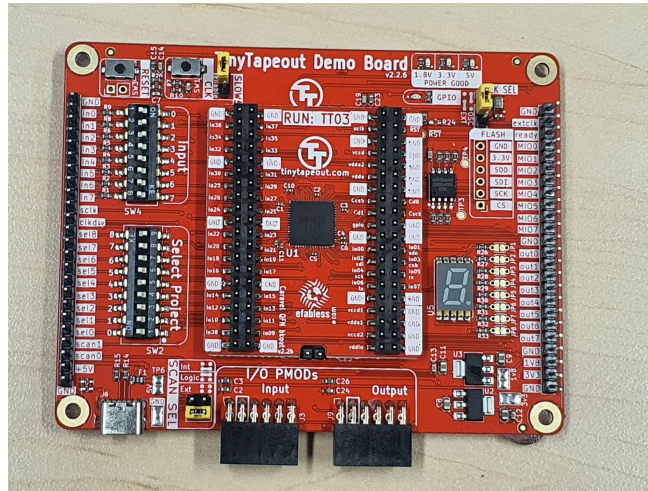
Microrobot /Finite State Machine



Programmable Finite
State Machine

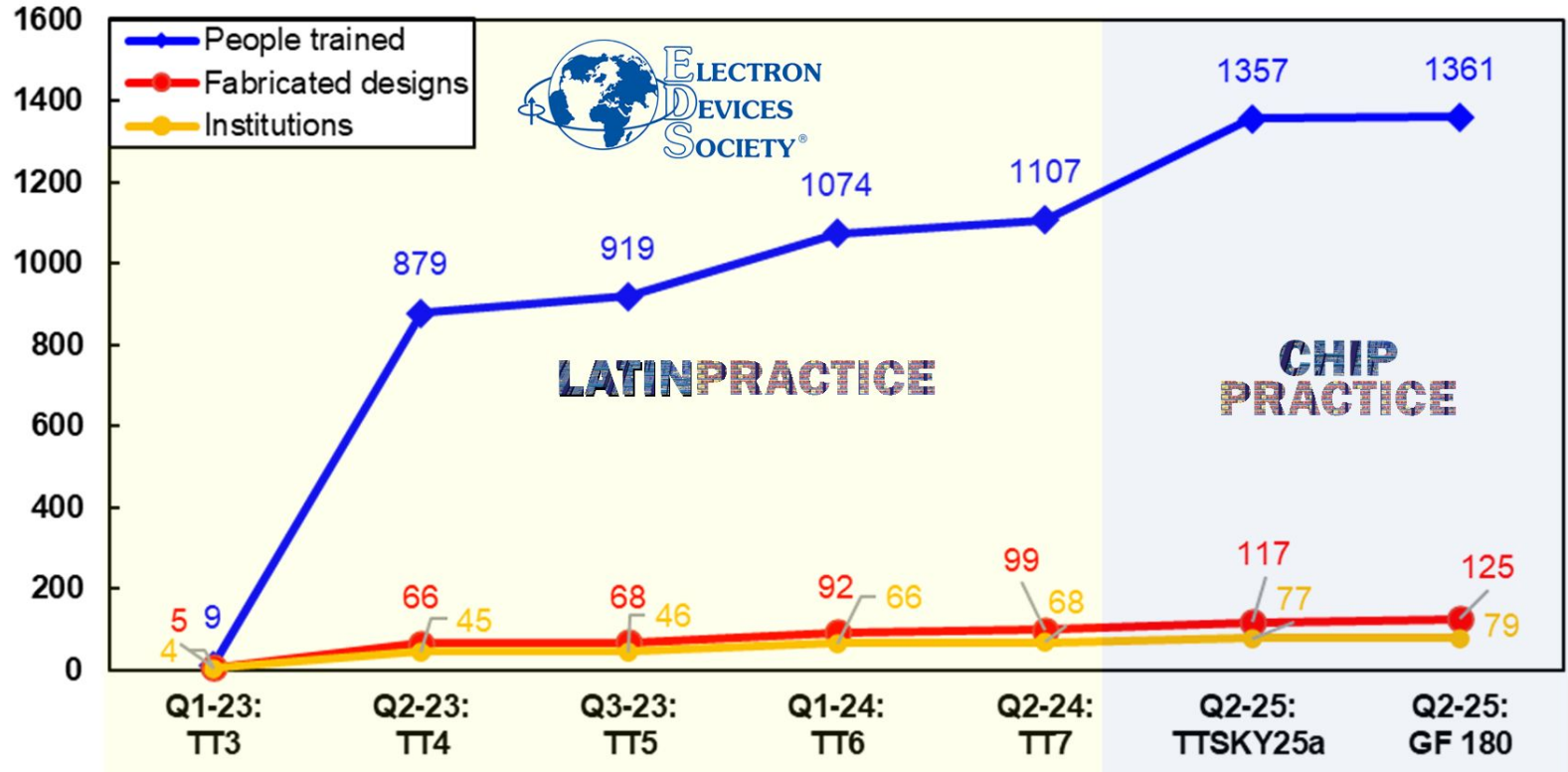


Digital Temperature sensor



125	124	126	133	127	122	128	121	129	120	130	119	131	118
111	138	112	137	113	136	114	135	115	134	116	133	117	132
139	110	140	109	141	108	142	107	143	106	144	105	145	104
97	152	98	151	99	150	100	149	101	148	102	147	103	146
153	96	154	95	155	94	156	93	157	92	158	91	159	90
83	166	84	165	85	164	86	163	87	162	88	161	89	160
167	82	168	81	169	80	170	79	171	78	172	77	173	76
69	180	70	179	71	178	72	177	73	176	74	175	75	174
181	68	182	67	183	66	184	65	185	64	186	63	187	62
55	194	56	193	57	192	191	190	189	188	187	186	185	184
195	54	196	53	197	52	198	51	199	50	200	49	201	48
41	208	42	207	43	206	44	205	45	204	46	203	47	202
209	40	210	39	211	38	212	37	213	36	214	35	215	34
27	222	28	221	29	220	30	219	31	218	32	217	33	216
223	26	224	25	225	24	226	23	227	22	228	21	229	20
13	236	14	235	15	234	16	233	17	232	18	231	19	230
237	12	238	11	239	10	240	9	241	8	242	7	243	6
0	249	1	248	2	247	3	246	4	245	5	244	0	243

Some numbers



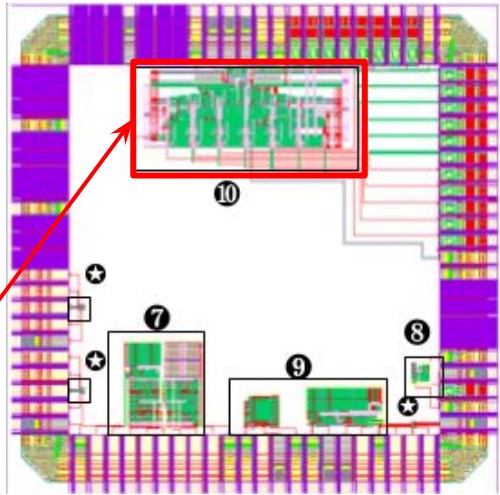
SSCS Contests

Chipathon 2023



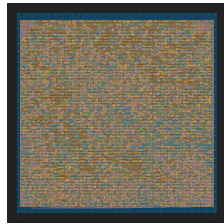
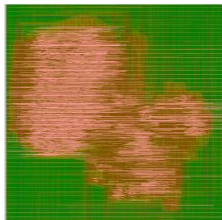
BRACOLIN - 2023 SSCS PICCO OPEN-SOURCE CHIPATHON	
UFSC - LCI:	UNIANDÉS - CMUA:
GABRIEL MARANHÃO SOARES	JUAN SEBASTIÁN MOYA BAQUERO
DENI GERMANO ALVES NETO	FREDY SEGURA QUIJANO
CESAR AUGUSTO MARCELO ALBUQUERQUE	
AUGUSTO DE PAULO FRANCO	
FELIPE HUGO COSTA DE OLIVEIRA	
THIAGO HENRIQUE SANTOS	
NATANAEL RISSI BERTAMONI	

FIGURE 4: "Team Odin": team snapshots.



- ⑦ Current controlled band-pass filter
- ⑧ Clock reference generator (1MHz)
- ⑨ 1.3V Voltage Reference (left) & Vout=1.65V LDO (right)
- ⑩ SAR ADC
- ★ Short Channel transistors (characterization)

Code-a-Chip



GreenRio 2: A Linux-compatible RISC-V processor developed with a fully open-source EDA flow. ([link](#))

Coordinate rotation computer (CORDIC) with OpenLane. ([link](#))

2025 TC-OSE @ CAC y Chipathon

2025 Technical Committee on the Open-Source Ecosystem



Boris Murmann
Univ. Hawaii
USA



Mehdi Saligane
Brown University
USA



Mitch Bailey
Indep. Contractor
Japan



Kwantae Kim
Aalto University
Finland



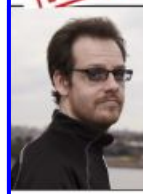
Ali Sabir
FAST-NUCES
Pakistan



Jorge Marin
U Tec. Federico
Chile



Juan S. Moya
Symbiotic EDA
Colombia



Tim Ansell
ARC PBC
USA



Saptarshi Ghosh
ETH Zurich
Switzerland



Matt Venn
Chipflow
Spain



Harald Pretl
Kepler Univ., Linz
Austria



Sadayuki Yoshitomi
Rapidus
Japan



Tim Edwards
Efabless
USA



Jun-Ichi Okamura
AIST Solutions
Japan



Akira Tsuchiya
University of Shiga
Japan

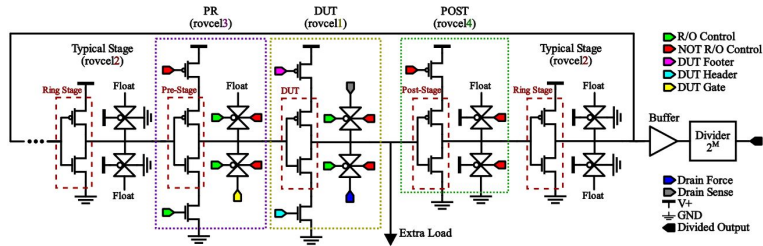


Gregory Kielian
Google
USA

UNIC-CASS contest

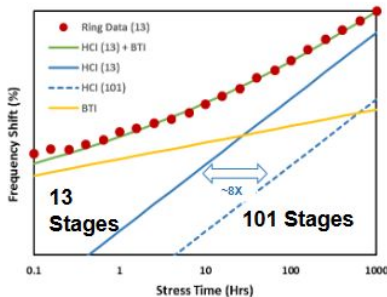
2024 (sky130)

UNIC-CASS Material



Ring Oscillator Frequency Shift

Frequency shift is a combination of low time slope BTI and high time slope HCI shift



From: HC_BTI_RingOsc_Overview. Fernando Guarín



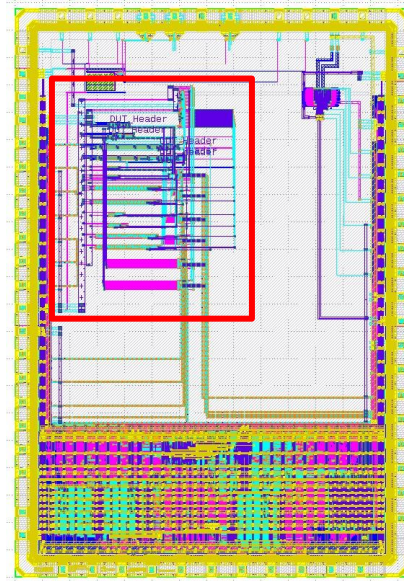
Jeison Acevedo
(Est. MSc. UIS)



Jorge Angarita
(Est. MSc. UIS)



Eduardo Caballero
(Est. MSc. UIS)



Juan S. Moya
(Investigador UMich)



Nestor Matajira
(Ingeniero UIS)



Ramón Stiven Sarmiento
Castro (Estudiante UIS)



Nicolas Orcasitas Garcia
(Ingeniero UIS)



Daniel Barrios
(Ingeniero UIS)

Workshops in 2024 and 2025 (COL)

2024

Onsilicon

42 participants

Workshop
Diseño de Circuitos Integrados

Introducción al

Diciembre 12 y 13 de 2024
Universidad Nacional de Colombia
Sede manizales

Evento Gratuito

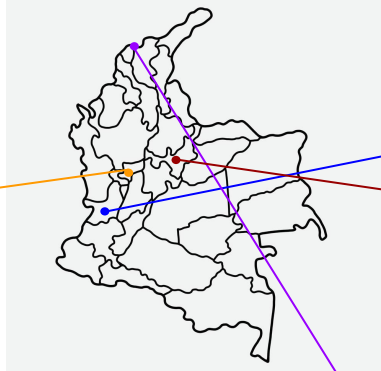
Aprenda a diseñar de manera práctica un chip analógico y digital usando herramientas libres y propietarias

Cupos limitados

Organizan: IEEE Colombia Section, CAS, Universidad Nacional de Colombia, Con el apoyo de

75 años CAS IEEE Colombia Section

https://forms.gle/Sy8oCm93Q1t1z9



2025

Symbiotic EDA

16 participants
Oct. 27th and 28th

COLOMBIAN WORKSHOPS
ON INTEGRATED CIRCUIT
DESIGN FOR BEGINNERS

INSTITUCION UNIVERSITARIA DE BARRANQUILLA
SEDE PLAZA DE LA PAZ

OCTOBER 27-28

SPEAKERS:

DR. JORGE IVAN ARRIN HURTADO
PROFESSOR OF THE COLLEGE OF ENGINEERING AND TECHNOLOGY OF BARRANQUILLA, INSTITUCION UNIVERSITARIA DE BARRANQUILLA

DR. JUAN SEBASTIAN ROYA BAQUERO
LEADS SEVERAL COURSE DESIGN AND DEVELOPE THE INTEGRATED CIRCUIT DESIGN OF THE UNIVERSITY OF BARRANQUILLA

HOST: CAS, IEEE ColCaribe, REIP

JOIN HERE

45 participants

Sept. 1st and 2nd

Workshop
Diseño de Circuitos Integrados
para principiantes

Septiembre 1 y 2 de 2025

Pontificia Universidad Javeriana Cali

Evento Gratuito

Aprenda a diseñar de manera práctica un chip usando herramientas libres

Cupos limitados

Organiza: CAS, IEEE Colombia Section, Pontificia Universidad Javeriana Cali

31 participants
Nov. 11th and 12th

Uptc
Universidad Pedagógica y Tecnológica de Colombia

10 de noviembre de 2025

Workshops in 2024 and 2025 (COL)

2024



42 participants

Workshop
Diseño de Circuitos Integrados

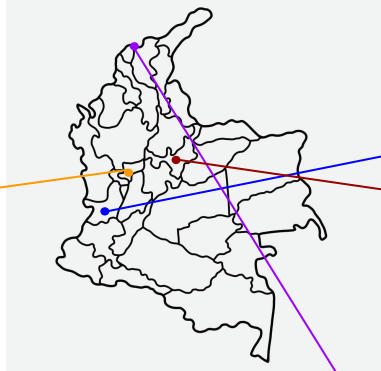
Introducción al

Diciembre 12 y 13 de 2024
Universidad Nacional de Colombia
Sede manizales

Evento Gratuito

Aprenda a diseñar de manera práctica un chip analógico y digital usando herramientas libres y propietarias

Cupos limitados



134 participants trained in both digital and analog IC flows (fundamentals courses).

2025



16 participants
Oct. 27th and 28th

COLOMBIAN WORKSHOPS
ON INTEGRATED CIRCUIT
DESIGN FOR BEGINNERS

INSTITUCIÓN UNIVERSITARIA DE BARRANQUILLA
SEDE PLAZA DE LA PAZ

OCTOBER 27-28

SPEAKERS:

DR. JORGE IVAN ARRIN HURTADO
PROFESOR DE LA ESCUELA DE INGENIERÍA DE SISTEMAS DE INFORMACIÓN Y TELECOMUNICACIONES, INSTITUCIÓN UNIVERSITARIA DE BARRANQUILLA

DR. JUAN SEBASTIÁN ROYA BAQUERO
INGENIERO SENIOR CIRCUIT DESIGNER Y CONSULTOR EN ANÁLISIS Y DISEÑO DE LA FÍSICA DE LOS SEMICONDUCTORES EN LA ESCUELA DE INGENIERÍA DE SISTEMAS DE INFORMACIÓN Y TELECOMUNICACIONES, INSTITUCIÓN UNIVERSITARIA DE BARRANQUILLA

HOST:

CAS IEEE ColCaribe REIP

JOIN HERE

45 participants

Sept. 1st and 2nd

Workshop
Diseño de Circuitos Integrados para Principiantes

Septiembre 1 y 2 de 2025

Pontificia Universidad Javeriana Cali

Evento Gratuito

Aprenda a diseñar de manera práctica un chip usando herramientas libres

Cupos limitados

31 participants
Nov. 11th and 12th

Uptc[®]
Universidad Pedagógica y Tecnológica de Colombia

10 de noviembre de 2025

2025 Cherry on Top

CALL FOR APPLICATIONS

IEEE Solid-State Circuits Society & Electron Devices Society Present:

SEED: SEMICONDUCTOR EDUCATION, EMPOWERMENT, & INDUSTRY DEVELOPMENT

The First Grassroots-Level Semiconductor Industry & Education-Based Outreach Program

Who Can Apply?

- Senior PhD students
- Young Professionals
- Junior Faculty

Benefits

- Up to \$5000 USD Travel Grant
- Opportunity to travel to underserved regions
- Professional Growth, Network, and Global Impact.

DEADLINE: SEPTEMBER 26, 2025



JSMB



Jorge Iván Marín



Lorena García

Dec. 1st - 11th

43 participants
5.5 days Workshop



UNIVERSIDAD DEL QUINDÍO

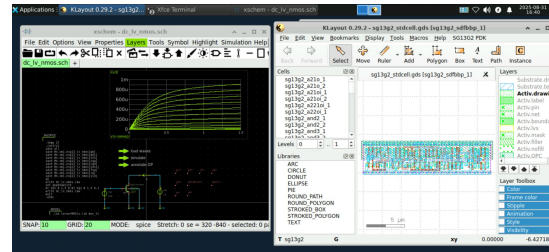
Analog Training



Digital Training

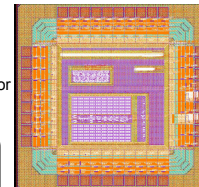


Bluegarden: Environment for IC design and verification using open source tools



SymbioticEDA tapeout with ihp130 TO09/25:

- SPI core
- ADC
- 13- RO and 101-RO for reliability characterization



Digital Flow
Analog Flow
AMS Flow

November 3, 2025

Dear Dr. Moya-Baquero,

Thank you for applying to the IEEE SSCS / EDS Semiconductor Education, Empowerment, and Industry Development (SEED) Program. We are following up on your recent interview with the SEED selection committee members. [Congratulations on your selection to the 2025 roster!](#)

The interviewers enjoyed speaking with you regarding your plans for student outreach in **Columbia** and your plans for a workshop and engagements at the university level. They are looking forward to learning more about the outcome of this visit, your report that will highlight the results of the engagement and your recommendations for future longer term engagements. The selection committee encourages you to include a high-school visit to your itinerary and outreach plans.



2025 Cherry on Top

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JSMB

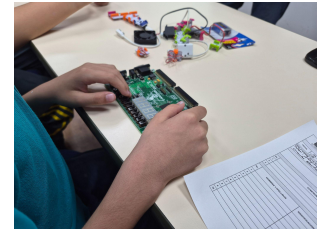
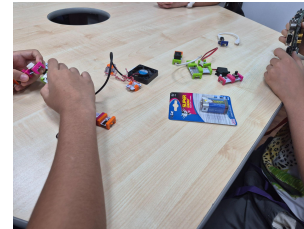


Jorge Iván Marín



Lorena García

Dec. 1st - 11th



2025 Cherry on Top

CALL FOR APPLICATIONS

IEEE Solid-State Circuits Society & Electron Devices Society Present:

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JSMB



Jorge Iván Marín

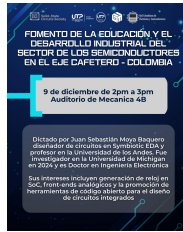


Lorena García

Dec. 1st - 11th



Universidad Tecnológica



UNIVERSIDAD NACIONAL DE COLOMBIA SEDE MANIZALES



Measurement Environments For Everyone, Everywhere



Ingeniería especializada a la medida

Visit to local electronics industry with the possibility to develop ASIC solutions with OS tools

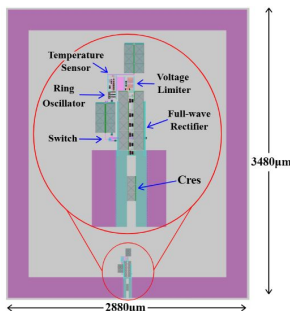
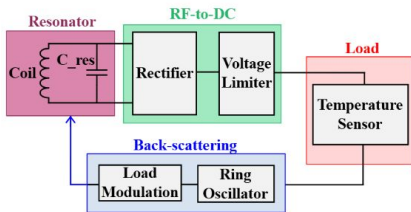


Undergrad Thesis 2023 (sky130)

Senior applications Engineer (Synopsys)

Block Design for an RFID Integrated Tag in an Open-Access Technology Node.

Antony Sanabria Calderón, **Karla Camacho Mercado**, Juan Sebastián Moya Baquero* and Ernesto Aguilera Bermúdez[†]
 *Integrated Systems Research Group - OnChip, Universidad Industrial de Santander, Bucaramanga - Colombia
[†] Research Group - RadioGis, Universidad Industrial de Santander, Bucaramanga - Colombia
 antony2180367@correo.uis.edu.co, karla2180397@correo.uis.edu.co,
 juan2178217@correo.uis.edu.co, eaguilera@uis.edu.co



Master's student at Dresden University of Technology + Testing Engineer (Intern) at Infineon

Open-source standard cell and I/O cell design

Jhon Steven Pinto, Nelson Rodríguez, Juan Sebastián Moya, Jaime Barrero
 Integrated Systems Research Group - OnChip, Universidad Industrial de Santander, Bucaramanga - Colombia
 jhon2180408@correo.uis.edu.co, nelson.rodriguez4@correo.uis.edu.co,
 juan2178217@correo.uis.edu.co, jbarrero@c3t.uis.edu.co

Universidad Industrial de Santander

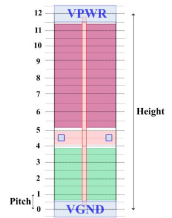
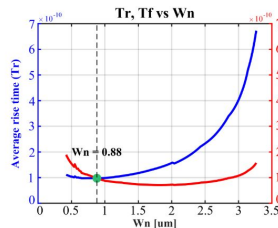
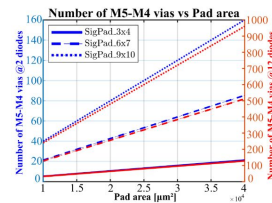
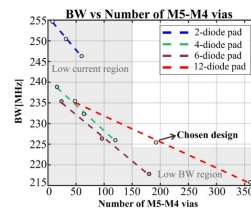
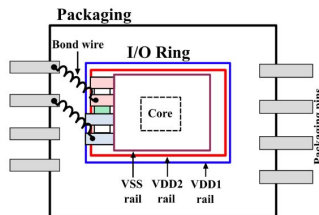


Fig. 1: An standard cell of 12-track height.



Cell	Area	Function
INV	8.83	!A
BUFF	11.04	A1
NAND2	11.04	!(A1 & B1)
NOR2	11.04	!(A1 B1)
AOI21	15.46	!((A1 & A2) B1)
OAI21	15.46	!((A1 A2) & B1)
AOI22	19.87	!((A1 & A2) (B1 & B2))
OAI22	19.87	!((A1 A2) & (B1 B2))
AOI211	19.87	!((A1 & A2) B1 C1)
OAI211	19.87	!((A1 A2) & B1 & C1)



Politics in Colombia

Asunto: Radicación Proyecto de Ley por la cual se fomenta la industria electrónica y de semiconductores en Colombia.

Respetados señores,

Por medio de la presente nos permitimos radicar el Proyecto de Ley “Por la cual se fomenta la industria electrónica y de semiconductores en Colombia”.

De manera atenta solicitamos respetuosamente iniciar el trámite correspondiente, en cumplimiento de las disposiciones previstas en la Constitución y la Ley, conforme el siguiente articulado y la respectiva exposición de motivos.

Cordialmente,

ARTÍCULO 1. Objeto. La presente ley tiene por objeto crear condiciones que favorezcan el fortalecimiento del ecosistema de la industria electrónica y de semiconductores, a través de reconocer esta industria como un eslabón estratégico para la soberanía tecnológica y el crecimiento económico del país; fomentar la creación y consolidación de empresas especializadas en electrónica y semiconductores; propender por el entrenamiento y la formación de capital humano nacional; apoyar el desarrollo de procesos de investigación, transformación, comercialización e innovación y crear mecanismos para atraer la inversión nacional y extranjera en el sector, con el fin de apoyar la inserción de Colombia en la cadena de valor global de la industria electrónica.

Approved in second debate in the Senate on August 19, 2025.

Continues its passage through the House of Representatives



Lorena García

Conclusions and Remarks

- OS tools are important for developing the IC design workforce in Latin America.
- OS tools democratise IC design and lower the barriers to accessing manufacturing.
- Great efforts from IEEE are contributing to this OS ecosystem.
- This could be an interesting approach for developing commercial ASICs for the local industry.
- OS tools and flows need to be improved to develop more reliable solutions and attract more attention from industry.

Thanks a lot!

Questions?

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