Silicon-Proven Learning With Open PDKs and MPW Access for IC Education

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Summary

- Motivation and Context
- IC Design Flow (Concept to Silicon)
- Capstone IC Design at USFQ
- Conclusions

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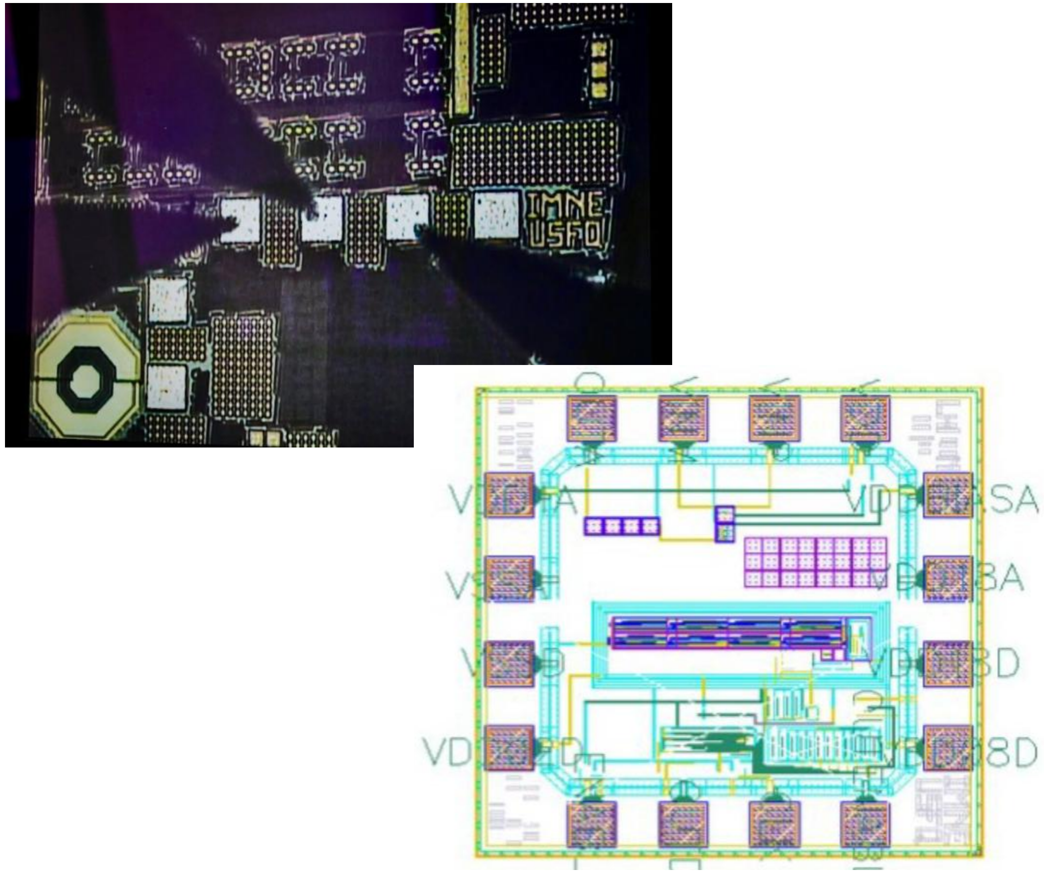
Motivation – Barriers in Latin America

Historically, IC design in countries such as Ecuador has faced:

- High **costs** of EDA tools and fabrication.
- **Strict NDAs** that prevent open academic use.
- A **limited industrial ecosystem**.

In Ecuador:

- Early efforts in the 1990s (1.2 μm CMOS chips) were discontinued due to cost.
- The **first modern microchip** appeared in **2022**.

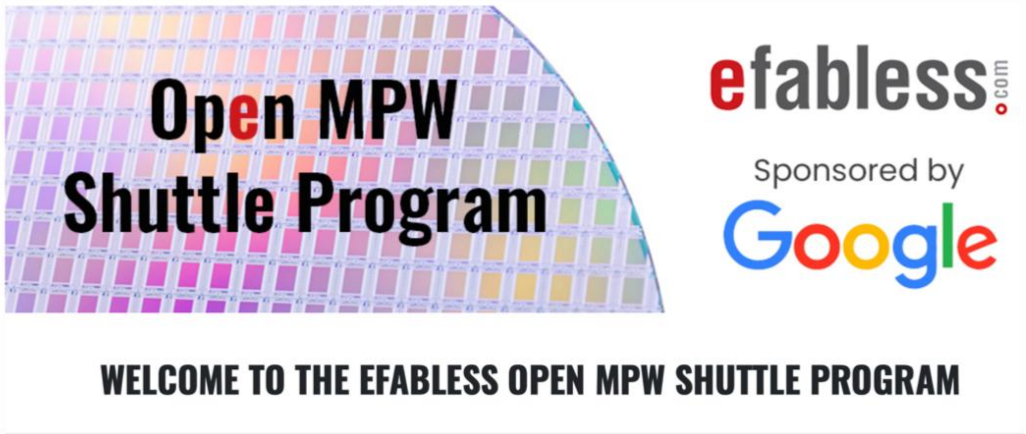


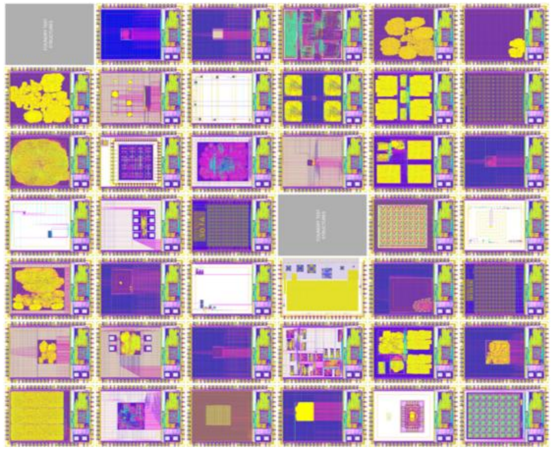
Rise of Open-Source EDA

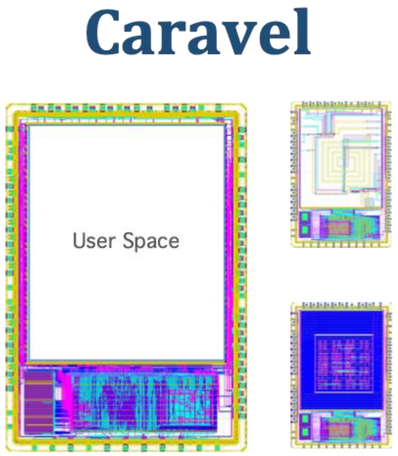
- Open-source EDA tools and public PDKs (e.g. **SKY130,GF180mcu, SG13G2**) have enabled new opportunities.

- Toolchains like **Yosys** and **OpenLane (Librelane)**, with MPW services such as **Tiny Tapeout**, support complete ASIC flows without proprietary software.

- **Democratization of IC design:** accessible to universities, researchers, and independent developers.







MPW = multiple designs on same wafer → shared cost

Essential IC Design Tools (Digital & Analog)

Design Task	Cadence	Synopsys	Open-Source Tools
Digital Simulation	Xcelium	VCS	Icarus Verilog, Verilator
Synthesis	Genus	Design Compiler	Yosys
Place & Route	Innovus	IC Compiler II	OpenROAD
Timing Analysis	Tempus	PrimeTime	OpenSTA
DRC / LVS	Pegasus / Assura	IC Validator	Magic, Netgen
Analog Schematic	Virtuoso	Custom Compiler	Xschem
Analog Simulation	Spectre	HSPICE	Ngspice
Analog Layout	Virtuoso	Custom Compiler	KLayout, Magic

Open Source vs Proprietary

Advantages of the Open-Source Approach

- Accessible from anywhere in the world
- Ideal for universities, research centers, and prototyping
- Enables exploration and modification of tools for specific use cases

Advantages of the Industrial (Proprietary) Approach

- High integration with commercial fabrication flows
- Professional support and quality certification
- Optimized for high-complexity and high-volume designs

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IC Design Methodologies

RTL / Semi-Custom (Top-Down)

•Design described in **Verilog (RTL)**
•Logic synthesized into **standard cells**
•Automated **Place & Route**
•Used for **large digital systems and SoCs**

Transistors → Custom Layout → DRC/LVS/PEX

Full-Custom Design

•**Transistor-level** circuit and layout design
•Not directly described in Verilog
•Verified using **SPICE and layout extraction**
•Used for **analog, mixed-signal, and custom digital blocks**

Verilog (RTL) → Synthesis → P&R → GDS

Tools for Digital Design (OpenLane/Librelane)

ASIC Design Flow

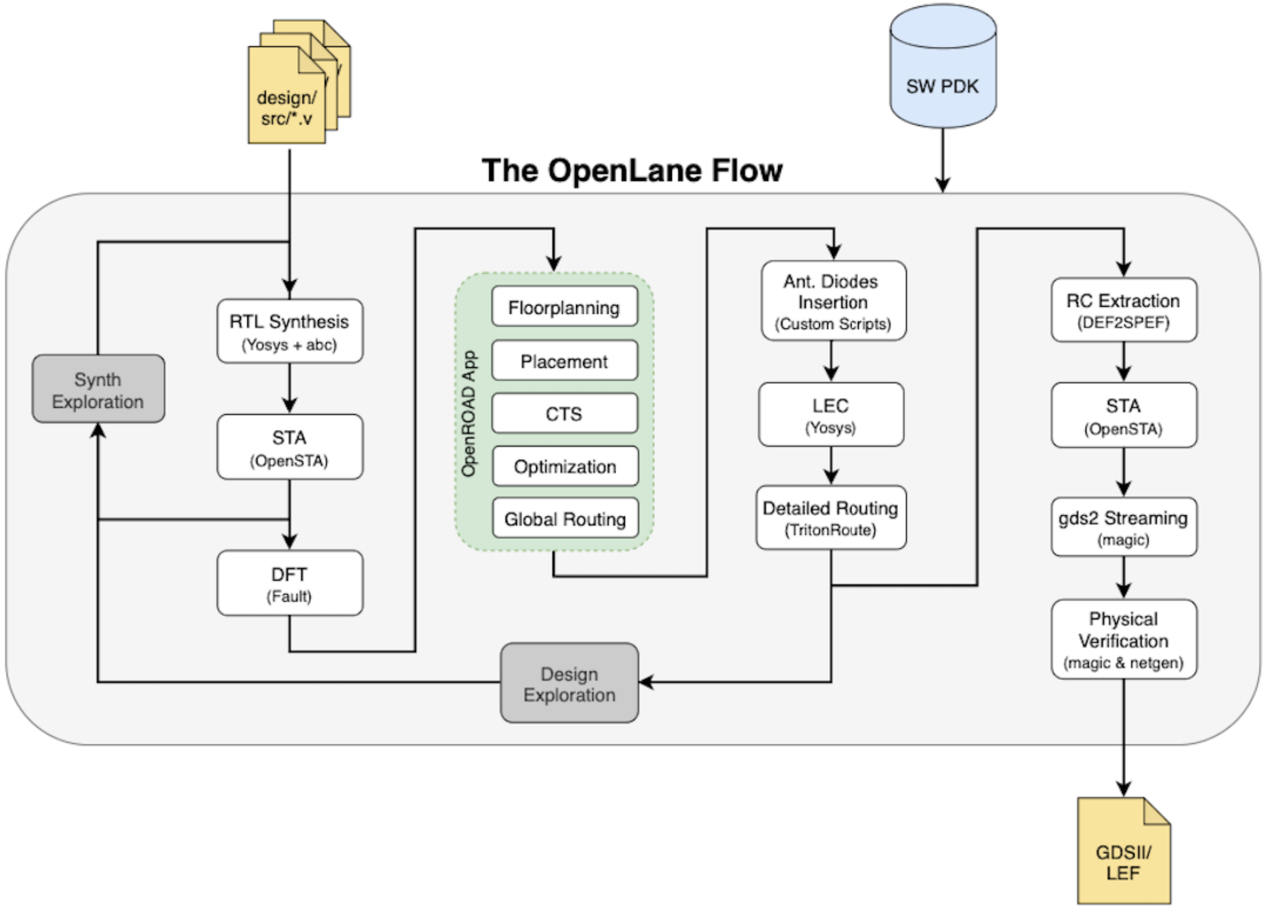
OpenLane provides an automated digital design flow for **ASICs** *(RTL → GDSII)*.

Originally initiated by **Google** and **SkyWater** to enable open-source chip design using the **SKY130 PDK**.

Automation

•Provides scripts and tools to automate:

- Synthesis
- Floorplanning and placement
- Clock-tree synthesis (CTS)
- Routing
- Timing, DRC, and LVS verification



From Concept to Reality (Full-Custom)

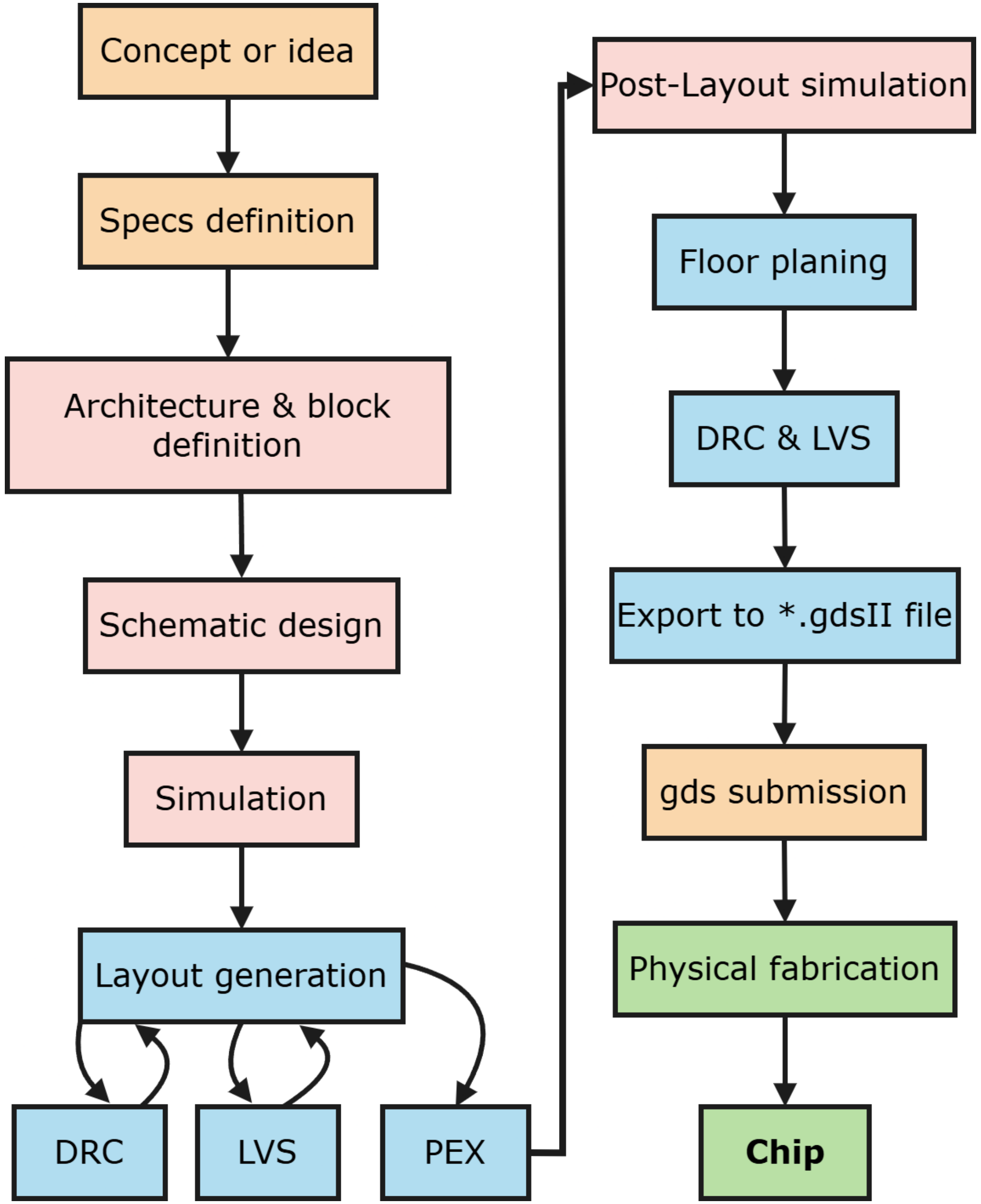
From Idea to Silicon

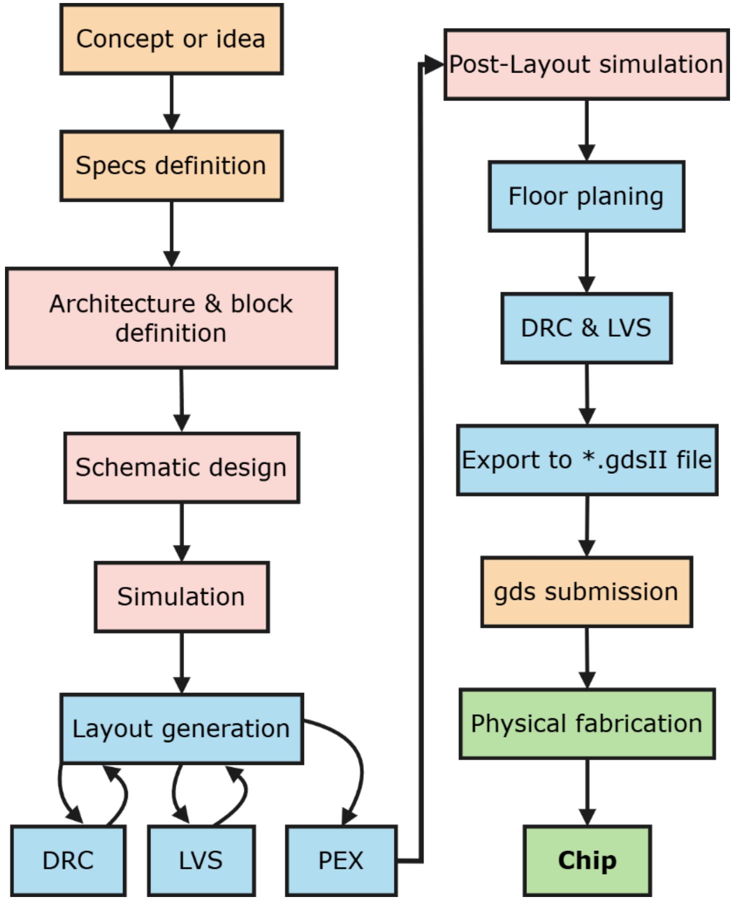
- Transforms a concept into a functional circuit, and then into a real chip.

Complete Process

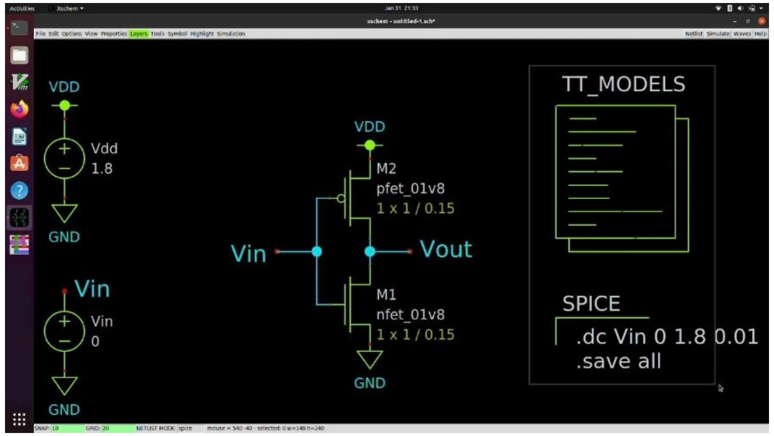
- Design the **schematic** and simulate it.
- Create the **physical layout**.
- **Verify and refine** your design.
- **Send it for fabrication** and receive your chip!

System Engineer / Manager
Analog Designer
Layout Engineer
Foundry (Fab)
Test & Verification Engineer

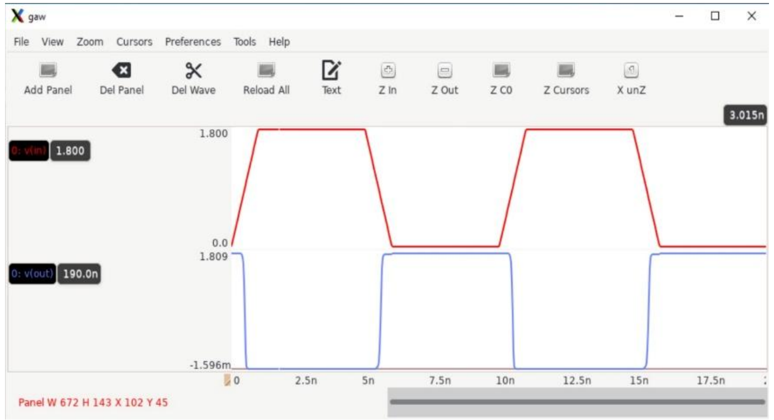




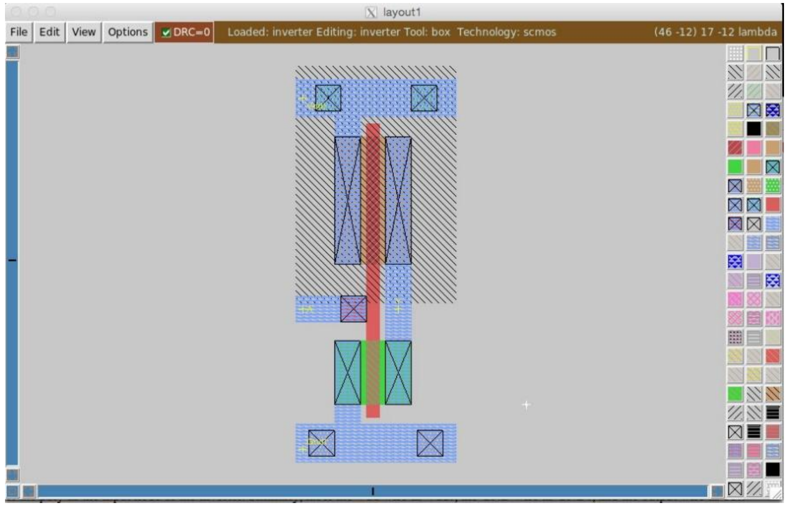
Schematic Design



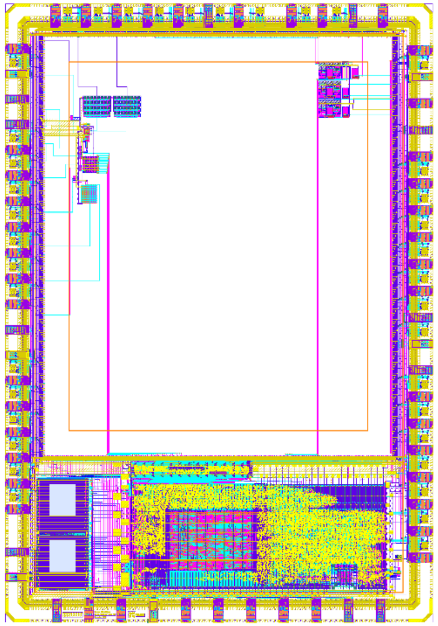
Simulation



Layout Generation (DRC,LVS,PEX)



Floor Planning



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Capstone IC Design at USFQ
(Integrated Circuits Course)

- USFQ defines its IC capstone as an individual full-custom design using the SKY130 open PDK.

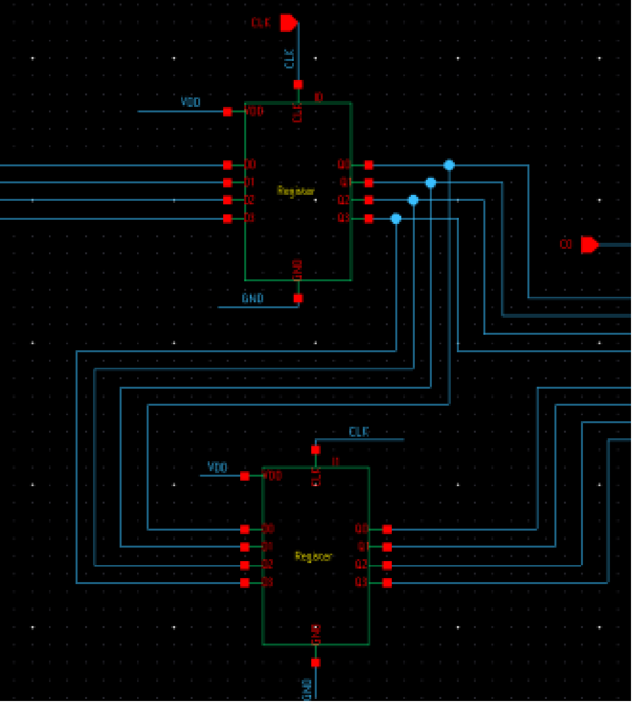
Key Elements

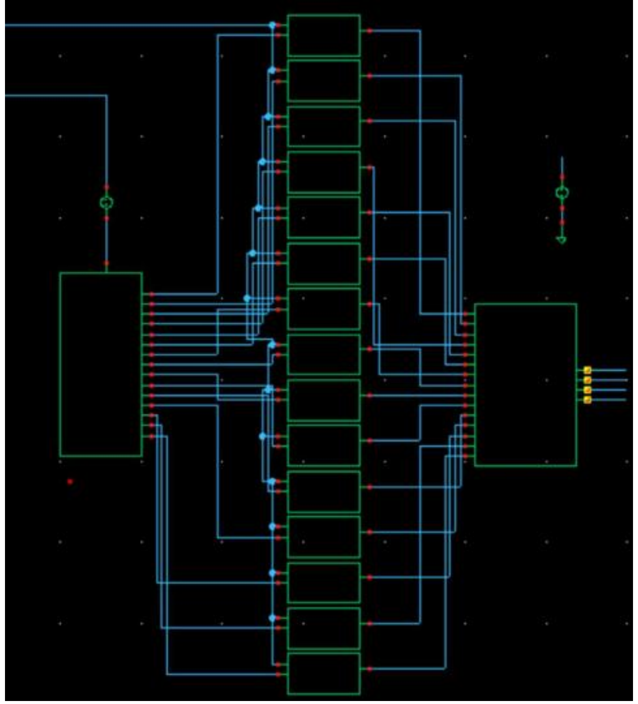
Student-selected **mixed-signal ICs** (biomedical, IoT, low-power systems)

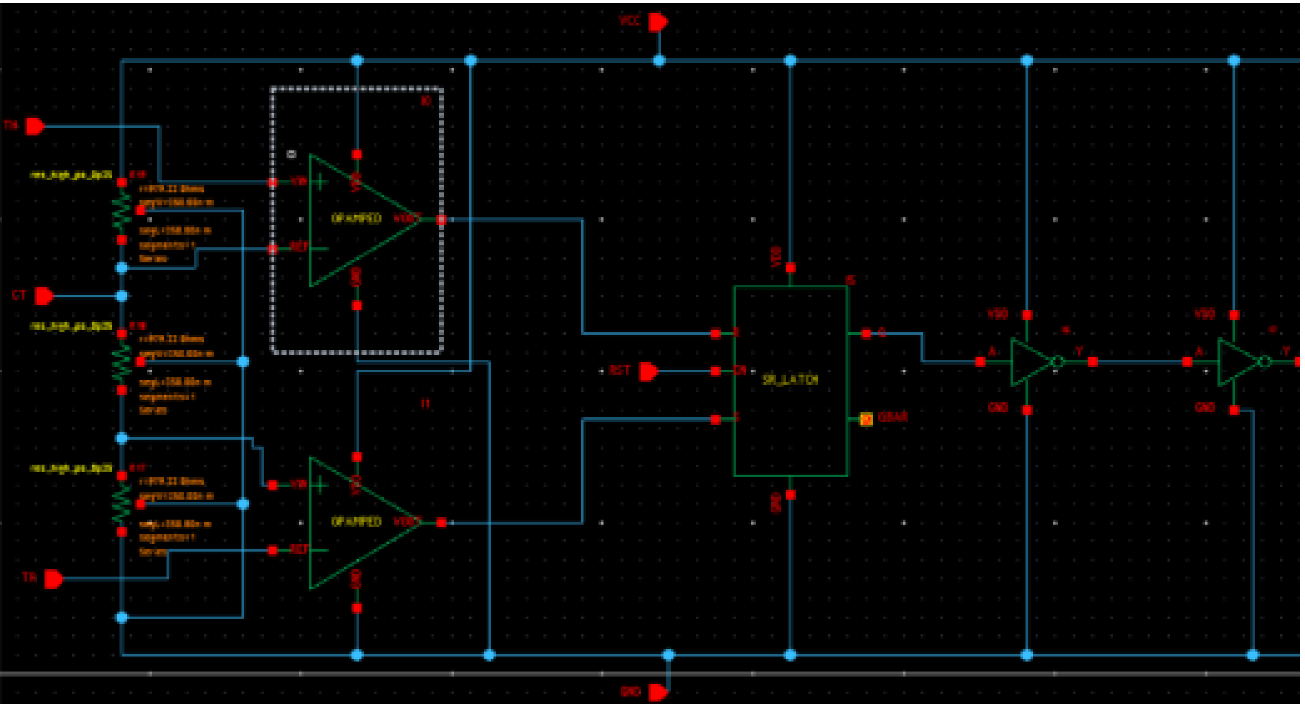
End-to-end industrial flow:

- **Specs → schematic → simulation**
- **Layout → DRC / LVS / PEX → post-layout verification**

Optimization of **power**, **delay**, **and area.**





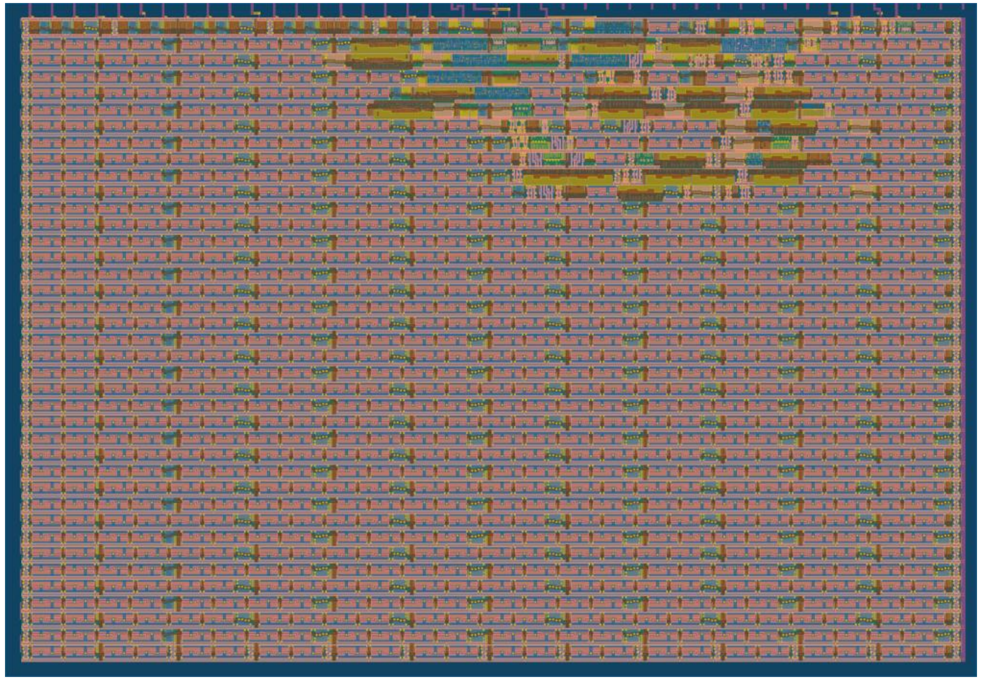


Some Selected Capstone Projects (Ready Designs)

- **Process Variation Sensor** – Ring-oscillator–based monitoring and compensation
- **Glucose Detection IC** – Mixed-signal biomedical system
- **FLASH ADC** – Fully parallel, comparator-based architecture
- **CMOS 555 Timer** – 555 Transistor-level implementation
- **Logic-in-Memory** – CMOS–ReRAM hybrid architecture

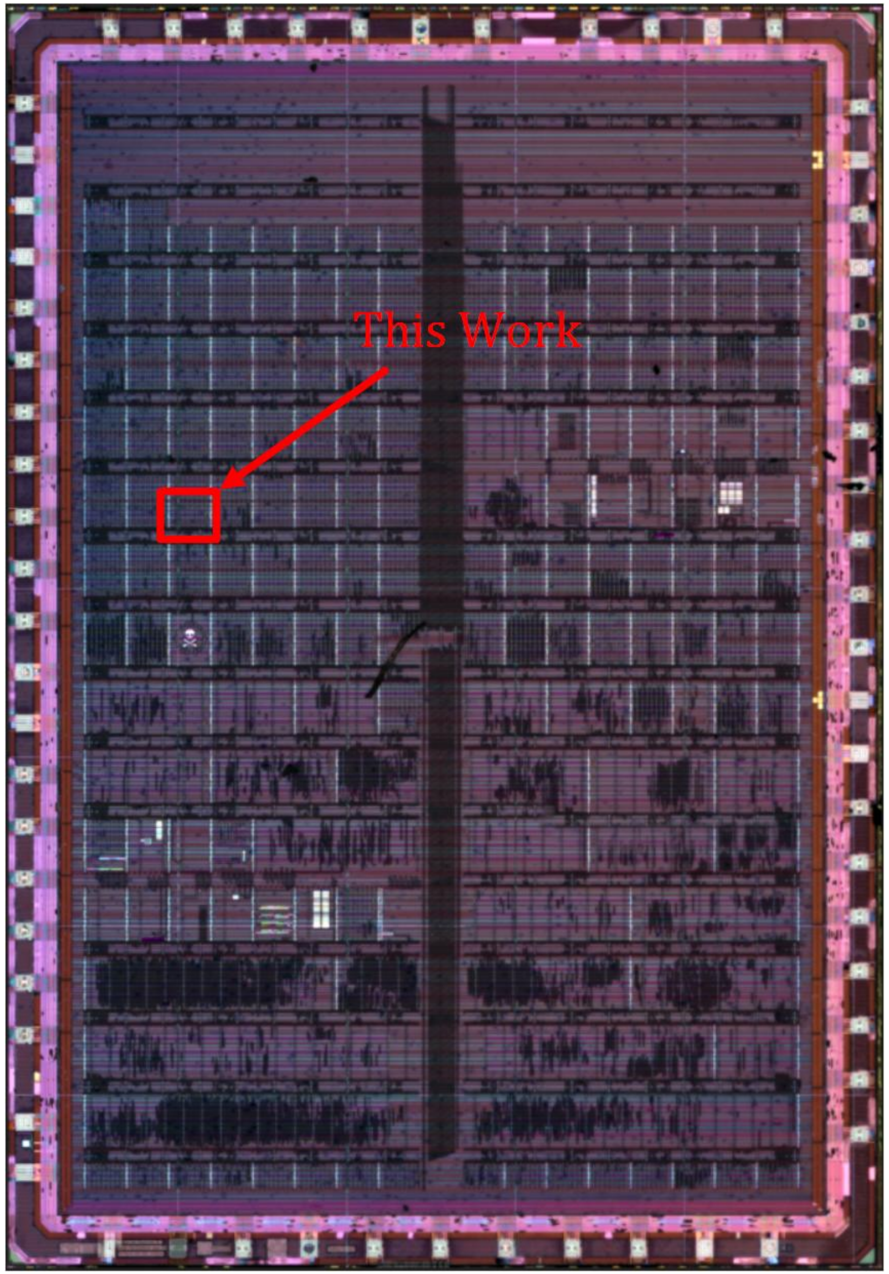
Digital Design: Layout & Integration

- Place-and-route via OpenLane + Magic checks
- Fits into **160 × 100 µm² Tiny Tapeout tile**
- 1.8 V supply



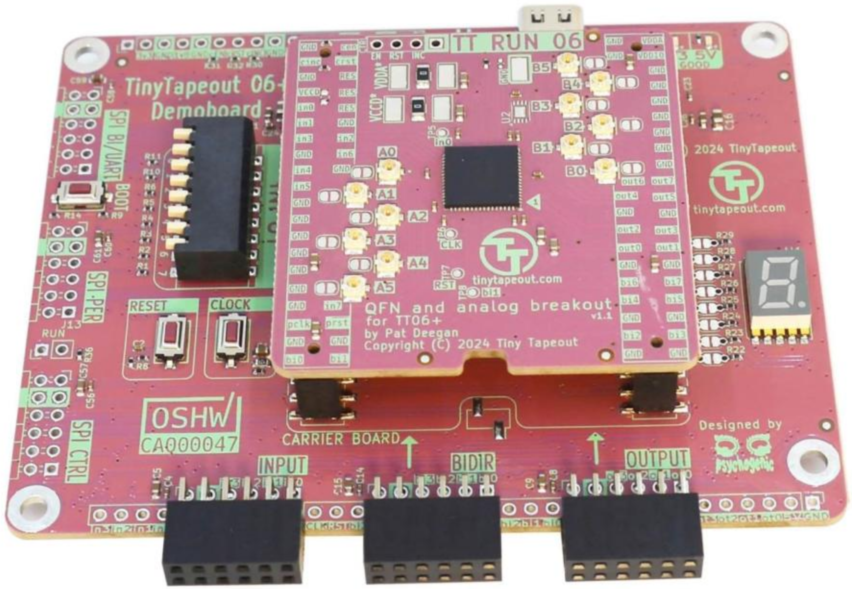
OpenROAD

skywater TECHNOLOGY

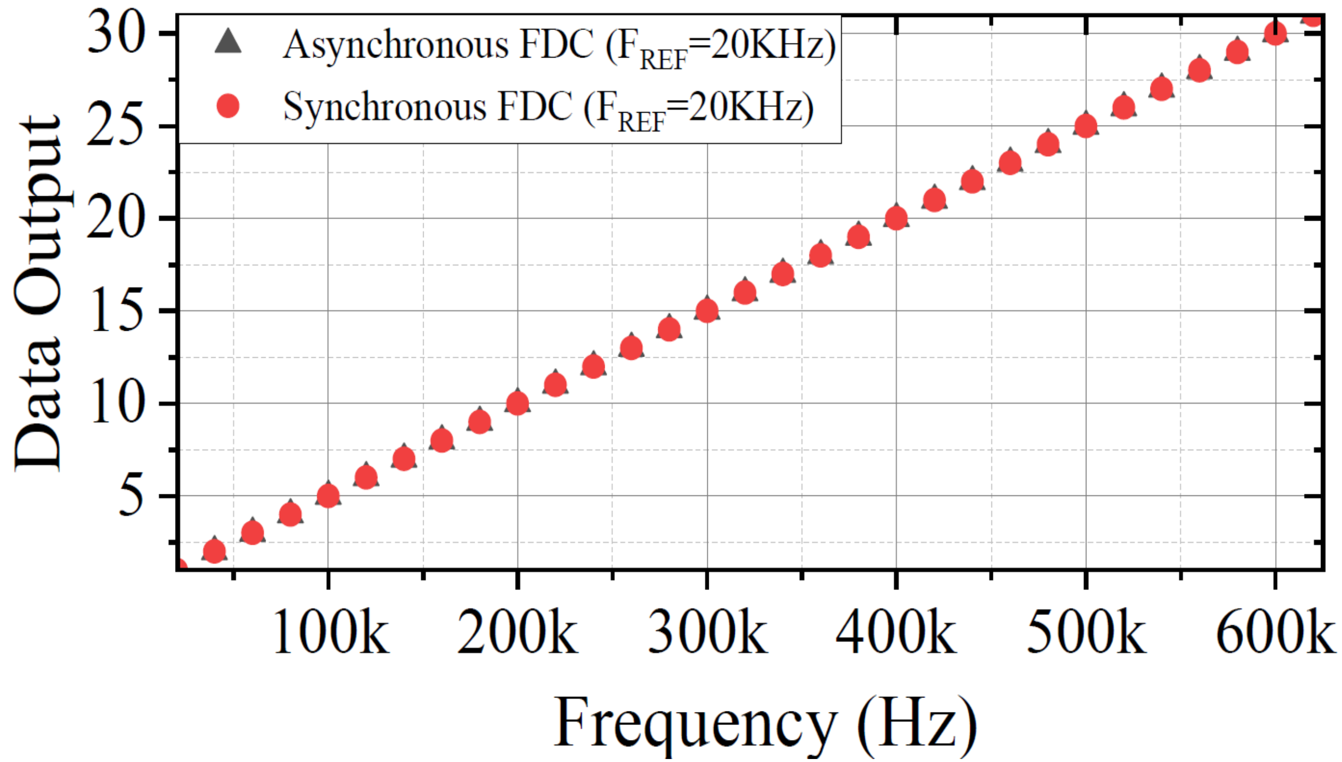


(Example) Fabrication & Testing Platform

- Fabricated in **Tiny Tapeout 6 MPW run**
- Integrated padframe: 4 inputs, 5 outputs
- Breakout board used for measurements
- IOs labeled, standard 3.3 V interface



Measurement Results (TT06)

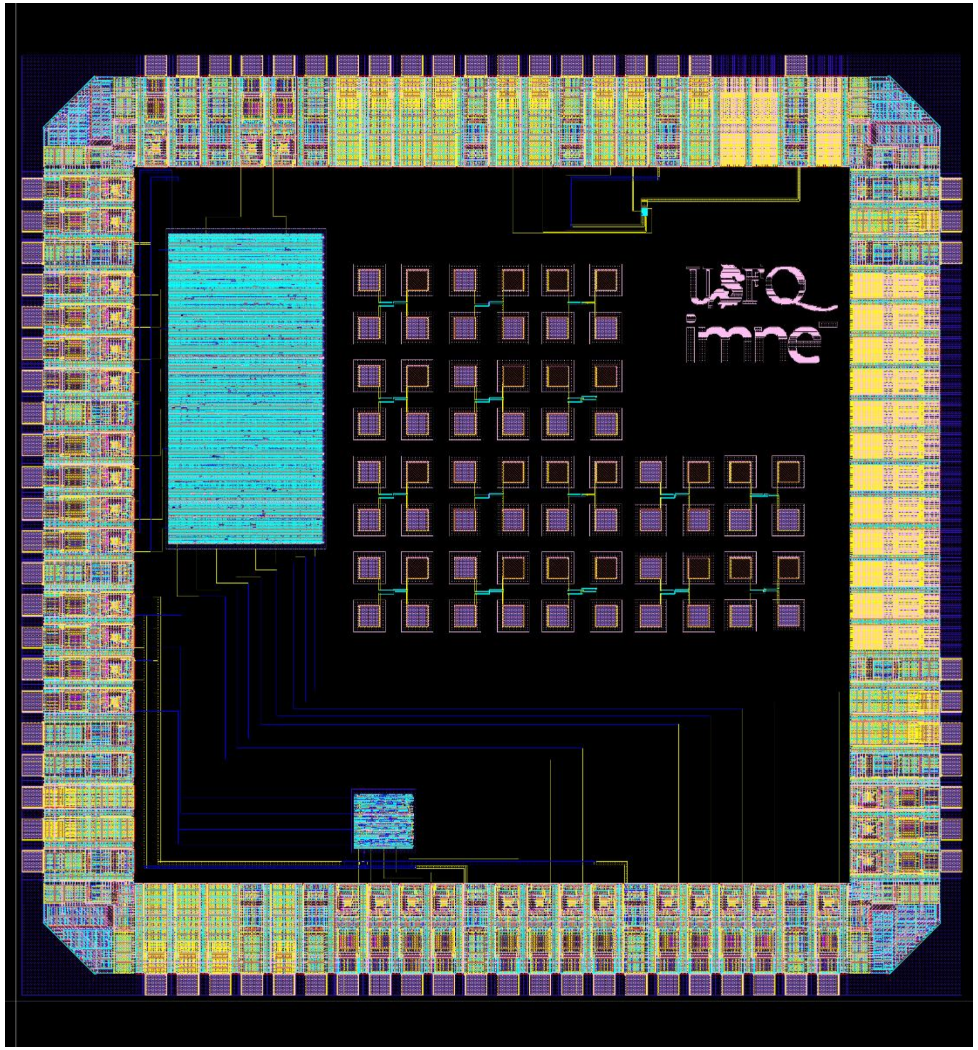


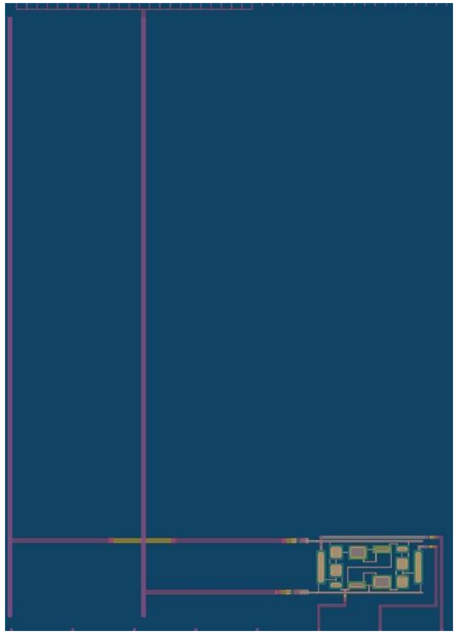
- Measured outputs showed **linear relation** between input frequency and 5-bit digital code.
- Both designs produced **nearly identical results**, validating the architectures.

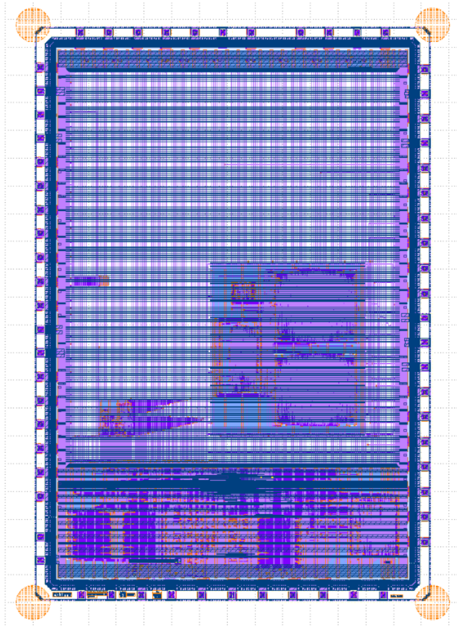
Other Examples:

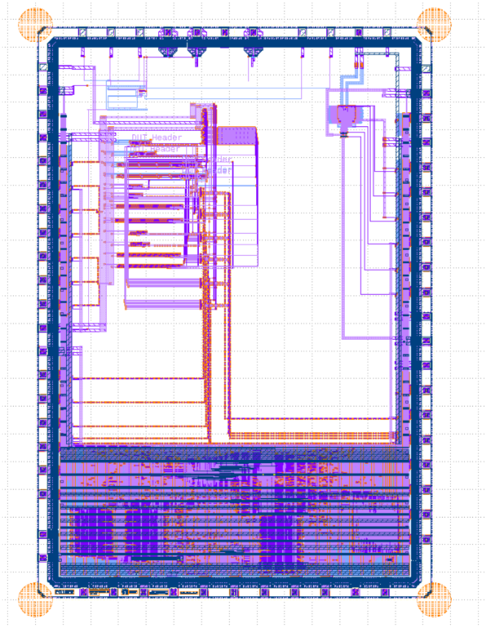
- **Analog Comparator** TT07 Index 231
- **Sky130 Digital Playground** TTsky25a Index 419
- **Dual-Channel PWM with SPI Control + Extra Test Logic:** TTsky25b Index 805

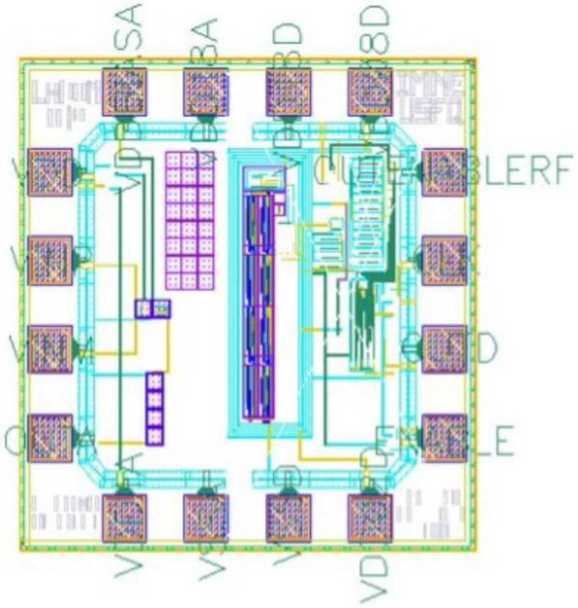
Some Examples:











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- Open-source EDA tools and public PDKs enable **end-to-end IC design education** with real silicon outcomes
- MPW access (e.g., Tiny Tapeout) makes **fabrication affordable and scalable** for universities
- Students gain **industry-relevant skills** from specs to post-layout verification
- The USFQ model demonstrates that **silicon-proven IC education is feasible in Latin America**

Thanks for your attention

Questions?