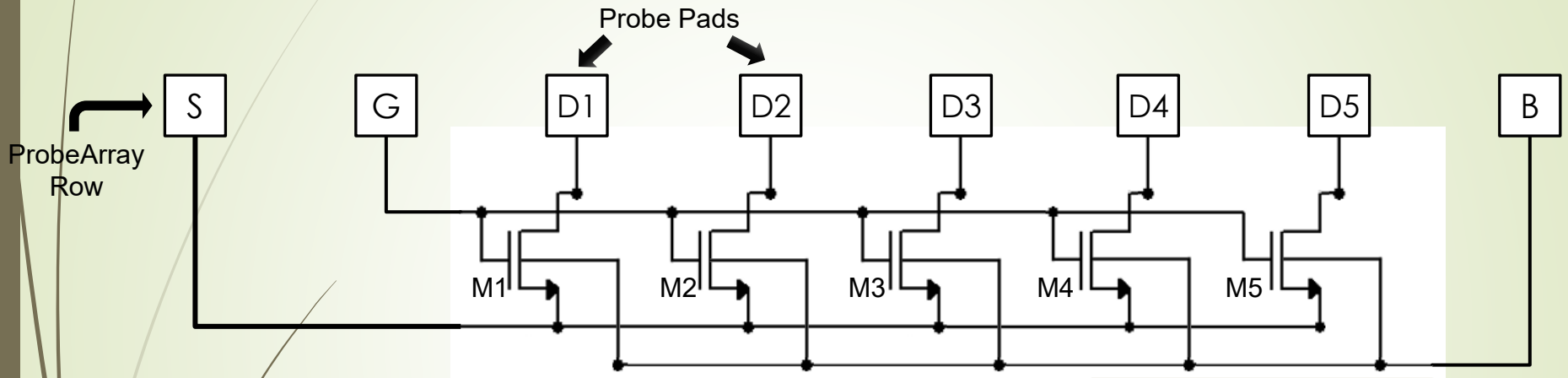
OpenPDK Mismatch Testchip

- Juan Pablo Martinez Brito - CEITEC S.A., Brazil
  In collaboration with:
- Jorge Marin - Associate Professor at Pontificia Universidad Católica de Valparaíso Chile
- Mauricio Montanares - Associate Researcher for Open Source PDK @IHP Germany
- Fernanda Quintana Muñoz - Electronics Engineer (B.Sc.) Valparaíso, Valparaiso Region, Chile
- Krzysztof Herman - Research associate for Open PDK Development @ IHP Germany

Outline

- Review Actual Test Setup with Prober / Test automation.
- Circuit approach for device array testing.
- Test Results.
- Conclusions.

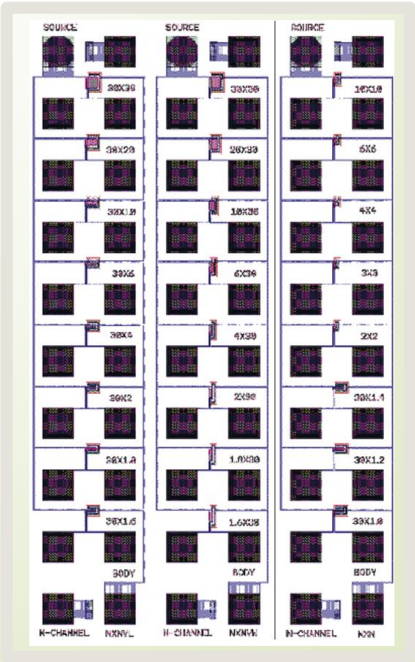
PCM Test Structures



Each device is selected by accessing proper probe pads

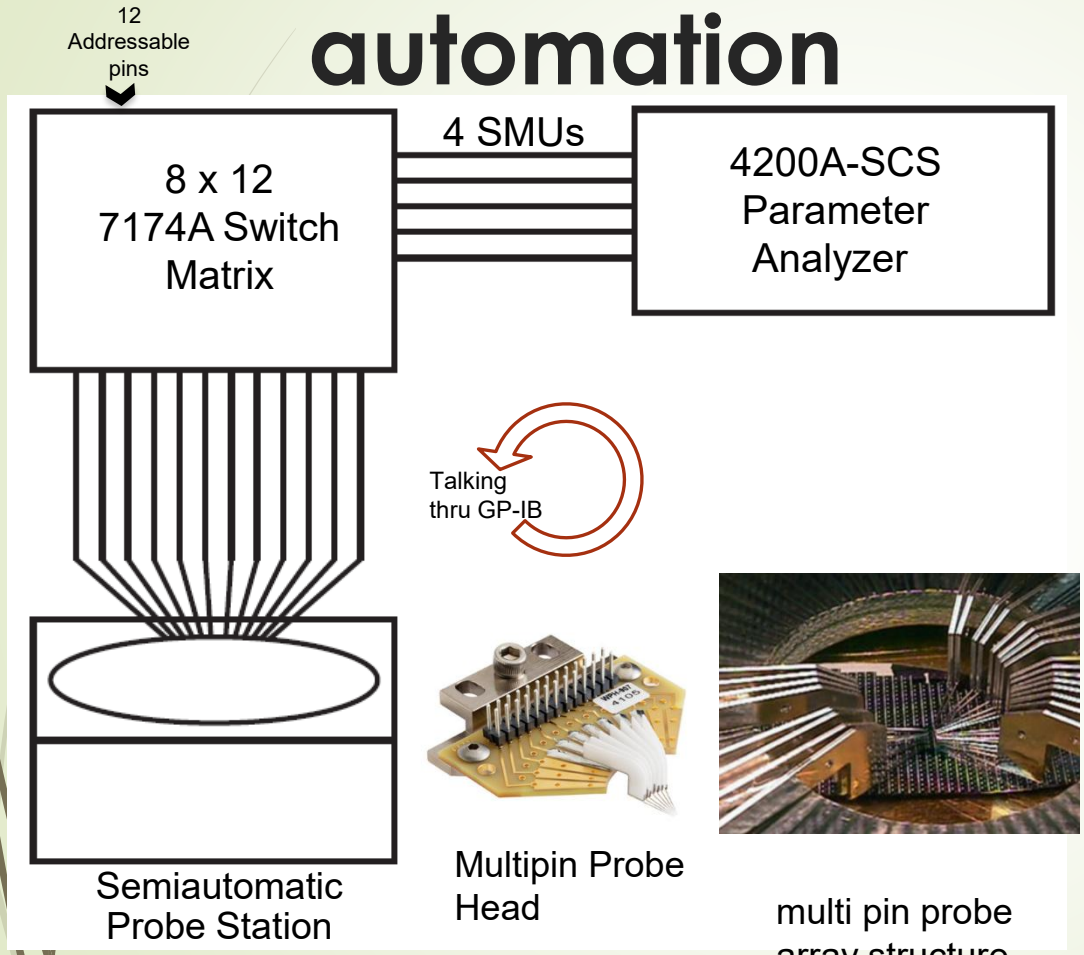
Device address :

1. M1: (S, G, D1, B)
2. M2: (S, G, D2, B)
3. M3: (S, G, D3, B)
4. M4: (S, G, D4, B)
5. M5: (S, G, D5, B)



PCM Test Structure

Test Setup used for automation



- 4200A-SCS commands the Switch Matrix & the Prober using GP-IB bus.
- Each device is selected within each row by proper Switch Matrix addressing.
- The prober walks to multiples rows.
- The prober also walks from die-to-die using pattern recognition.

Circuit approach for device array testing

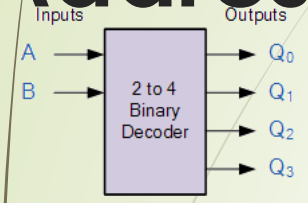
Literature review

- Research field (Keywords):
  - Rapid (Fast) Device Characterization
  - Test Array
  - Device modeling and Characterization
  - MOSFET Mismatch evaluation

- Work mainly inspired on :
  - K. Agarwal et al., "**A test structure for characterizing local device mismatches**," 2006 Symposium on VLSI Circuits, 2006. Digest of Technical Papers., Honolulu, HI, USA, 2006, pp. 67-68, doi: 10.1109/VLSIC.2006.1705315.

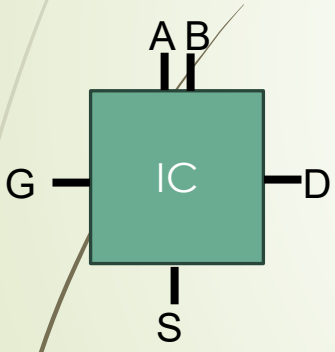
- My results were published here:
  - J. P. M. Brito and S. Bampi, "**Local Variability Evaluation on Effective Channel Length Extracted With Shift-and-Ratio Method**," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4662-4666, Nov. 2020, doi: 10.1109/TED.2020.3017178.

Addressing / switching scheme

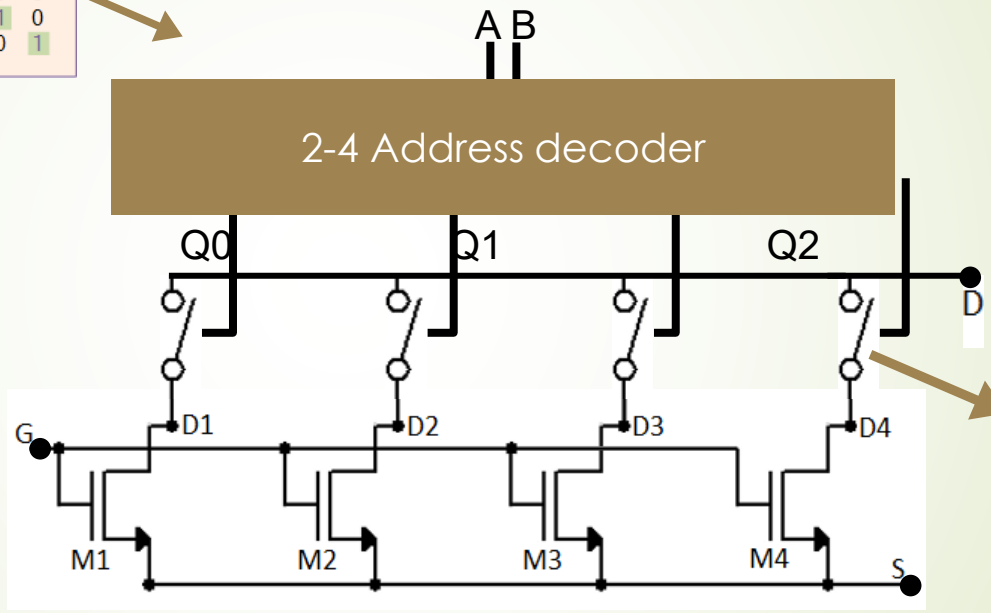


Truth Table

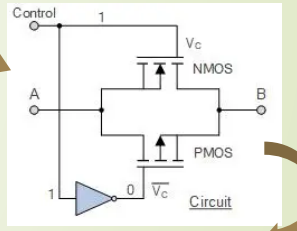
A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



For bonding / packaging; test in a PCB workbench.



Switches implemented as Transmission gates

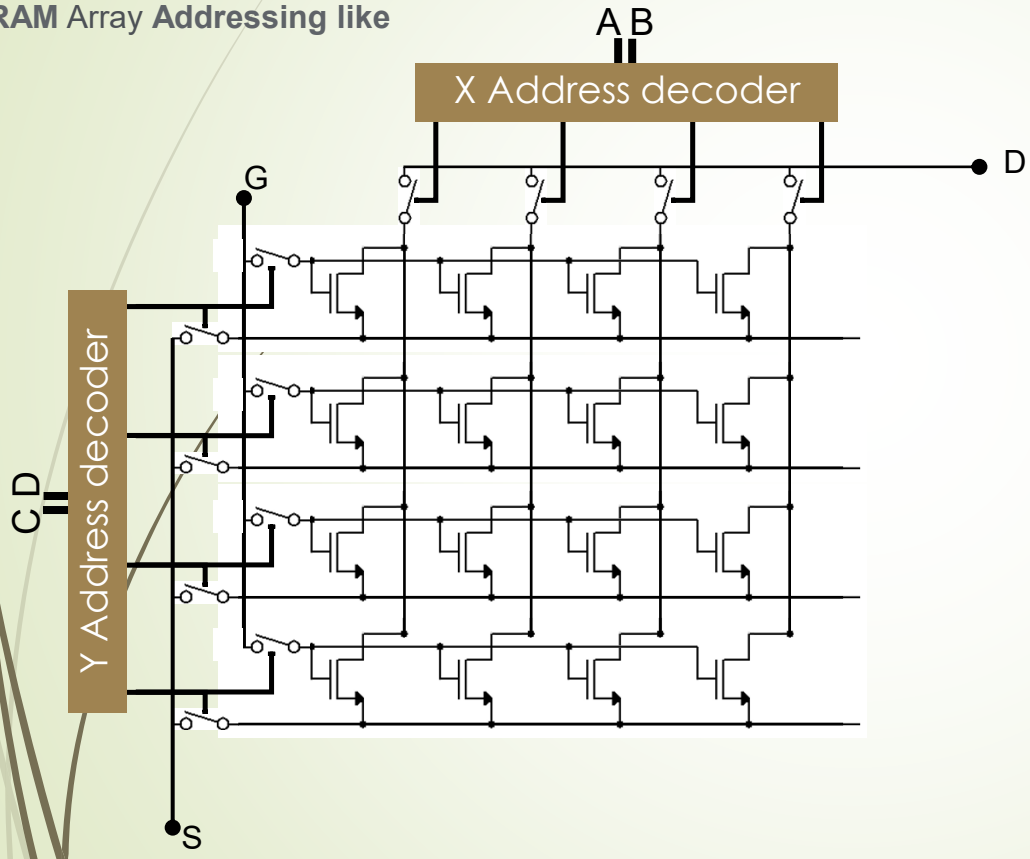


Thick oxide IO devices for low leakage

*bulk terminal erased to simplify the analysis

X-Y device array

SRAM Array **Addressing like**



- **X Address decoder for Drain selection**
- **Y Address decoder for Source and Gate selection**

Problem #1:

- IR Drop due to the on-resistance of the switches, metal routing, cables, etc.

Problem #2:

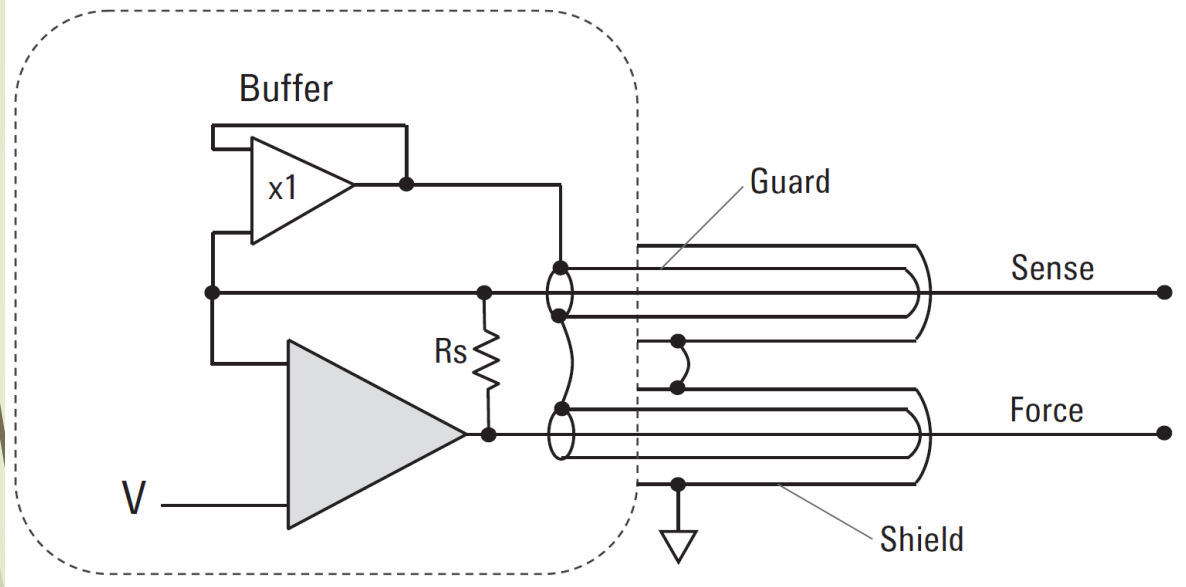
- Gate leakage from the non-selected devices.

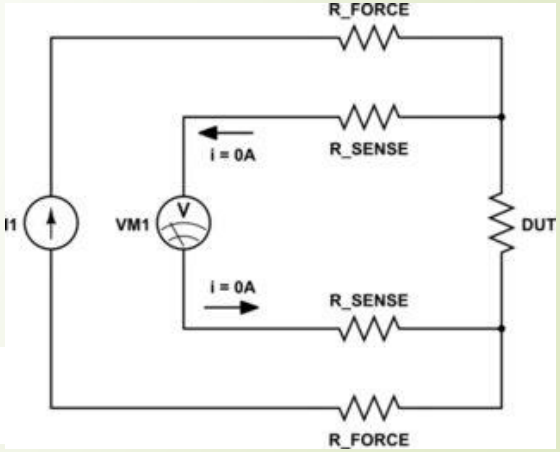
Problem #1

Problem #1:
IR Drop due to the on-resistance of the switches, cables, metal routing, etc.

Solution:
Kelvin 4-Wires bias solution

Force-Sense Kelvin SMU (i)

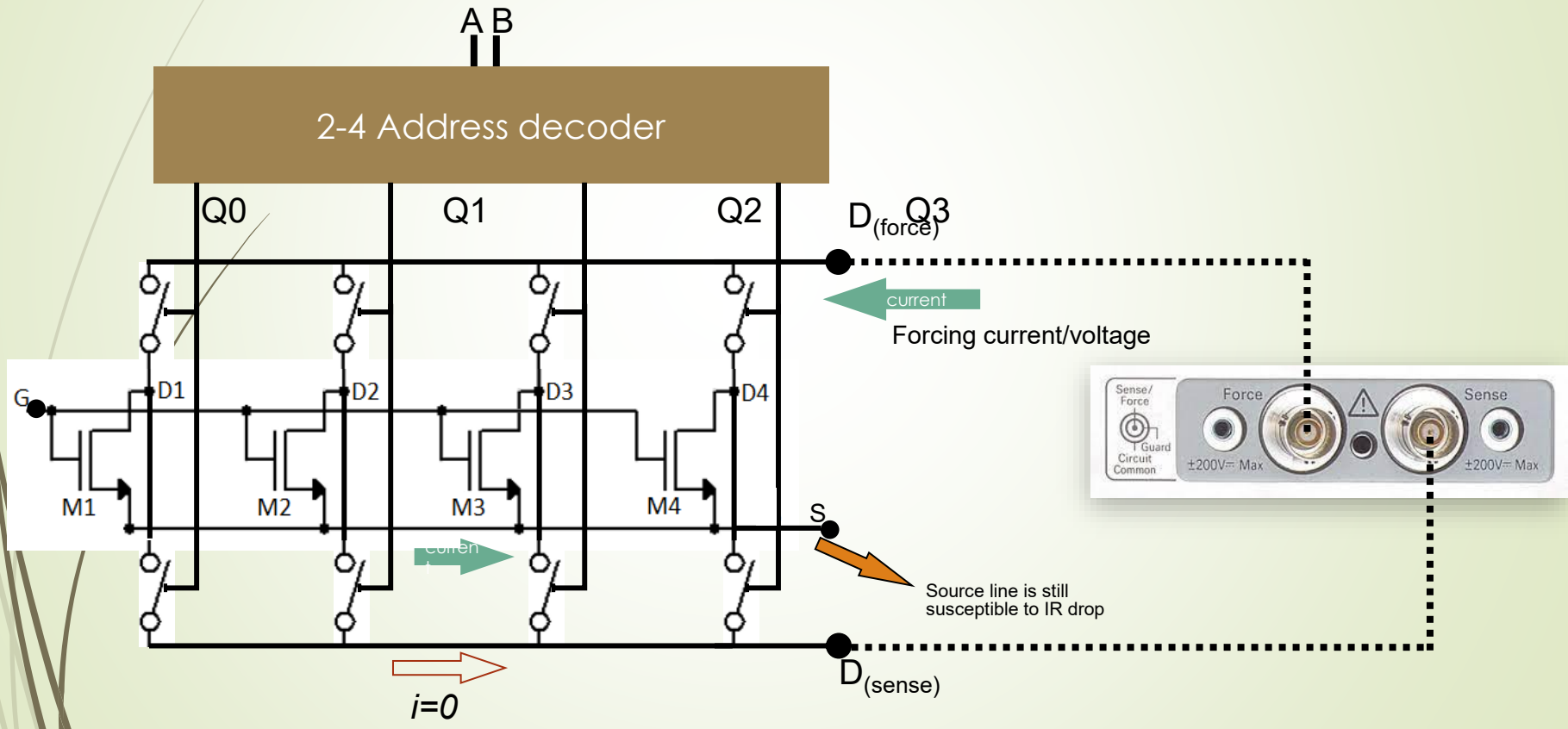




The SMU works to settle the output voltage (force) at a sensing point (sense) in setting voltage through analog feedback.

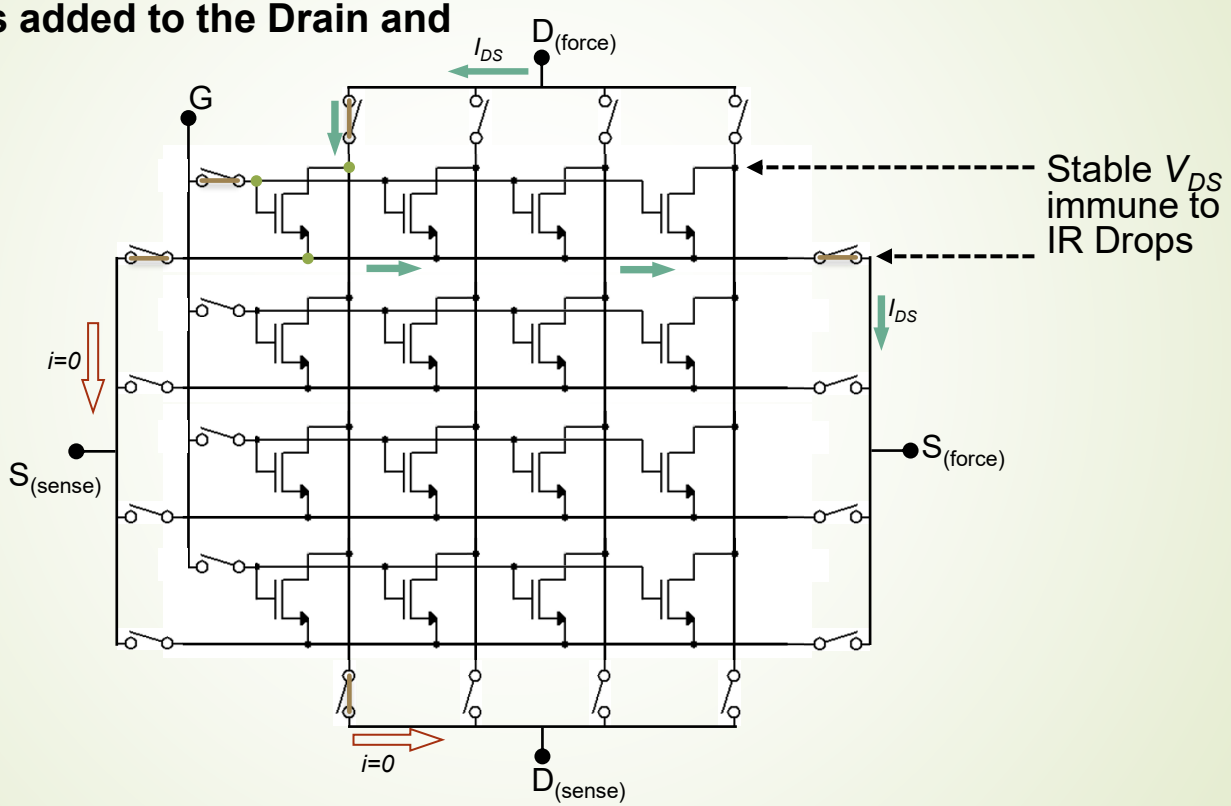
In short: Force terminal will force the voltage (above or below) to make Sense node as specified in the test spec.

Force-Sense at the Drain terminal



X-Y Device Array testing

Force-Sense lines added to the Drain and Source terminals



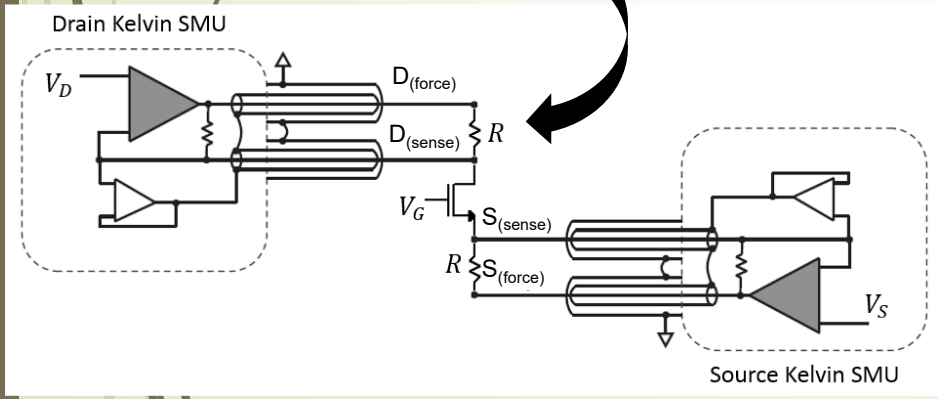
*address decoders erased to avoid visual pollution.

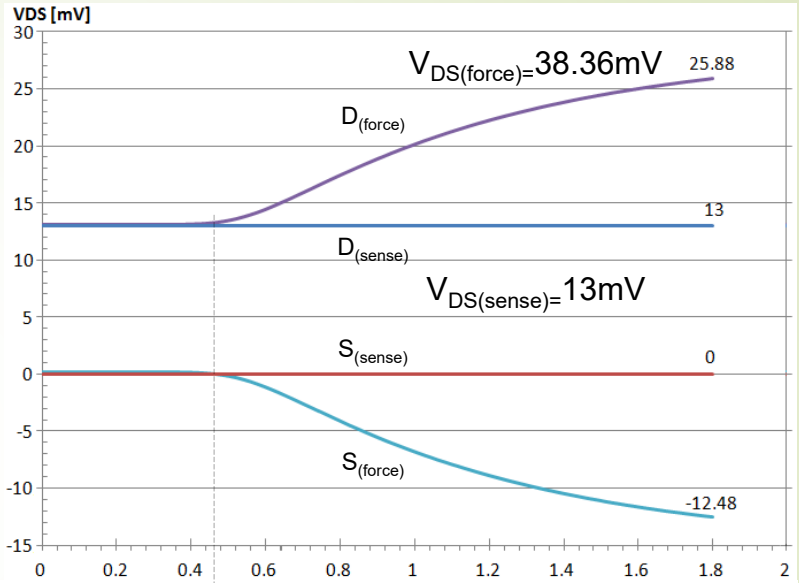
Force-Sense Kelvin SMU (ii)

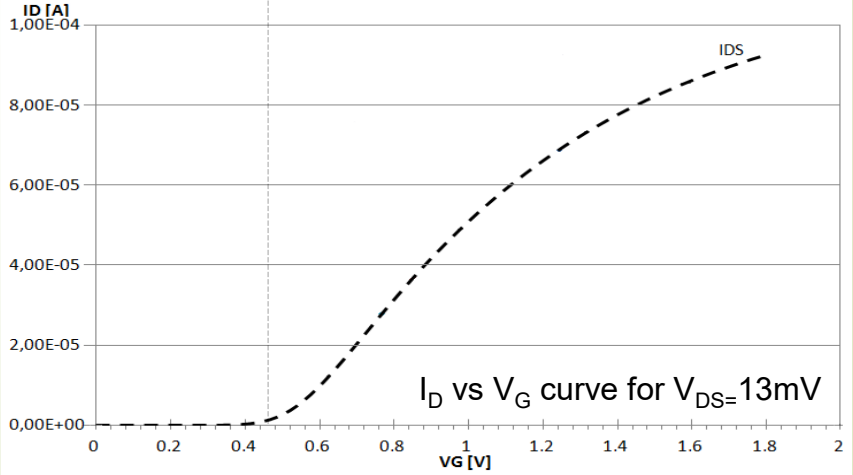
Using SMU Kelvin connection guarantees that the DUT's drain-to-source voltage (V_{DS}) does not change due to any **IR drop**.

The resistance (R) is the equivalent to :

- **Selection switches.**
- **Metal routing inside & outside the chip.**
- **Cable length resistances.**







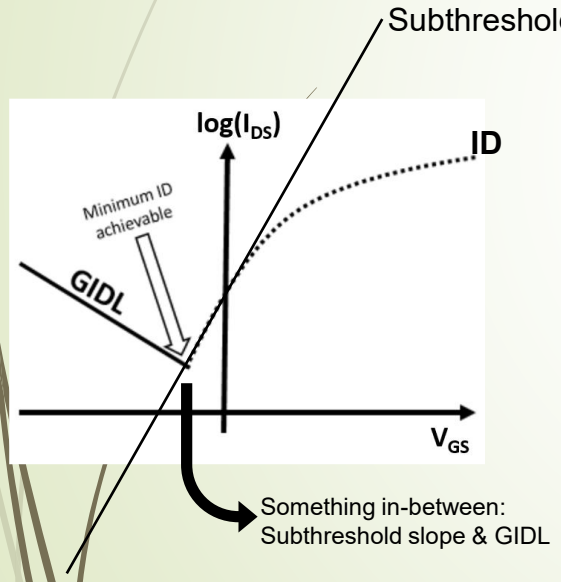
Problem #2

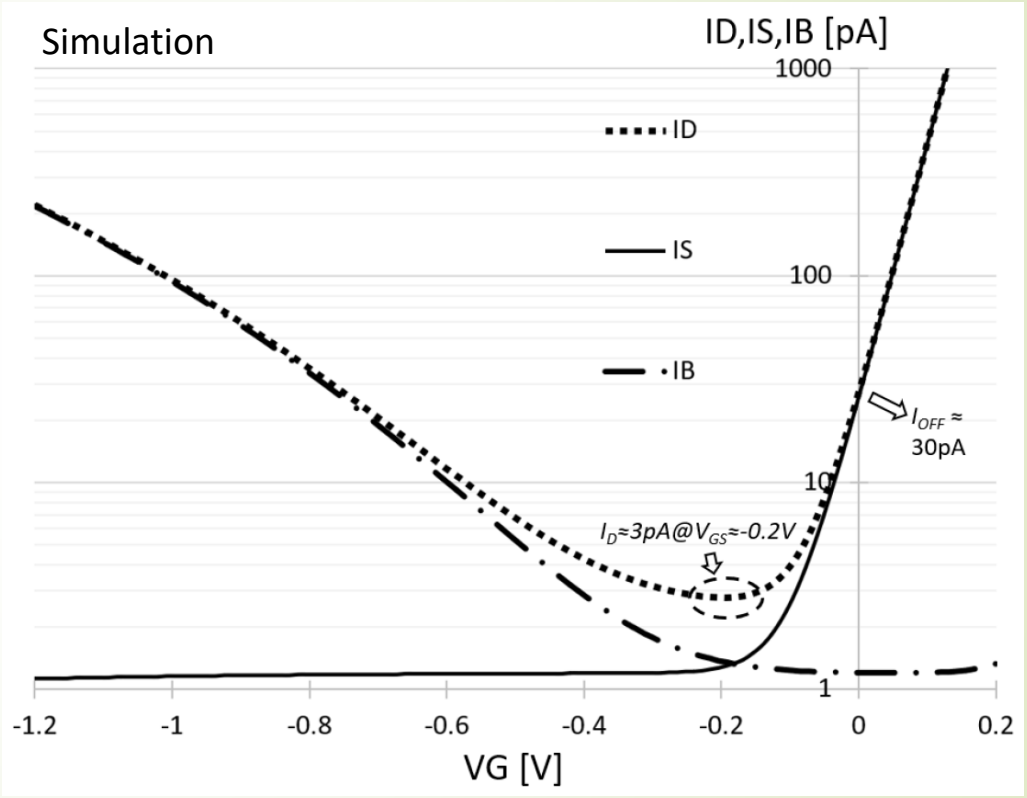
Problem #2:
Gate leakage from the non-selected devices

Solution:
Use a negative voltage to reduce current to the minimum

Unselect gates – NClamp voltage

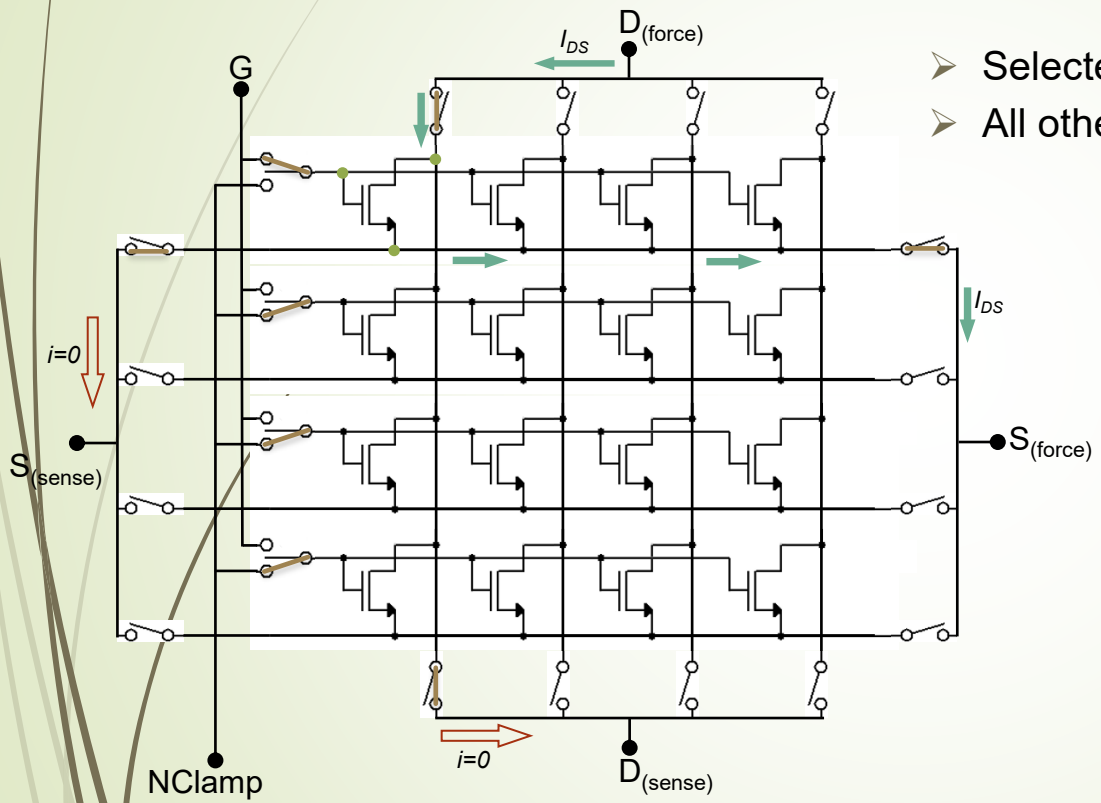
The minimum achievable drain current (ID) for a NMOS transistor is not when V_G=0V, but it is rather for a given value of V_G < 0V.



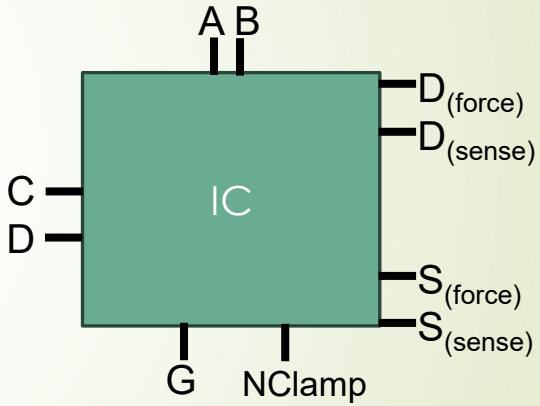


NClamp Voltage ≈ −200mV

Device Array with Force-Sense & NClamp



- Selected gate row connected to **G**.
- All other unselected rows connected to **NClamp**

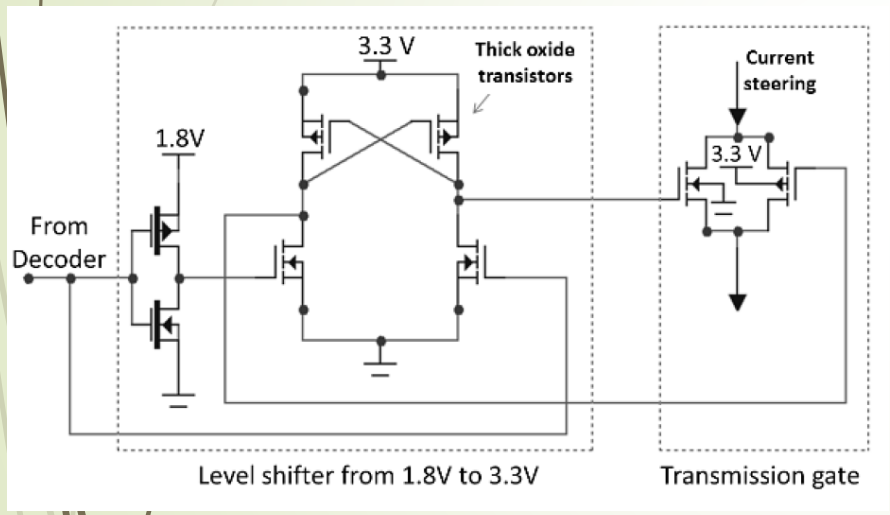


Final circuit for bonding. Test performed in the workbench in a PCB.

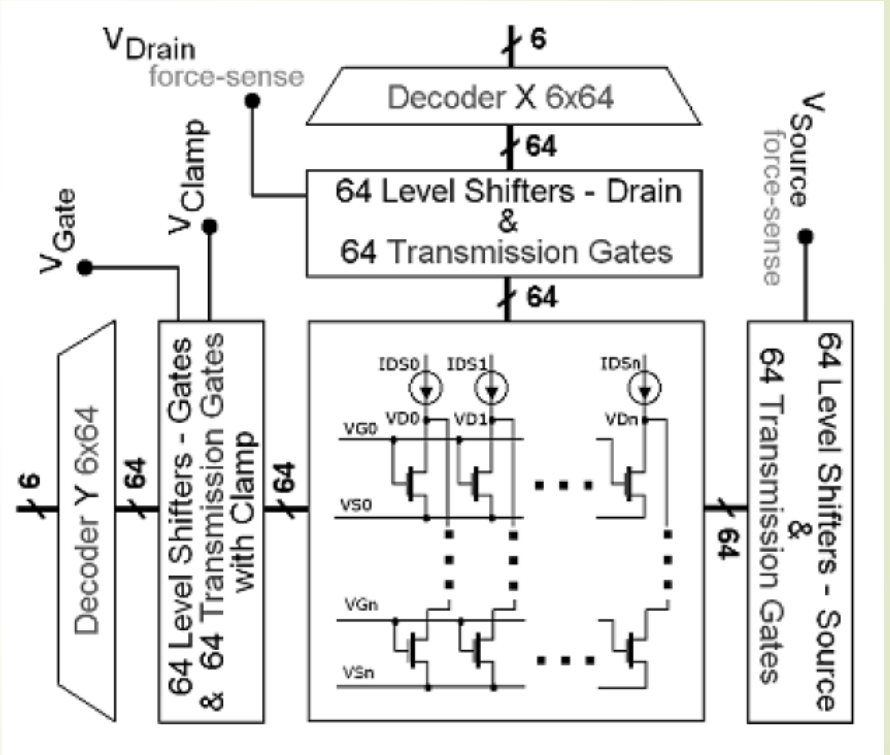
*address decoders erased to avoid visual pollution.

Circuit level block

Circuit per bit



Block Diagram

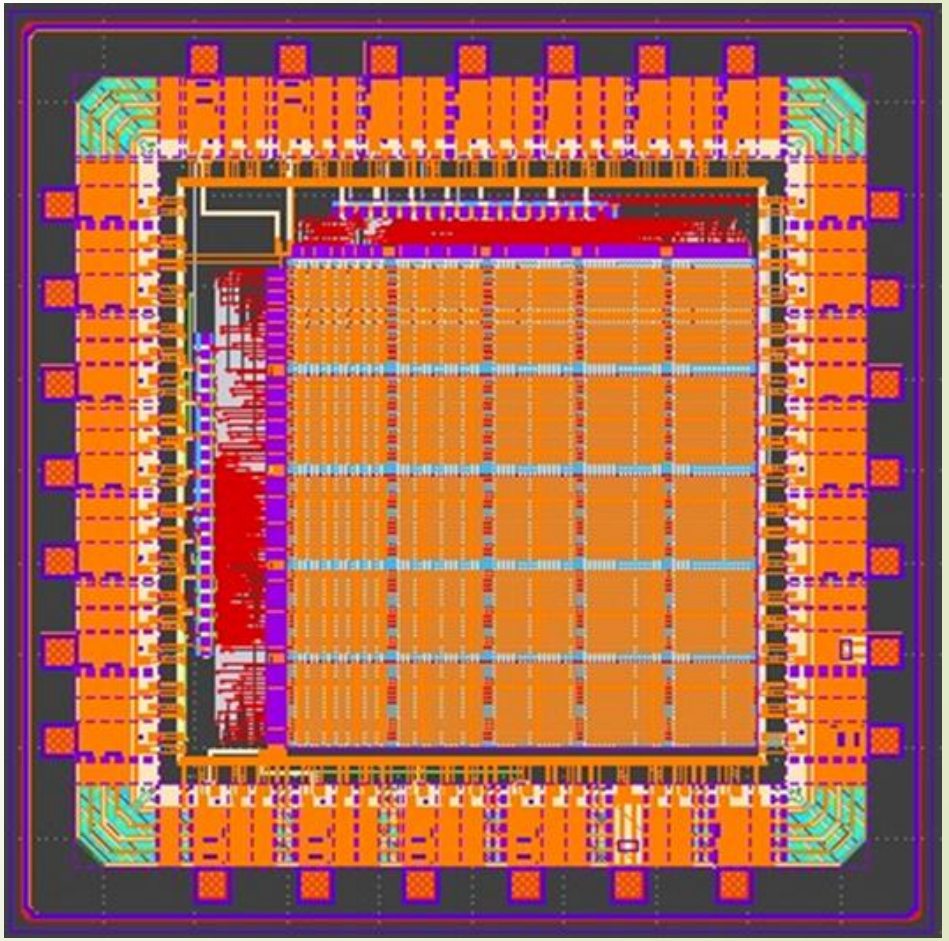


New testchip tape-out

@ Design rules IHP SG13G2

Transistor Sizes

W2.4 L2.08	W2.4 L1.04	W2.4 L0.52	W2.4 L0.26	W2.4 L0.13
W1.2 L2.08	W1.2 L1.04	W1.2 L0.52	W1.2 L0.26	W1.2 L0.13
W0.6 L2.08	W0.6 L1.04	W0.6 L0.52	W0.6 L0.26	W0.6 L0.13
W0.3 L2.08	W0.3 L1.04	W0.3 L0.52	W0.3 L0.26	W0.3 L0.13
W0.15 L2.08	W0.15 L1.04	W0.15 L0.52	W0.15 L0.26	W0.15 L0.13



MOSFET Matching Test Structure

- Complete 5×5 Matrix (25 subarrays)
  - • Each subarray contains 16×16 = 256 identical transistors
  - • Total devices per matrix: 25 × 256 = 6,400 devices
  - • W varies horizontally, L varies vertically
  - • Enables systematic mismatch analysis versus W, L, and W/L

Scripts for automatic matrix generation are here :

https://github.com/IHP-GmbH/TO_Sep2025/tree/main/MissMatch/doc

Conclusions

- Addressable test structure that allows to measure devices using ; a parameter analyzer, power supplies, all connected to a PCB (NO PROBE STATION IS REQUIRED)
- Structure designed to evaluate MOSFET mismatches. But it can be used for any other purpose: Bandgaps, LDMOS, Resistors, etc….
- IHP Tape-out in the oven…

Thank you