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European Nanoelectronics Access

ASCENT+

Access to European Infrastructure for Nanoelectronics

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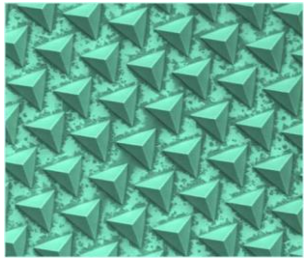
Making things is challenging!

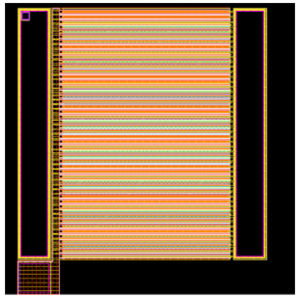
Advanced Equipment

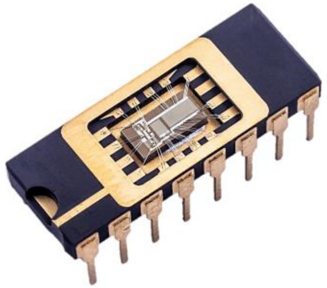
Platform Technologies



Cryogenic Photon Emitter

GaN HEMT





Half Bridge Switch with Driver

Expertise

Complete Offer Catalogue at our Showroom
https://www.ascent.network/access/

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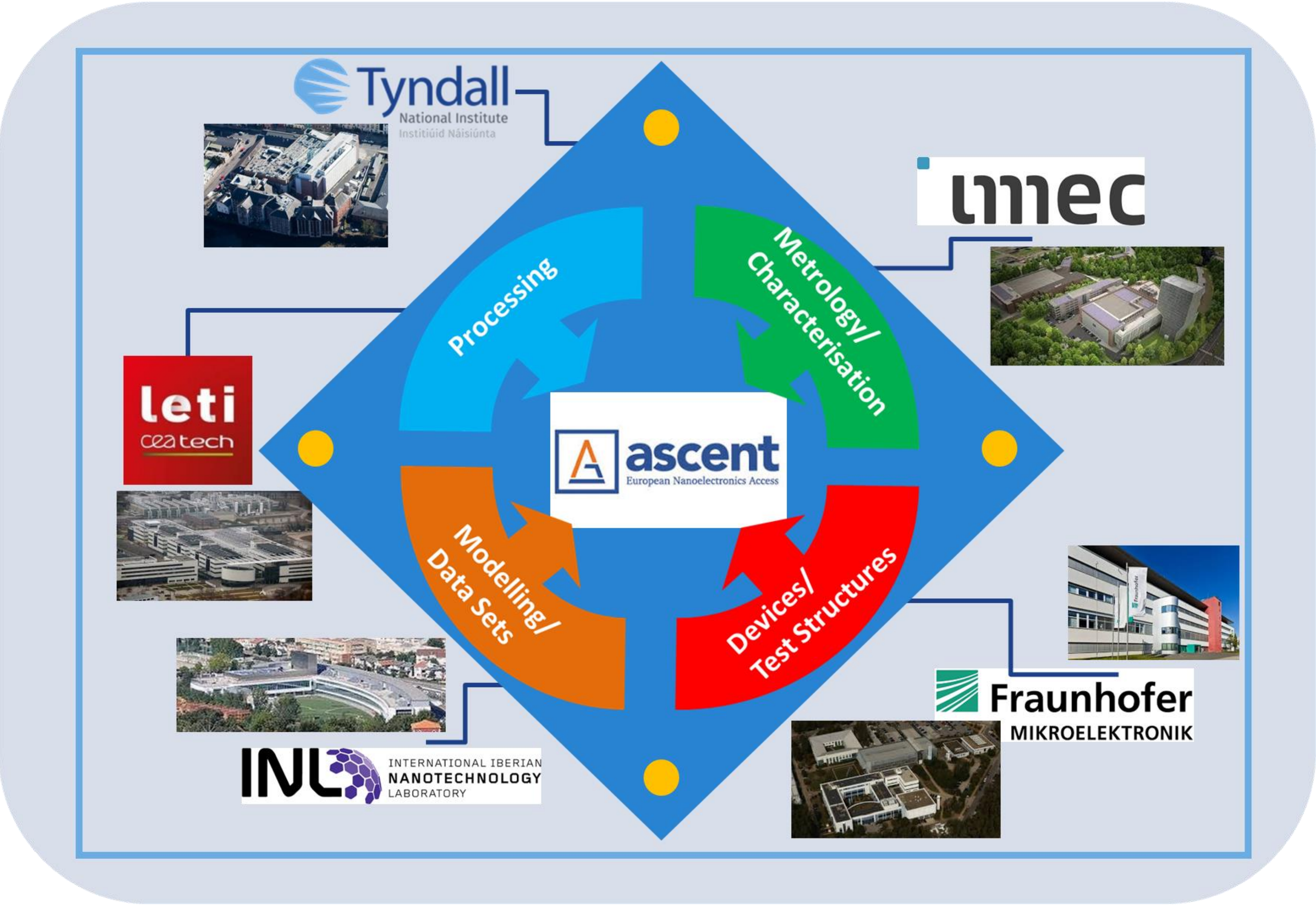
Vision

To integrate major European Infrastructures that enables users from across the world to address emerging research challenges and accelerate innovation path-finding in Nanoelectronics

Mission

ASCENT+ serves as the direct entry point to a European Nanoelectronics Research Infrastructure of global scale offering access to key enabling capabilities in state-of-the-art processing, modelling and simulation data sets, metrology and characterisation, and devices and test structures



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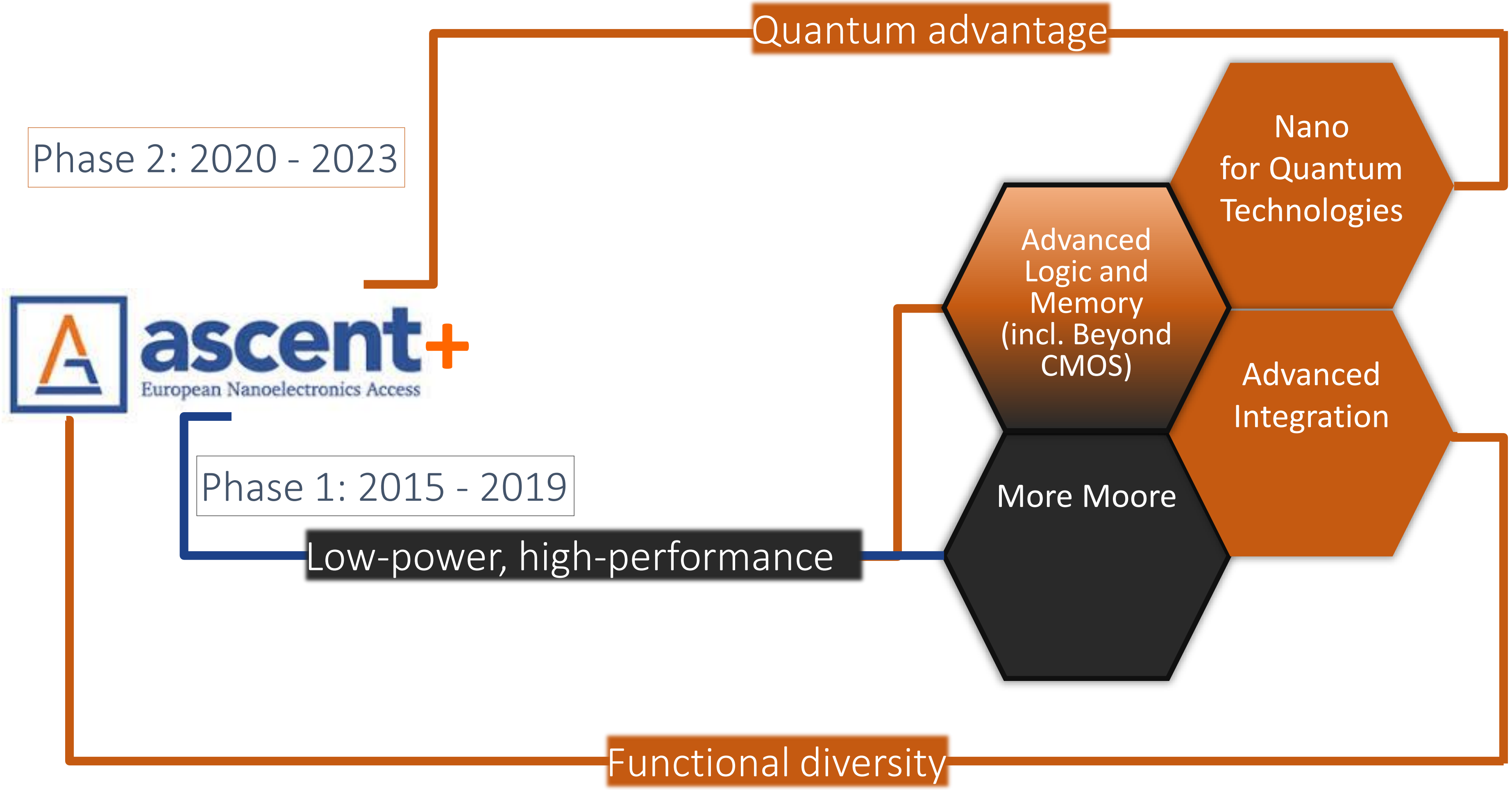
What is on offer?



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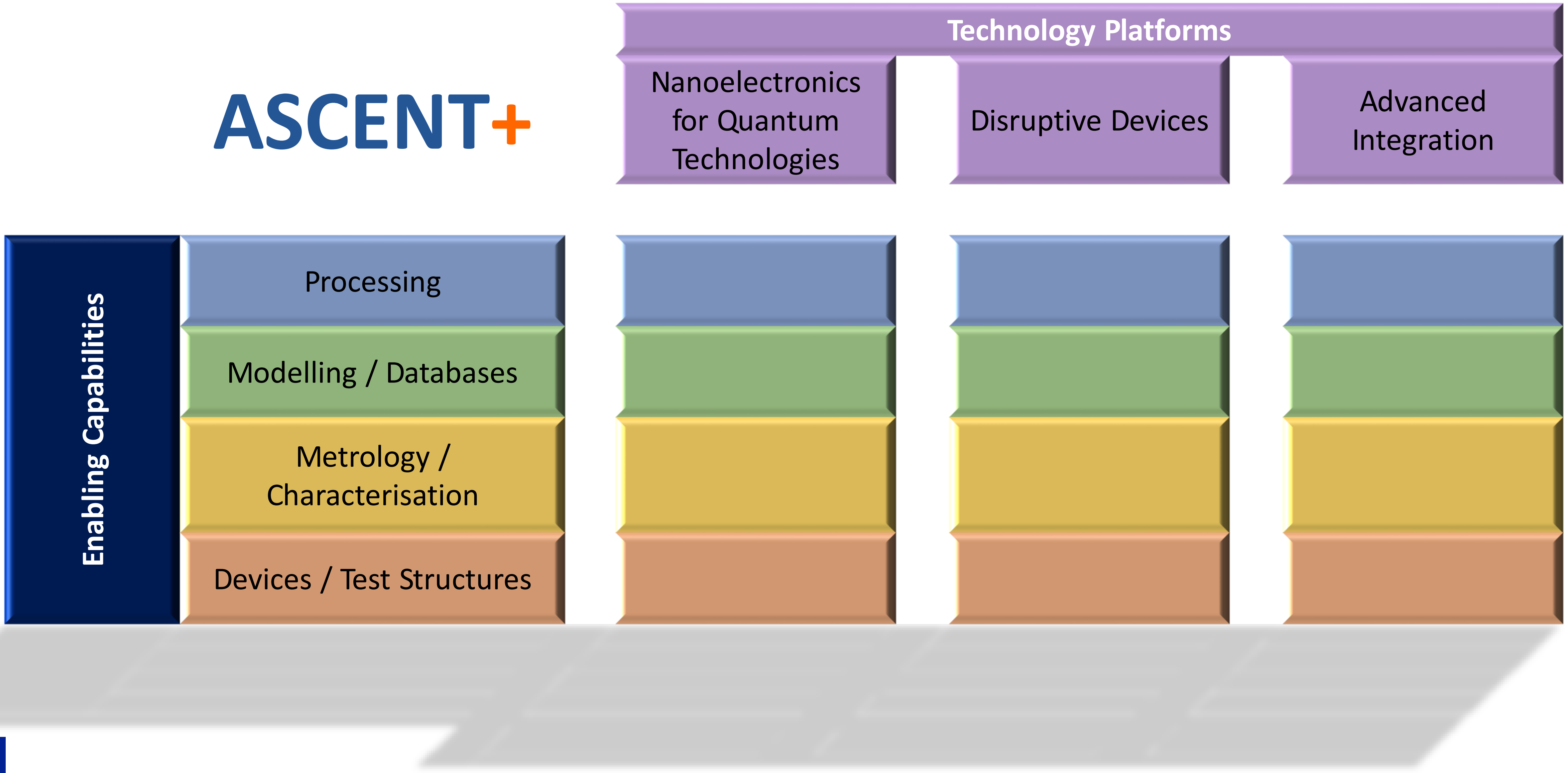
Enabling Capabilities vs. Technology Platforms



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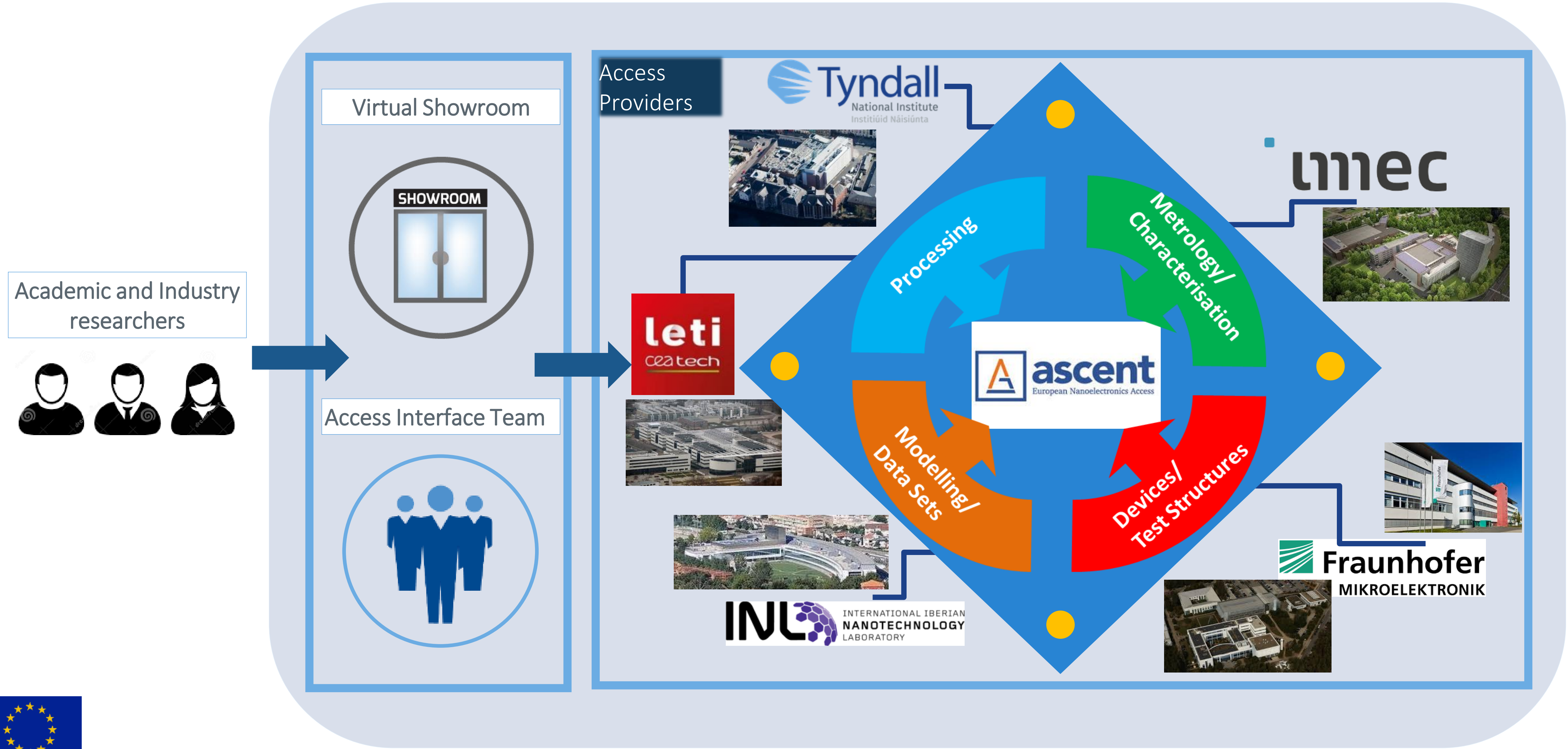
Making access easy!



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ASCENT+ Showroom

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Ascent+ Showroom

KEY ENABLING CAPABILITY

- Devices / Test structures (7)
- Metrology / Characterisation (32)
- Modelling / Databases (2)
- Processing (24)

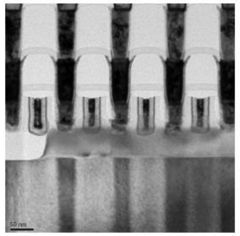
BY PLATFORM TECHNOLOGY

- Advanced Integration (31)
- Disruptive Devices (44)
- Nano for Quantum Technologies (44)

Showroom

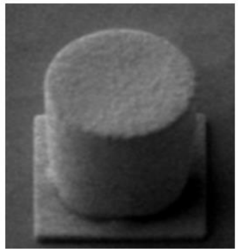
Ascent+ Offerings Showroom

Showing 1–25 of 60 results



14nm FinFET

READ MORE



3D Advanced Packaging

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4H-SiC Line

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AFM

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ALD

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Atom Probe Tomography (APT)

READ MORE

Atomic Force Microscope

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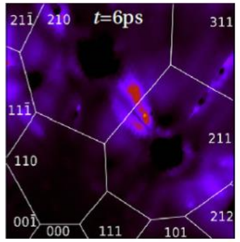

Atomistic Modelling

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Auger Nanoprobe

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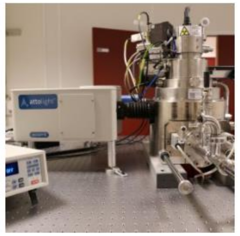

Cathodo-luminescence

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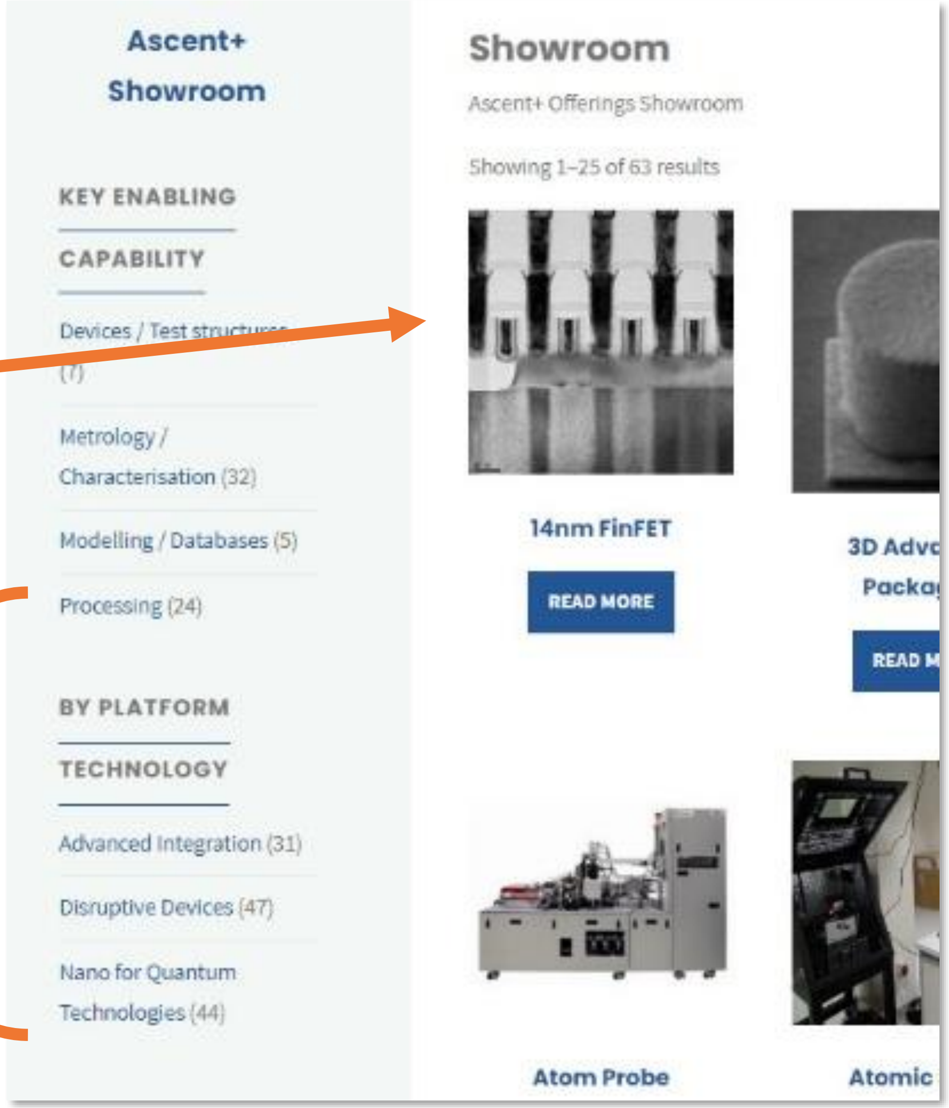
The Showroom

- Individual offerings available
  - Description
  - Technical Specifications
  - Facility
- “e-commerce” platform
  - Browse
  - Filter
  - Search



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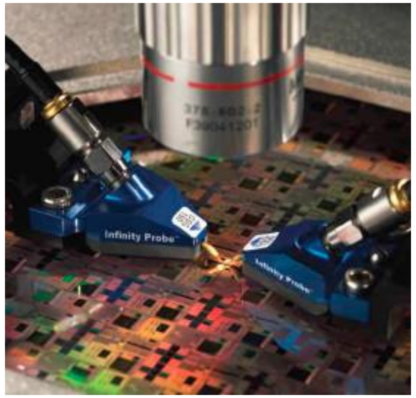
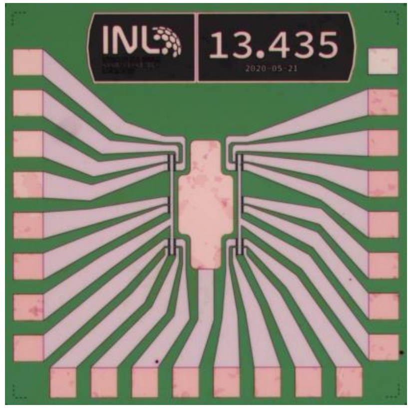
Guided Tour / Walk-through

Electron Beam Lithography

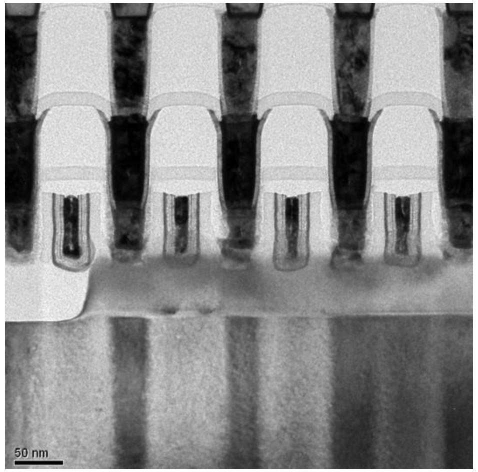
Electrical Characterisation



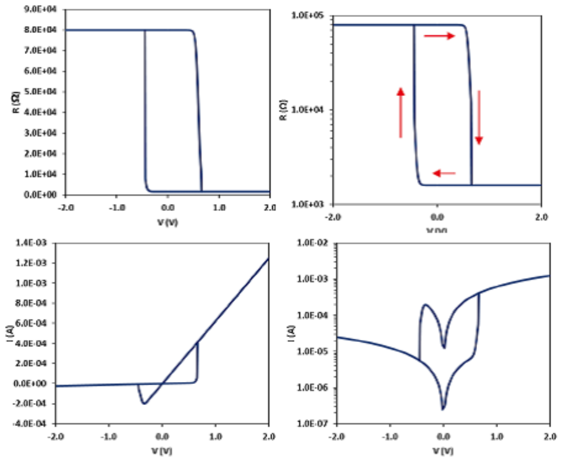
Graphene FET



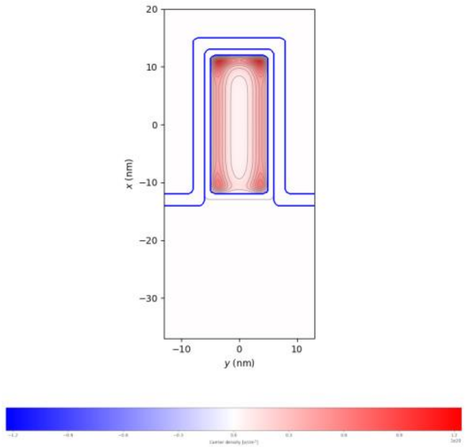
14nm FinFET



Resistive RAM Model



Si Nanowires Model



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ASCENT+ Interface Team

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Sign up
Enquire
Apply

Nicolas
Technical Contact

Paul
Access Coordinator

- 10 years experience of Infrastructure Access

- Fast response
- Managed professionally
- Technical assistance

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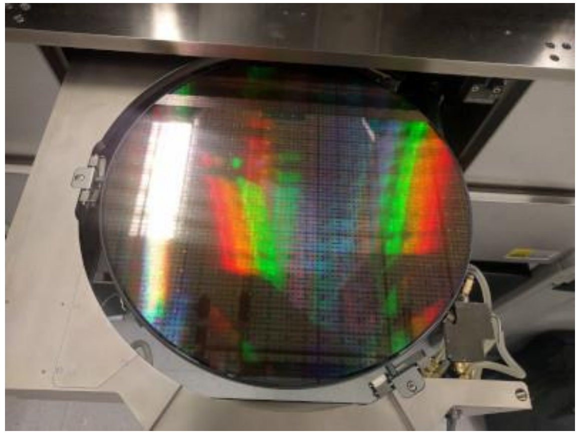
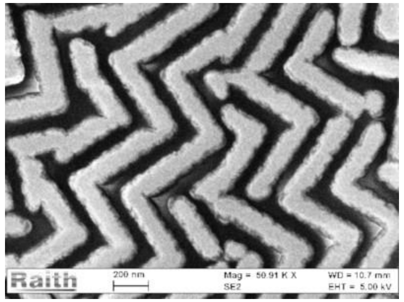
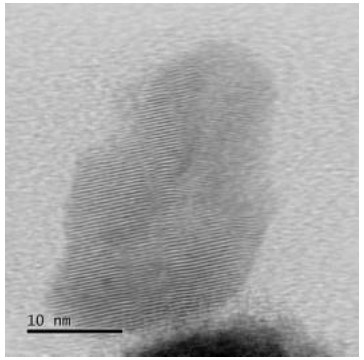
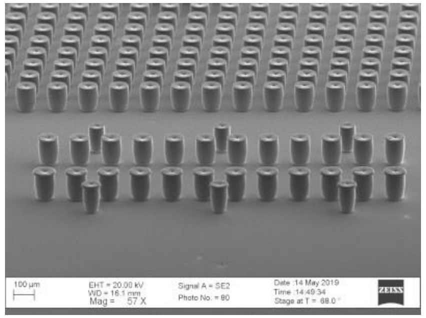
ASCENT+ Transnational Access

- Short/focused projects (e.g., proof-of-concept, validation/verification, feasibility study, test-chips)
- Free-of-charge
- One or more of these offerings
- At a single or multiple facilities
- Visit or remote









Case Study

I've fabricated topological insulators for QuBits. Could you help me to find out how good the interface is?

What materials are you working with? What thickness are your interfaces?

Te...

A and B. xxx nanometers.

Then our HR-TEM at Facility 4 is the best option for you

Facility

...oC)

User

Could you give me more details: number of samples, dimensions, handling restrictions, etc.

Yes sure. Here you are ….

Yes, I think this is suitable for a Transnational Access Project. We can do FIB HR-TEM for 3 samples during your visit and then do 4 more remotely.
Total: 12 days work

FAST & EASY

Great. Work together in the proposal and send it for evaluation once it's ready. Good luck!!

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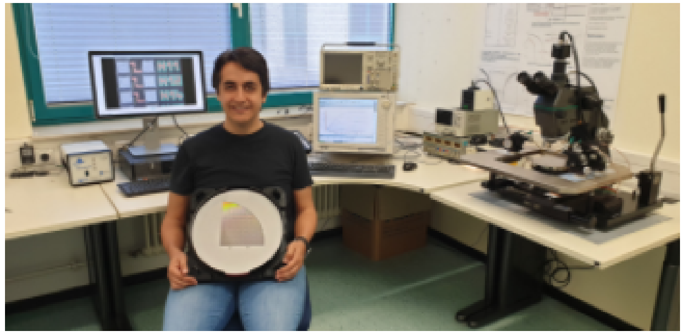
Use case 1: One quarter of a 300mm wafer from CEA-Leti for electrical characterization of SOI Ω-gate FETs



Ascent Project Ref No

153

User

Kerim Yilmaz

Affiliation

NanoP, THM University of Applied Sciences, Giessen, Germany

Description

The Nanoelectronics Device Modeling Research Group, led by Prof. Dr. Alexander Klös, focuses on device simulation and compact modeling of different type of transistors.

My PhD research tasks include the development of physics related modeling approaches for nanowire transistor structures, in particular considering three-dimensional effects on the electrical behavior.

I received one quarter of a 300mm wafer from CEA-Leti to perform electrical characterizations with our wafer prober, especially on the narrowest SOI Ω-gate NW FETs with different channel length. Of interest are devices with short-channel characteristics such as DIBL, slope degradation or VT roll-off.

The developed compact model for short and long channel cylindrical gate-all-around (GAA) MOSFETs shows good agreement with TCAD Sentaurus simulation data. The experimental data will allow to calibrate the simulator and to evaluate and prove the accuracy and reliability of the developed compact model.

It is a physics based unified model which provides analytical solution for the potential in the channel and can be used for DG, FinFET and GAA MOSFETs with minor changes in the core model.

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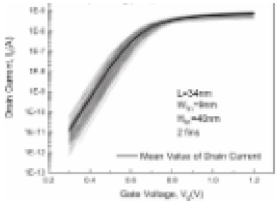
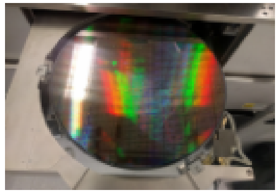
Use case 2: I_d-V_g measurements to investigate the variability of nanoscale triple-gate junctionless transistors at imec





Ascent Project Ref No

119

User

Theodoros A. Oproglidis

Affiliation

Aristotle University of Thessaloniki, Department of Physics, Thessaloniki, Greece

Description

The goal of this project is to investigate the variability of triple-gate junctionless transistors fabricated in imec, Belgium. ASCENT network provided the opportunity for a week’s visit to measure I-V characteristics from a large number of transistors in order to assess both local (matching pairs) and global variability. For this reason, various device technologies were selected. For the local variability investigation, channel length varies from 28nm to 34nm and for global variability from 26nm to 90nm for different number of fins. The devices’ fin width, fin height and channel doping are fixed and equal to 9nm, 40nm and 1.5×10^{18} cm^{-3} respectively.

The first results have confirmed the expected variability challenge for the triple-gate junctionless transistors, mainly due to their ultra-high doped channel. Our previous analytical compact model was formulated in order to be continuous and symmetric (verified using the Gummel Symmetry Test – GST) and is used to extract the ideality factor, threshold voltage, mobility, series resistance and the channel length modulation parameter from the variability measurements. The results following the statistical analysis of the aforementioned variables will be used to assess the sources of variability as well as predict the variability in the device performance.

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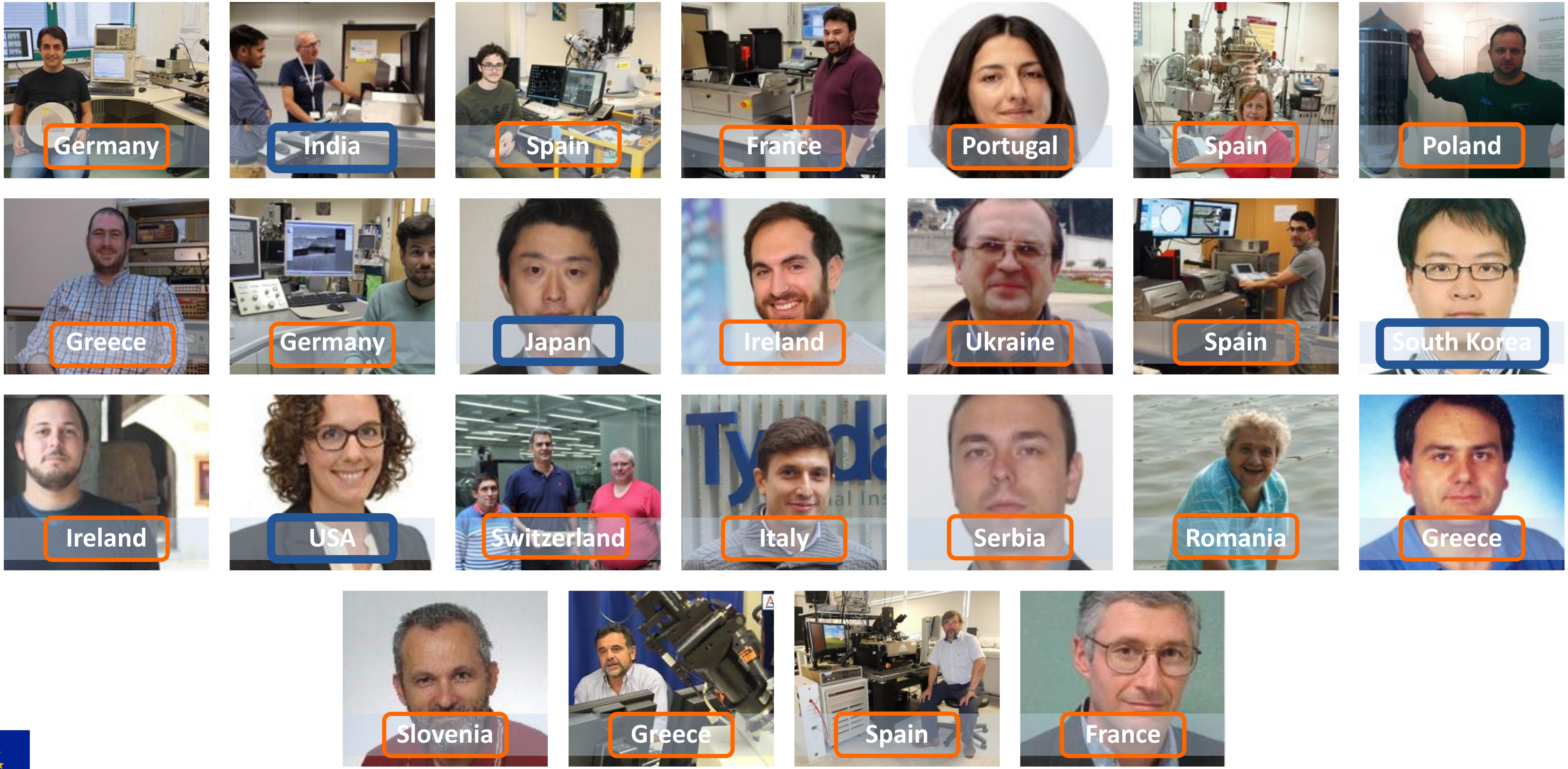
Open to the world



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Free of charge access projects from all over the world!

Phase 1: 100 projects to researchers from 30 countries

Number of members = 401   Number of countries = 42

Phase 2: 300+ projects available!!!

To academic and industry researchers worldwide

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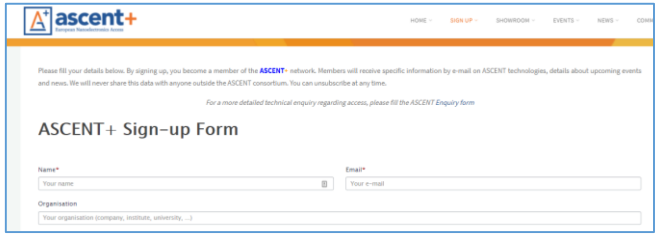
Summary: Stay connected!

- **Sign up: Keep up to date**
  https://www.ascent.network/contact/signupform/
  Upcoming webinars organised



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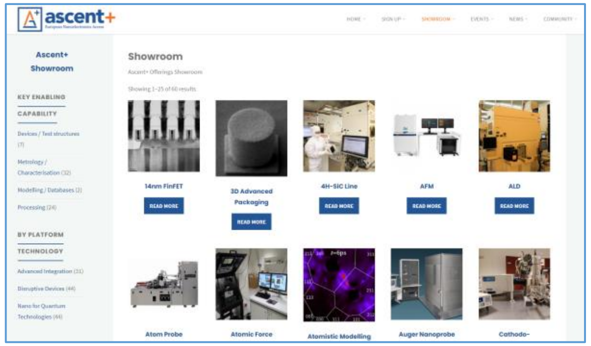

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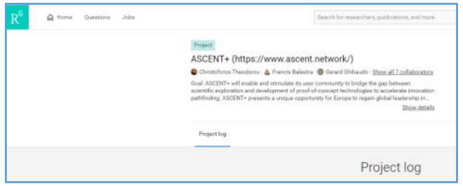

https://www.researchgate.net/project/ASCENT-https-wwwascentnetwork

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