# Physics-based SiC FET Model Upto High Current and Voltage Regions

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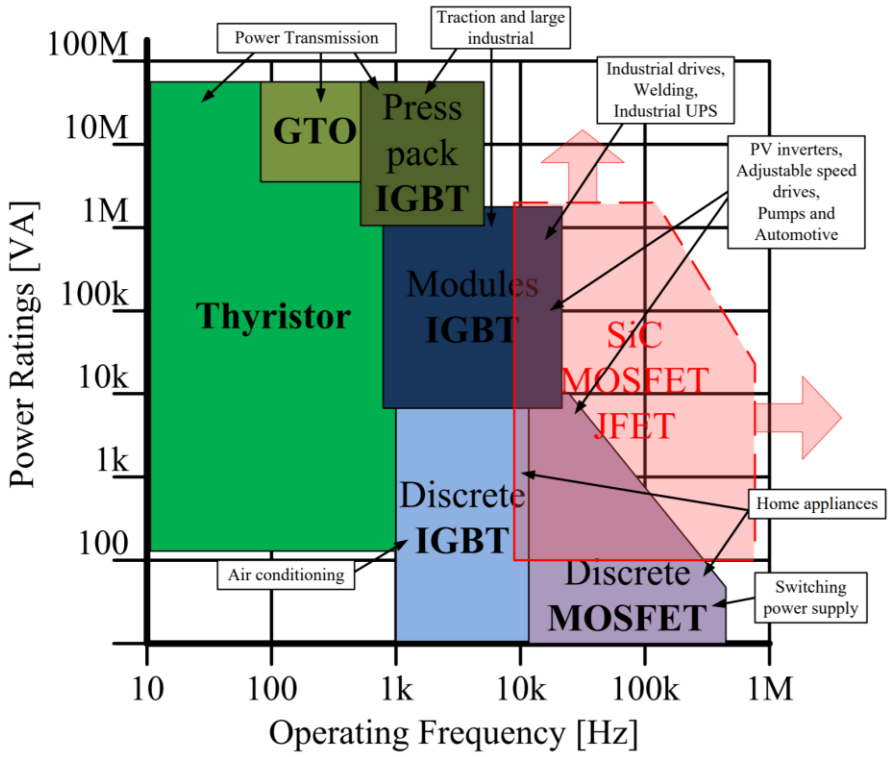
# Outline

- Silicon Carbide FET Technology Overview
- Status of compact models for SiC FETs
- Physics-based SiC FET model
- Model Results
- Summary

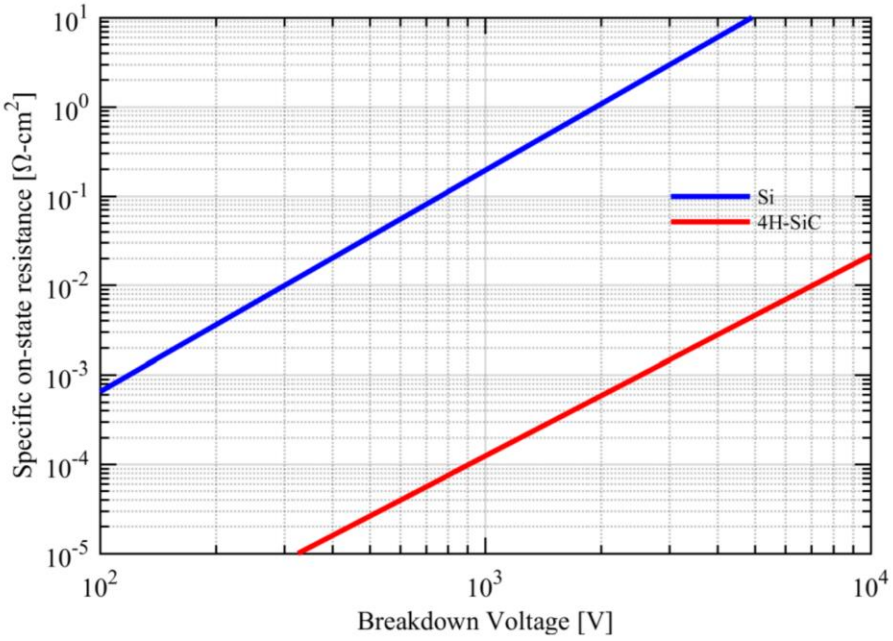
# SiC FET Technology Overview

## APPLICATION SPACE AND CAPABILITIES

SiC MOSFET
Application space



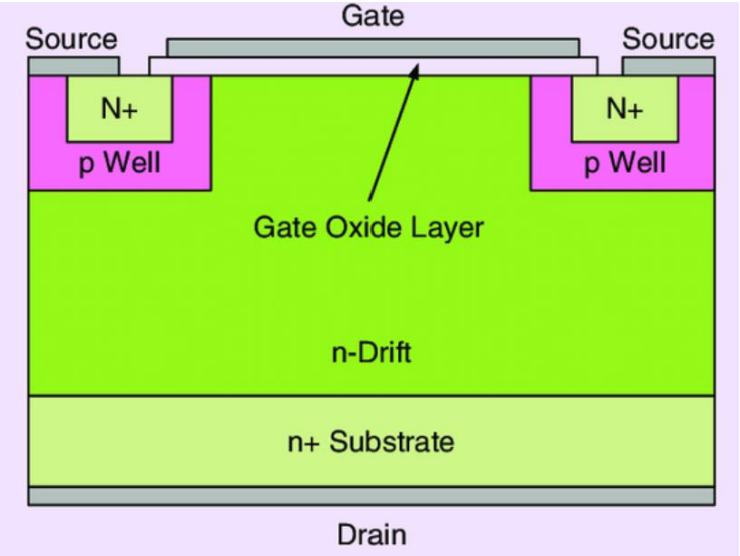

SiC MOSFET
Ron Vs BV



# SiC MOSFET Technology Overview

## DEVICE DESCRIPTION

- For VGS > VTH → P-well is inverted, leading to current flow vertically
- ON-resistance depends on channel resistance and drift region resistance
- For VGS < VTH → Channel is absent, hence very small current
- Blocking voltage is controlled by n-p diode formed by drift region and p-well



# Status of SiC FET compact models

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**SiC Compact Modeling Styles**

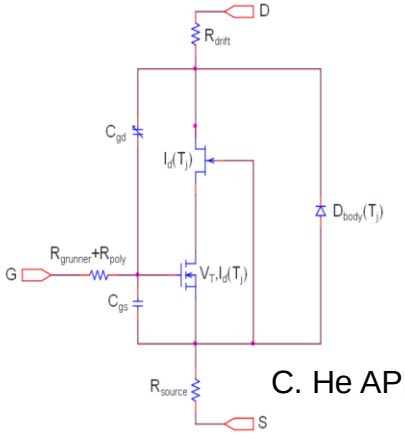
## Empirical Models

$$C_{\mathrm{gd}} = \begin{cases} A \tan h(aV_{\mathrm{gd}}) + B, & \text{if } V_{\mathrm{gd}} > 0 \\ C\ a \tan(aV_{\mathrm{gd}}) + D, & \text{if } V_{\mathrm{gd}} < 0 \end{cases}$$

Z. Dang IEEE Trans. Pow. Elect. 2018

## Equivalent Circuit Based

- BSIM3 FET
- Statistical ability




C. He APEC 2017

## VTH-based

- Piece-wise
- Continuous

$$I_{ds} = \frac{\beta}{1 + \frac{\beta V_{ds}}{g_{sat}}} \left( V_{geff} - \frac{k}{2} V_{ds} \right) V_{ds}$$

R. Kraus Trans. Power Elect. 2016

# Status of SiC FET compact models

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## SiC Compact Modeling Styles

**Empirical Models** (see slide # 5)

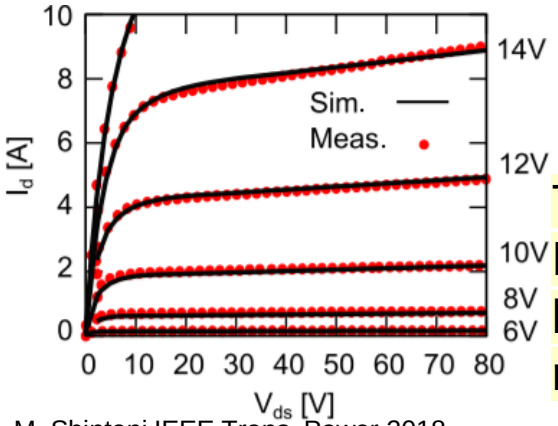
**Equivalent Circuit Based** (see slide # 5)

**VTH-based** (see slide # 5)

**Surface-potential-based**

$$I_{DD} = C_{ox}(V_{gs} - V'_{fbc} + \phi_t)(\phi_{sD} - \phi_{sS}) - \frac{1}{2}C_{ox}(\phi_{sD}^2 - \phi_{sS}^2)$$
$$- \frac{2}{3}\phi_t\sqrt{2\varepsilon_{SiC}kT \cdot \mathbf{NA}}\left\{\left(\frac{\phi_{sD}}{\phi_t} - 1\right)^{\frac{3}{2}} - \left(\frac{\phi_{sS}}{\phi_t} - 1\right)^{\frac{3}{2}}\right\}$$
$$+ \phi_t\sqrt{2\varepsilon_{SiC}kT \cdot \mathbf{NA}}\left\{\left(\frac{\phi_{sD}}{\phi_t} - 1\right)^{\frac{1}{2}} - \left(\frac{\phi_{sS}}{\phi_t} - 1\right)^{\frac{1}{2}}\right\}$$

M. Shintani IEEE Trans. Power 2018




M. Shintani IEEE Trans. Power 2018

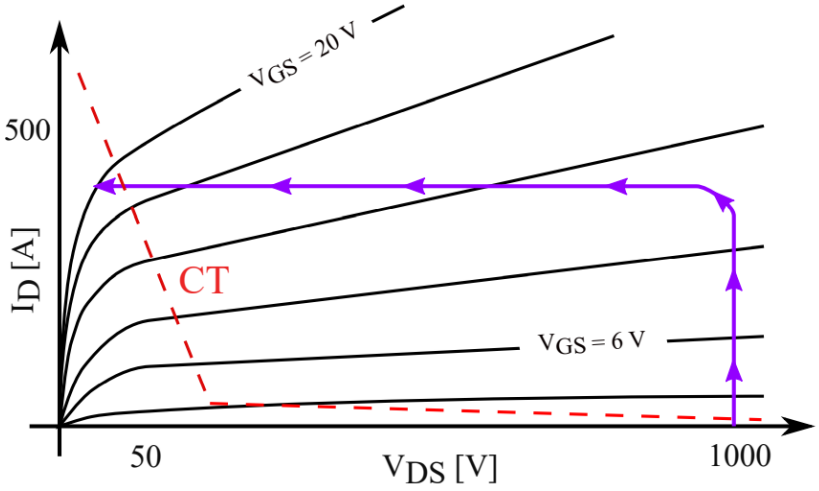
Typical validation of available Models do not include high current and voltage regions

# SiC FET Modeling

## IMPORTANCE OF HIGH CURRENT AND VOLTAGE REGIONS

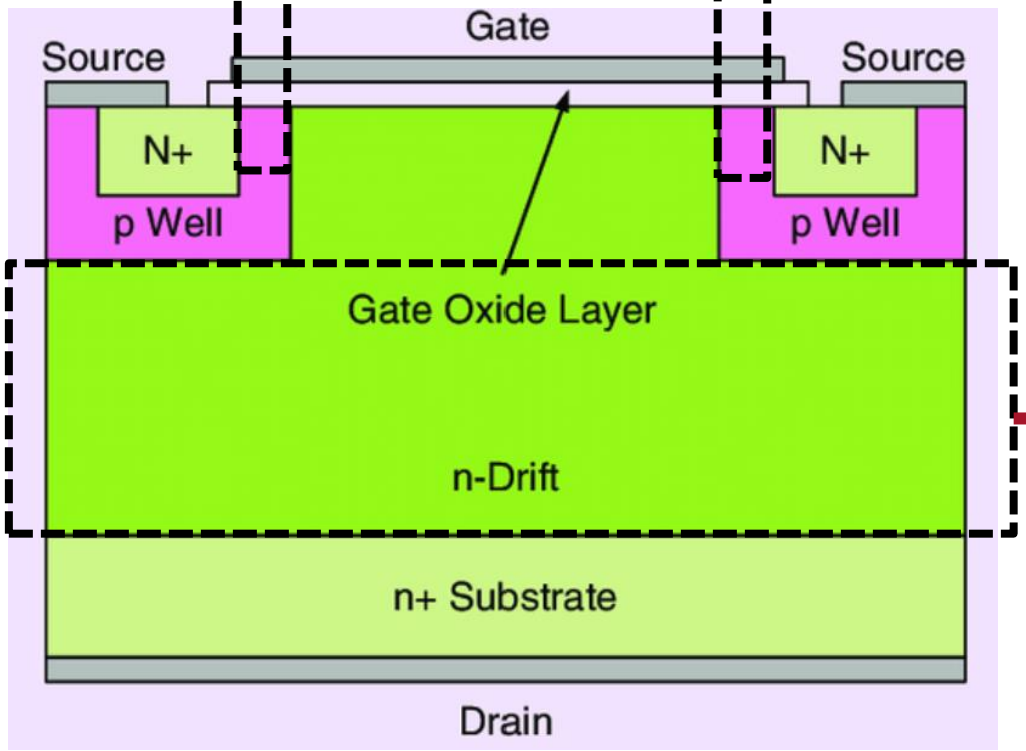
- Conventional current-tracer measurements do not capture the high I and V regions of the device behavior
  - As a result, no model validation is typically performed in these regions
- In circuit application during switching event the device will traverse high current and voltage regions

Red: Conventional Measurements range
Purple: Trajectory during switching




C. Salcines, WiPDA 2018

# SiC FET Model Development

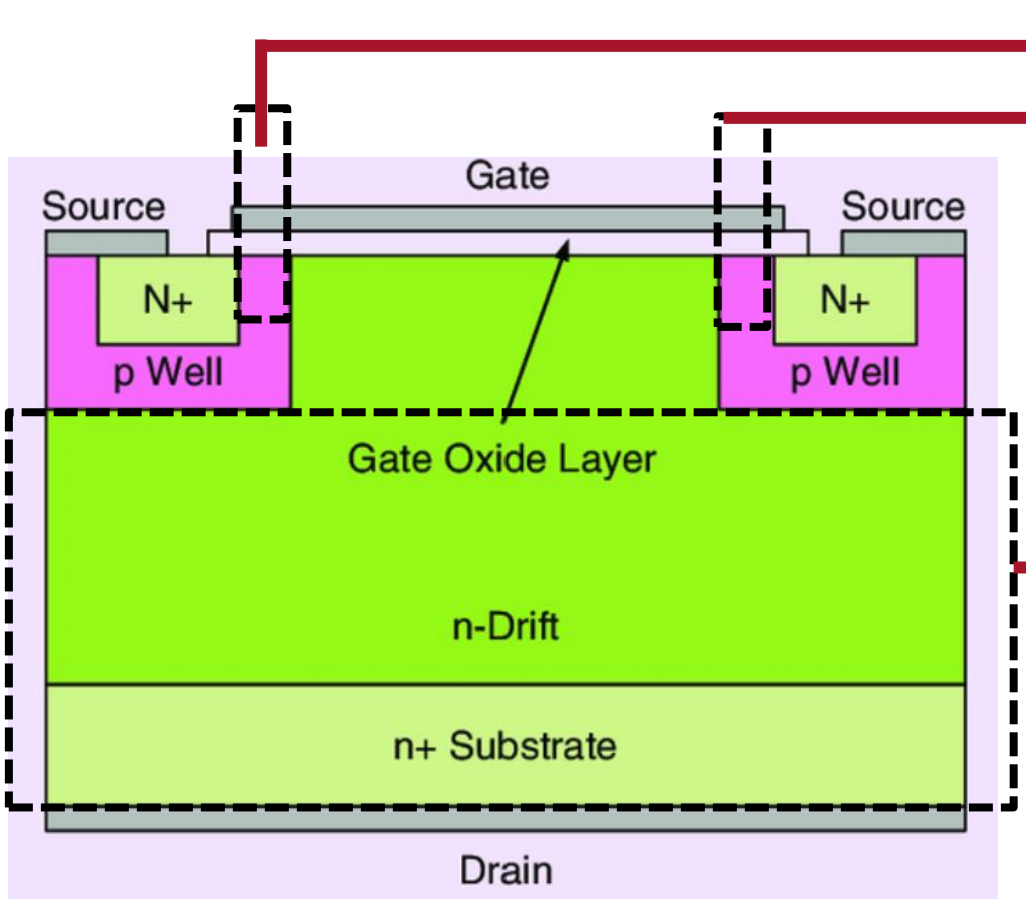



FET channel electrostatics and transport model

Drift region Model

**Can we apply known solutions to these regions?**

# SiC FET Model Development




FET channel electrostatics and transport
Model: EKV/BSIM6

Drift region
Model: ASM GaN

# SiC FET Model Development

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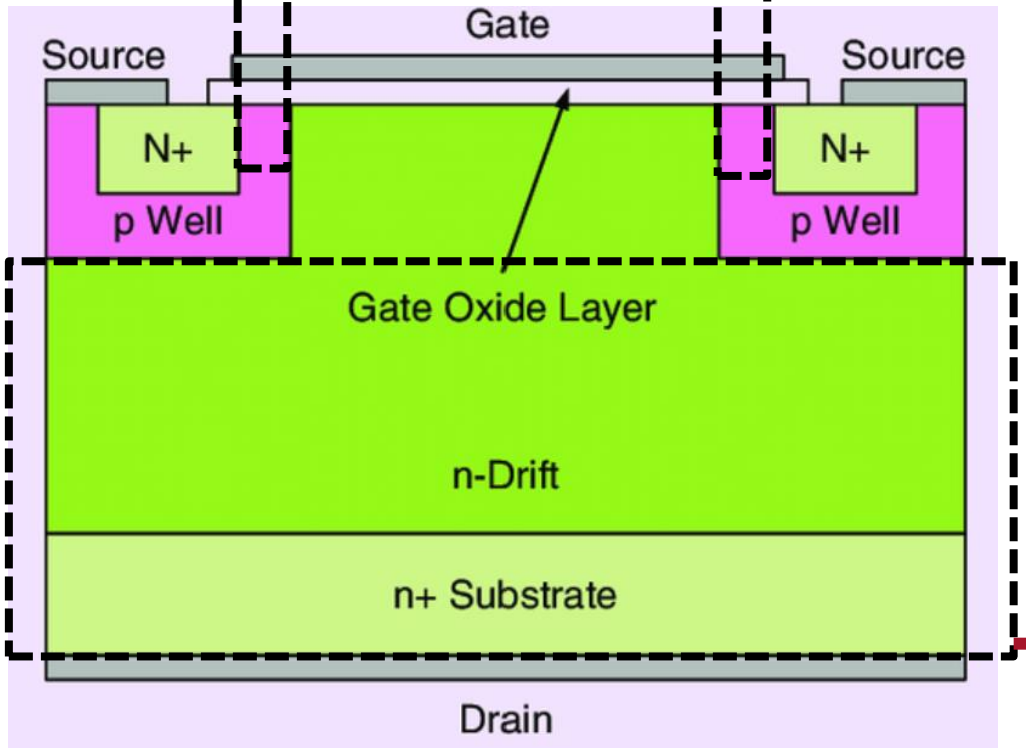
## FINDINGS WHEN KNOWN SOLUTIONS ARE DEPLOYED




FET channel electrostatics and transport
Model: EKV/BSIM6
**Need to account for SiO2/SiC interface charges**

Drift region
Model: ASM GaN

# SiC FET Model Development

Core charge model accounting for interface charges

$$V_{GS} - V_{FB} - \gamma\sqrt{\psi_s} - \frac{\alpha\psi_s}{1 + \frac{\alpha\psi_s}{N_{it}}} = 0$$

QS, QD

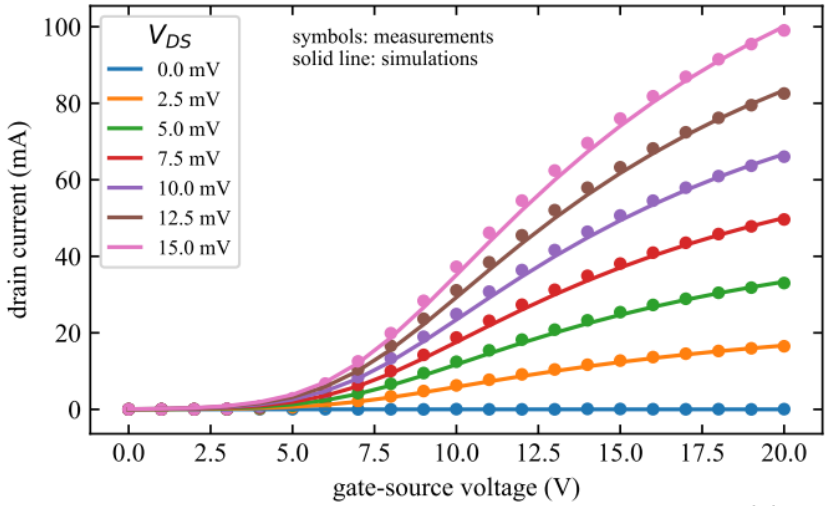
Mobility-field dependence
Velocity Saturation
Self-heating – multiple time-constants
Drift region model

ID

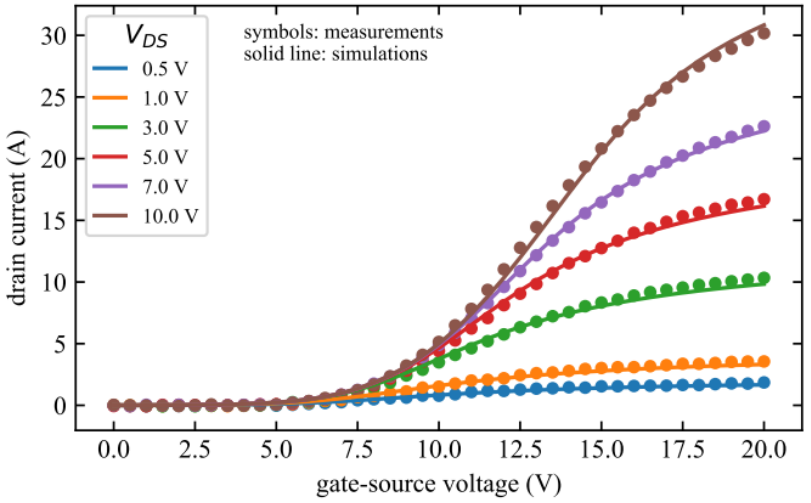
# Model validation

Symbols: Measurements
Line: Model

Low current




High current

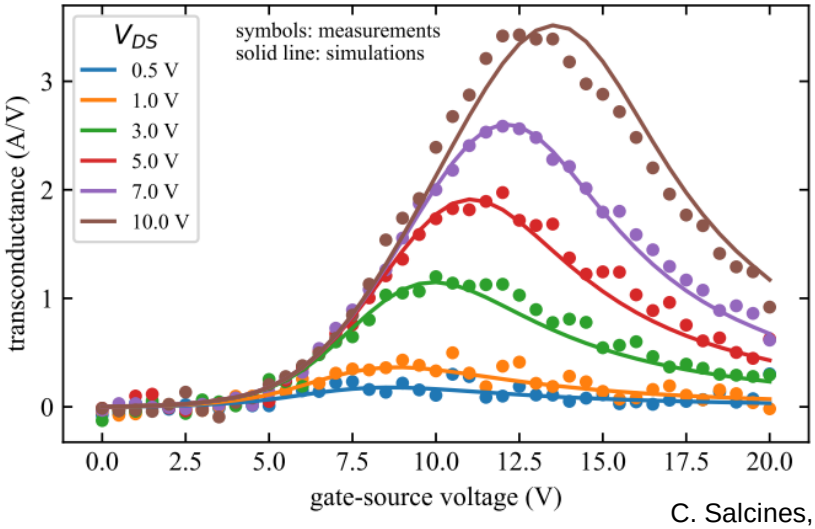



C. Salcines, PhD Thesis, In press

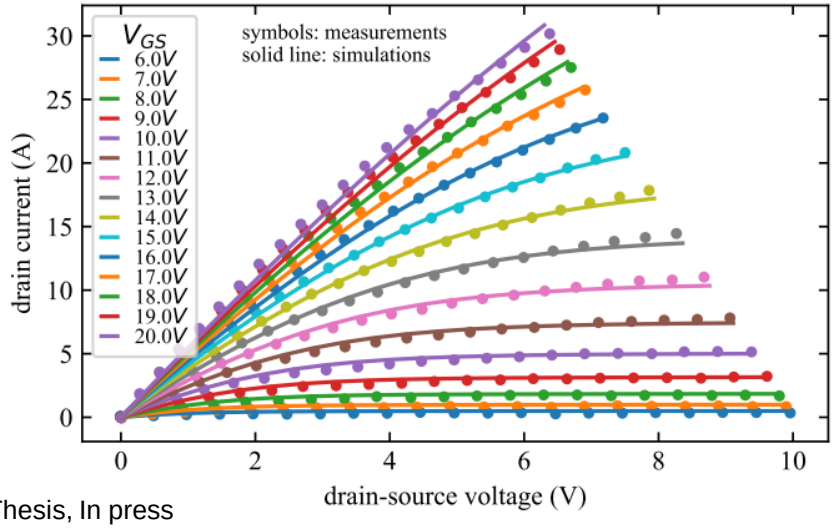
# Model validation

Symbols: Measurements
Line: Model

Trans-conductance




High current ~ 30 Amps

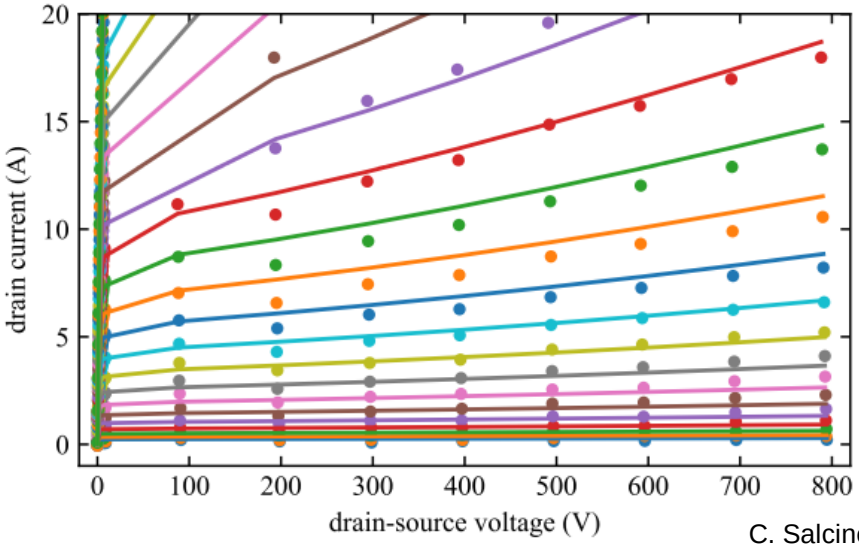



C. Salcines, PhD Thesis, In press

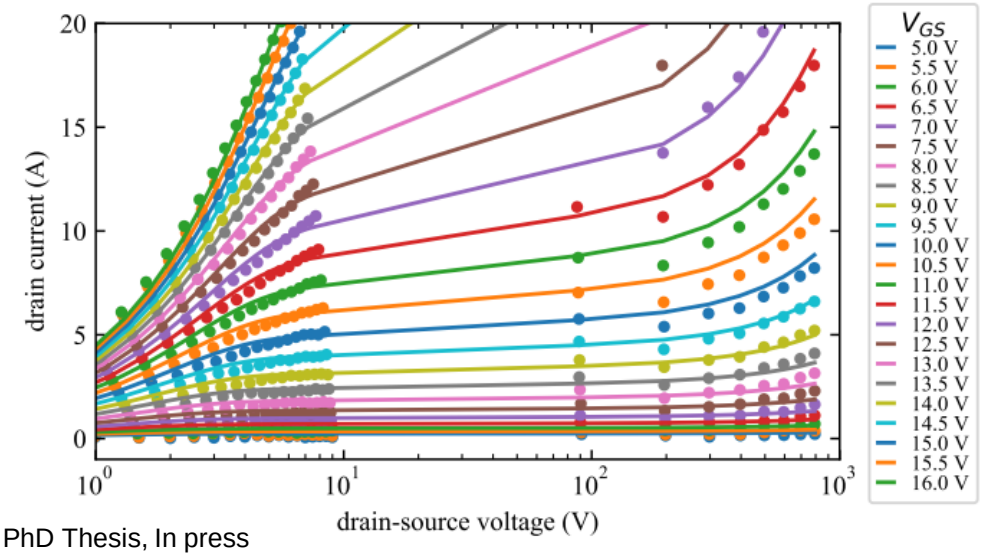
# Model validation

Symbols: Measurements
Line: Model

High Vds linear scale




High Vds log scale

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**Modeling high Vds regions need accounting of Nit and its temperature dependence**

# Summary

- Accurate physics-based compact model for SiC FETs capturing high current and high voltage regions developed
- It is found that the effect of interface charges and their temperature dependence is crucial in SiC FET models
- Model has been validated using novel characterization techniques to cover the high Ids, and high Vds parts of the device behavior

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# Thank You!